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A 121 dB SNDR Zoom ADC Using Dynamic Amplifier and Asynchronous SAR Quantizer

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Abstract: This paper presents a discrete-time zoom analog-to-digital converter (ADC) for low-bandwidth high-precision applications. It uses a coarse-conversion 5-bit asynchronous self-timed SAR ADC combined with a fine-conversion second-order delta-sigma modulator to efficiently obtain a high signal-to-noise distortion ratio (SNDR). An integrator circuit using a high-gain dynamic amplifier is proposed to achieve higher SNDR. The dynamic amplifier uses a switched tail current source to operate periodically, simplifying the common-mode feedback circuit, reducing unnecessary static current, and improving the PVT robustness. Dynamic error correction techniques, such as redundancy, chopping, and dynamic element matching (DEM) are used to achieve low offset and high linearity. And a 2-bit asynchronous SAR quantizer with an embedded feed-forward adder is used in the second-order delta-sigma modulator to reduce the quantization noise caused by redundancy, and further achieve higher energy efficiency. Simulation results show that the ADC achieves a peak SNDR of 121.1 dB in a 390 Hz bandwidth at a 200 kHz sampling clock while consuming only 170 μW from a 2.5 V supply and the core area is 0.55 mm^2. This results in a Schreier figure of merit (FoM) of 184.7 dB.

Keywords: analog-to-digital converter; zoom ADC; delta-sigma modulator; dynamic amplifier; asynchronous SAR; multi-bit quantizer

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1. Introduction

High precision applications, such as industrial measurements, medical diagnostics, and IoT devices, which are often slowly changing signals, are placing increasingly stringent requirements on the energy efficiency and performance of high-precision analog-to-digital converter designs. ΔΣ ADCs, which achieve high signal-to-noise ratios through oversampling and noise shaping [1,2], are often preferred for high-precision applications. However, conventional architectures of ΔΣ ADCs meeting all these requirements often result in low energy efficiency or high power consumption of the ADC, making them unsuitable for battery-driven autonomous systems. MASH or multi-bit architectures can achieve high resolution, but still only moderate energy efficiency [1,3,4]. SAR ADCs can be very energy efficient [5–8], but they are limited to medium bandwidth and medium resolution, and it is difficult to achieve high-resolution without calibration.

In recent years, many hybrid ADCs [8–12] have been proposed to combine the advantages of different architectures to achieve an outstanding performance that cannot be achieved by a single architecture. Zoom ADC [11,12] is a hybrid ADC that combines SAR ADC and ΔΣ ADC to achieve high resolution and high energy efficiency. The zoom ADC uses a two-step structure to zoom the reference range of the ΔΣ ADC to a small range near the input signal through SAR ADC coarse conversion, and unlike conventional two-step ADCs [13,14], the fine converter of the zoom ADC does not digitize the residuals of the coarse converter, so the accuracy of the conversion depends entirely on the accuracy

of the fine ΔΣ ADC. In addition, zooming relaxes the resolution requirement of the fine converter, which leads to shorter conversion times and smaller internal signal fluctuations, thus relaxing the requirement for amplifier swing rate in the integrator and reducing the power consumption of the fine ΔΣ modulator.

However, in order to make the whole system architecture efficient, the op-amps in the loop filter integrator must have high gain to avoid quantization noise leakage. Traditionally, they are implemented by high-gain OTAs with a cascaded structure [1,3]. However, they use static bias currents, and their common-mode feedback (CMFB) wastes a large amount of unnecessary static current in integrator circuits with time-varying operating conditions due to the long build-up time and the constant operation of the circuit. Inverter-based amplifiers [15] does not require bias circuits and have high energy efficiency, which makes them an attractive choice for integrators. However, the proposed topology does not provide the required DC gain and is susceptible to PVT variations. Moreover, zoom ADCs are usually designed to provide at least ±1 LSB redundancy [11,12,16,17] in coarse conversion results to relax the error requirements of coarse conversion SAR ADCs. In the case of 1-bit quantization ΔΣ, this means that the modulator DAC must span at least three SAR LSBS, which leads to a significant loss of signal-to-quantization noise ratio (SQNR).

In this paper, we propose a discrete-time (DT) zoom ADC architecture that mitigates the SQNR loss due to redundancy and achieves ultra-high SNDR with high energy efficiency, and propose a new integrator based on a dynamic amplifier. A folded input pair is used in the dynamic amplifier to improve input/output swing and linearity, and a cascaded output stage is used to increase the amplifier's gain even further. The impact of the gain error on the high-precision ADC is mitigated.The modulator can now operate dynamically, saving a significant amount of power by eliminating unnecessary static current. By combining this technology with a low-swing zoom ADC architecture, it is possible to achieve both low power and high accuracy. We also use a 2-bit asynchronous SAR quantizer with an embedded feedforward adder in the fine conversion modulator, which can fully utilize the DAC voltage level of the modulator, reduce the quantization noise due to redundancy, improve the SQNR by 9.5dB, and reduce the oversampling rate (OSR). Compared with the traditional flash multi-bit quantizer, asynchronous SAR saves more area and power. The first stage integrator in the zoom ADC is chopped to reduce its offset and 1/f noise, and in addition we employ a dynamic element matching (DEM) algorithm to mitigate the mismatch between the sampling capacitor cells, thus further improving the zoom ADC performance. The proposed ADC achieves a peak SNDR of 121.1 dB in a 390 Hz bandwidth at a 200 kHz sampling clock while consuming only 170 μW. This results in a Schreier figure of merit (FoM) of 184.7 dB.

The rest of the paper is organized as follows: Section 2 briefly describes the zoom ADC architecture and describes the selection of SAR ADCs and the effect of amplifier finite gain errors on the system. Section 3 discusses the implementation of the specific circuit. Simulation results are presented in Section 4. Finally, conclusions are given in Section 5.

2. Zoom ADC System Design

2.1. Zoom ADC Architecture

Figure 1 depicts the proposed system architecture. A coarse conversion asynchronous SAR ADC and a fine conversion two-order feedforward ΔΣ modulator are used in the proposed zoom ADC. The input signal is first quickly coarsely converted, and then the "zoom" operation allows the reference of the fine ADC to span exactly across the input signal, thus relaxing the requirement for fine ADC resolution and reducing the number of conversion cycles required. Zooming also reduces the swing of the loop filter input and relaxes the linearity and drive requirements of the ΔΣ integrator, resulting in increased energy efficiency.

Moreover, by this "zoom" operation, we can also enlarge the coefficients of the first stage integrator of the fine ΔΣ. For conventional ΔΣ ADC, the first stage coefficient is usually less than 1 to ensure the loop stability and avoid overloading the integrator [18].

In the ADC of this paper, we take the first stage coefficient to 1.55 by simulation. Due to the limitation of thermal noise, the sampling capacitance of the first stage is usually taken very large for high precision ADC, and by amplifying the coefficient of the first stage, the size of the integrator capacitance can be greatly reduced, thus reducing the load of the integrator op-amp and the area of the circuit.

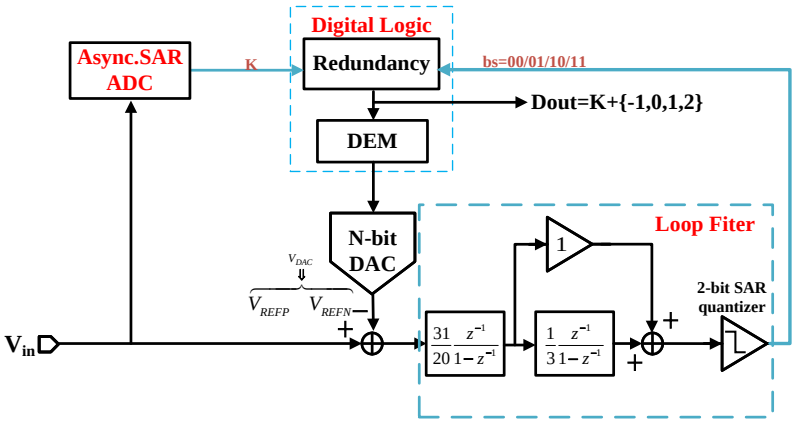


Figure 1. Block diagram of the zoom ADC with 2-bit second-order loop filtering and a coarse asynchronous SAR.

The digital code K generated after coarse conversion of the input signal in Figure 1 will be combined with the fine-converted code stream through digital logic and then converted to an analog signal through a DAC capacitor array as the high and low references for the fine ΔΣ modulator, as:

$$V_{REFP} = (K+1) \cdot V_{LSBSAR} \tag{1}$$

$$V_{REFN} = K \cdot V_{LSBSAR} \tag{2}$$

where V_{REFP} and V_{REFN} are the ΔΣ modulator's high and low references, respectively, and $V_{LSBSAR} = \frac{2 \cdot V_{REF}}{2^N}$ is the quantization step of the N-bit coarse conversion SAR.

It can be seen that since the reference voltage of the modulator is reduced by the SAR ADC from the full swing voltage $2 \cdot V_{REF}$ to $\frac{1}{2^N}$ of the previous one, reducing the resolution requirement of the modulator. Moreover, the amplitude of the input signal of the modulator becomes very small after the difference, so a simple and energy-efficient amplifier structure can be used in the integrator.

However, due to noise, linearity, and offset, we cannot guarantee that the coarse conversion SAR is error-free during conversion, as shown in Figure 2a, where the reference of the ΔΣ modulator cannot span the input signal due to coarse quantization conversion error, resulting in integrator overload.

To correct errors in coarse conversions, we introduce redundancy factors in the digital logic part where coarse and fine conversions are combined. As shown in Figure 2b, the input reference range of the ΔΣ can be extended by using redundancy. Even with possible errors, the input signal is accurately within that reference range. After incorporating the redundancy factor, the reference is denoted as:

$$V_{REFP} = (K+1+M) \cdot V_{LSBSAR} \tag{3}$$

$$V_{REFN} = (K-M) \cdot V_{LSBSAR} \tag{4}$$

where M is the redundancy factor needed to accommodate the non-ideal characteristics of the SAR ADC and ensure that the modulator remains in its stable operating range.

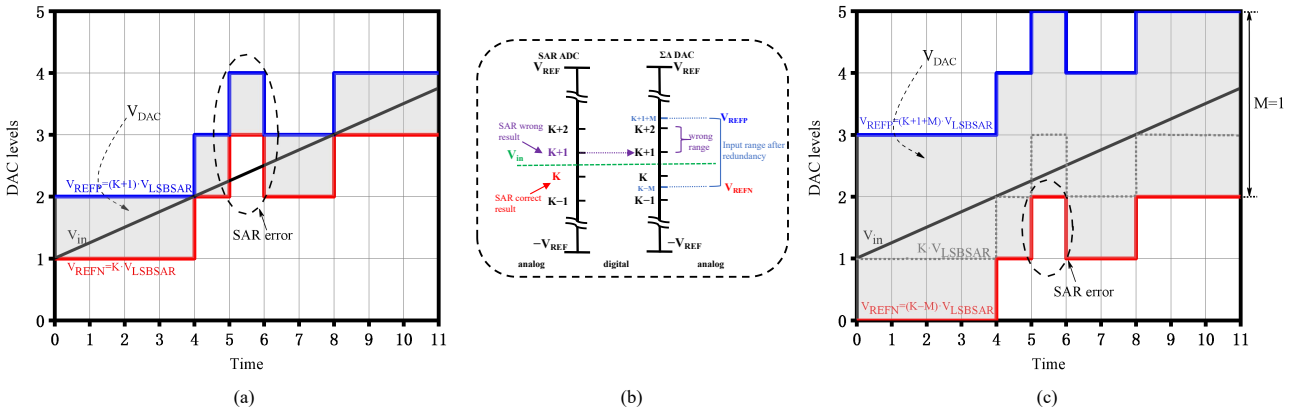


Figure 2. (**a**) Time domain waveform with coarse conversion error causing the input signal to be outside the reference range; (**b**) The coarse conversion result of the SAR ADC corresponds to the reference voltage range of the ΔΣ ADC; (**c**) Time domain waveform with input signal included in the reference range after redundancy.

With the use of redundancy factors, even if the coarse conversion ADC is not perfectly linear or there is a mismatch between coarse and fine conversion levels, as long as the error in the SAR conversion is below M LSBs, we can ensure that the input signal is always within the stable input range of the modulator, reducing the requirement for coarse conversion ADC performance metrics. As shown in Figure 2c, with redundant operation, we can ensure that the reference can span the entire signal despite the error in K. Therefore, SAR ADC does not limit the overall accuracy of zoom ADC.The combination of redundancy factor and quantizer output stream is completed by digital code.

However, ΔΣ DAC will span 3 V_{LSBSAR}, and this "redundancy" triples the quantization error of the modulator, reducing the SQNR by 9.5 dB compared to the case without redundancy. although this can be recovered by increasing the OSR, it is at the expense of power consumption.

To reduce the increase in quantization noise due to redundancy, we use a 2-bit SAR quantizer in the modulator quantizer section to take full advantage of the DAC level. This operation does not cause any change in the feedback DAC, and the dynamic element matching (DEM) scheme required to obtain high linearity remains unchanged. The resulting increase in SQNR results in a corresponding decrease in OSR, which in turn reduces both analog and digital power consumption, while the 2-bit asynchronous SAR quantizer uses only one comparator compared to the multi-bit flash quantizer, and can be combined with a feed-forward structured adder.

2.2. Maximum Input Frequency and Coarse Conversion Resolution

For the zoom ADC, the coarse conversion ADC works on a successive approximation principle that causes an N clock cycle delay in the update of the conversion result, which will result in a corresponding N clock cycle delay in the refresh of the resulting modulator reference voltage range. If the frequency of the input signal V_{in} is too high, the coarse ADC will not be able to update the reference range of the fine ADC fast enough, leading to an increase in distortion. In the following we analyze the maximum input frequency (F_{inmax}) that the zoom ADC can handle for a full-scale input signal.

For a sinusoidal signal, the fastest change in waveform occurs at the intersection of the signal and the x-axis, where the slope of the sinusoidal signal is greatest. For a full swing sinusoidal signal V_{in} with frequency f_{in} within the supply voltage V_{REF}, the maximum change in voltage within the conversion time T of the N-bit SAR ADC is expressed as:

$$\Delta V_{in} = V_{REF} \cdot T \cdot 2\pi \cdot f_{in} \tag{5}$$

According to Equations (3) and (4), the range of the zoom ADC stabilization input V_{zoom} can be expressed as:

$$\Delta V_{zoom} = V_{REFP} - V_{REFN} = (2M+1) \cdot \frac{V_{REF}}{2^{N-1}} \tag{6}$$

Need to ensure that the input signal variation ΔV_{in} is less than the stable reference range ΔV_{zoom}, brought into the two Equations (5) and (6), the maximum input signal frequency F_{inmax} is obtained as follows:

$$F_{inmax} < (2M+1) \cdot \frac{1}{2\pi \cdot 2^{N-1} \cdot T} \tag{7}$$

From Equation (7), it can be seen that the input frequency of the signal is inversely proportional to the conversion time T and resolution N of the SAR ADC and proportional to the redundancy factor M which ensures that the integrator is not overloaded.

In [11], the coarse SAR adc and fine ΔΣ ADC are executed sequentially, and the N-bit SAR ADC takes N cycles to calculate and update the coarse code K. A DR of 119.8 dB is achieved for the pseudo-DC input signal. however, due to its sequential operation, its bandwidth is limited to only 12.5 Hz.

As a result, instead of the traditional N-cycle SAR ADC, we use an asynchronous SAR ADC for the coarse conversion. The asynchronous SAR ADC computes the N-bit output code in a fraction of a clock cycle and ensures that it is transferred to the feedback DAC capacitor and updates the fine ADC reference range within half a sampling clock cycle. This cycle-by-cycle update of the fine reference means that the input only needs to remain within the fine reference for the duration of one cycle, which increases the maximum tolerable input frequency in (7), as well as allowing the use of a smaller redundancy factor.

The resolution of the coarse conversion ADC also determines the output swing of the fine integrator. The output range of the fine ΔΣ modulator integrator can be reduced by increasing the resolution of the coarse conversion ADC. Since the amplifier implementing the integrator function in the loop filter must provide accurate settling accuracy for the integrated charge, this can be achieved with less current and thus consume less power if the loop filter output has a smaller swing. Therefore, it is necessary to keep the integrator output swing as low as possible to improve energy efficiency.

With the signal-to-quantization noise ratio (SQNR) required to satisfy the design, we simulated the effect of coarse conversion ADC on fine conversion ADC integrator swing for different bits of N = 4, 5, 6 and redundancy factors M = 1, 2, 3. As shown in Figure 3, it can be seen that when M = 1, the loop filter input swing for N = 4 is approximately twice that of N = 5, resulting in a proportional increase in loop filter power consumption to maintain linearity. While a loop filter with N = 6 achieves a lower swing, the maximum tolerable input frequency of the zoom ADC is reduced and the accuracy requirements of the SAR ADC increase, requiring an additional redundancy factor. It also leads to an increase in quantization noise in the zoom ADC and an increase in integrator output swing. Moreover, as the resolution of the coarse quantized ADC increases, the complexity of its feedback DAC capacitance increases exponentially. For these reasons, a coarse resolution of N = 5 and redundancy of M = 1 is used in this design to provide the best trade-off among power consumption, signal tracking capability, and complexity.

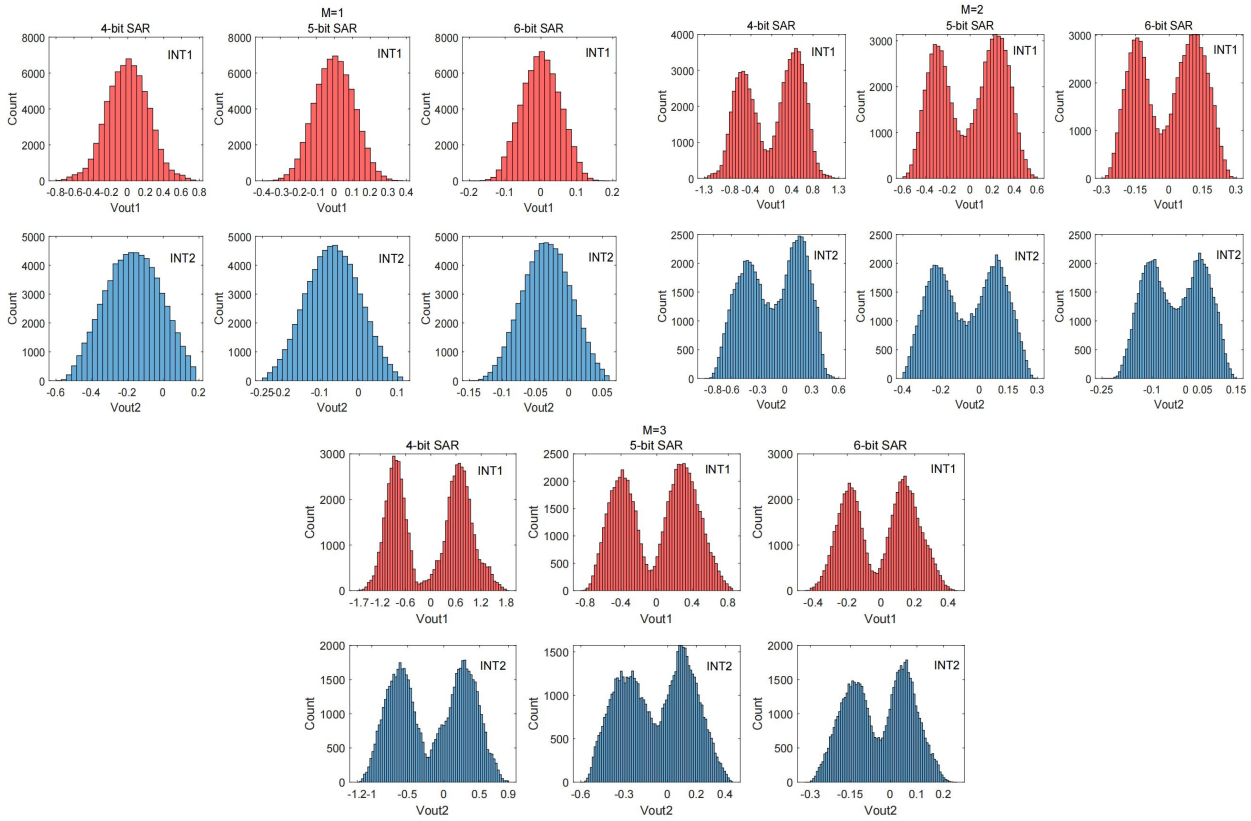


Figure 3. Output histogram of integrators INT1 and INT2 versus bits of coarse conversion ADC.

2.3. Amplifier Gain Error

The amplifier's finite DC gain and gain variation is a significant source of error in high-precision zoom ADCs. Figure 4 depicts a typical implementation structure of an integrator in a modulator, and analysis of the structure yields the expression as:

$$C_I[V_{out}(nT+T)+\frac{V_{out}(nT+T)}{A}]=C_I[V_{out}(nT)+\frac{V_{out}(nT)}{A}]+C_S[V_{in}(nT)-\frac{V_{out}(nT)}{A}] \tag{8}$$

As a result, the z-domain transfer function expression is obtained as:

$$H(z)=\frac{V_{out}(z)}{V_{in}(z)}=\frac{C_S}{C_I}[\frac{A}{1+A+\frac{C_S}{C_I}}]\frac{z^{-1}}{1-\frac{(1+A)}{(1+A+\frac{C_S}{C_I})}z^{-1}} \tag{9}$$

According to the above equation, the gain error is $\frac{A}{1+A+\frac{C_S}{C_I}}$, and the pole position shifts from $z=1$ to $z_p=\frac{(1+A)}{(1+A+\frac{C_S}{C_I})}$ in the unit circle.

The gain error has only a small effect on the signal transfer function (STF), but a change in the pole position causes the same shift in the zero position of the noise transfer function (*NTF*). For a second order modulator, due to gain error can result in:

$$NTF=(1-z_{p1}\cdot z^{-1})(1-z_{p2}\cdot z^{-1}) \tag{10}$$

where z_{p1} and z_{p2} denote the change in the pole position of the second stage integrator of the first stage integrator, respectively. At DC ($z=1$), the NTF is not zero but equals to $(1-z_{p1})(1-z_{p2})$. Similarly, at low frequencies, changes in the noise transfer function due to finite gain can have a large impact on low-frequency noise shaping.

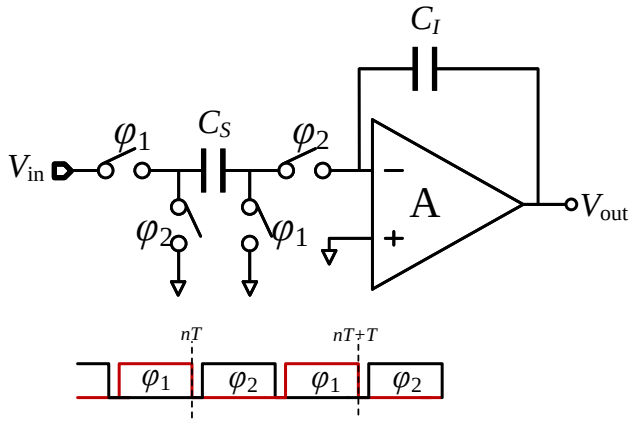


Figure 4. Switched-capacitor integrator with finite-gain amplifier.

However, the gain of the op-amp is constant in this assumption. In practice, the gain of the op-amp varies with its input voltage, and this variation can also lead to distortion. The variation for the DC gain can be approximated by a third-order polynomial [19] as follows:

$$A(V_{out}) = A_{dc} \cdot [1 - \delta(\frac{V_{out}}{V_{max}})] \tag{11}$$

where A_{dc} is the DC gain of fixed output, δ is the gain variation coefficient, usually taken as 0.9, which represents a significant third-order coefficient of variation, V_{out} is the output swing, and V_{max} is the maximum output swing.

Figure 5 depicts the modeling simulation of only the change in SQNR due to limited DC gain and amplifier gain variation in the zoom ADC integrator. It can be seen that a DC gain of 40 db causes a significant change in the noise transfer function (NTF) of the loop filter at low frequencies, which affects noise shaping and leads to a decrease in SQNR. To achieve the target SQNR of 130 dB (to allow a thermal noise-limited resolution of 20 bits) the DC gain of the amplifier must be at least 80 db or more for the effect of SQNR to be ignored. Although zoom type ADC can significantly reduce the integrator swing, considering the impact of op-amp gain on low-frequency high precision applications, we need to design a high gain and high linearity op-amp.

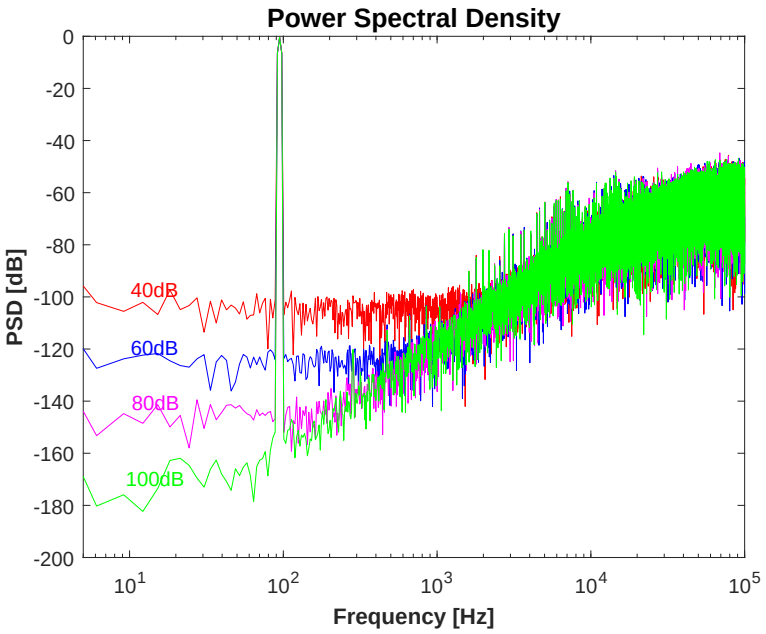


Figure 5. Effect of amplifier's DC gain and its nonlinearity on zoom ADC SQNR.

3. Circuit Implementation

The circuit schematic and timing diagram of the system is shown in Figure 6, which is composed of a 5-bit asynchronous SAR adc, a 2-bit SAR quantized two-order feed-forward ΔΣ modulator, and digital logic, where the redundancy factor is implemented by digital logic, and the specific details of the asynchronous SAR ADC circuit are shown in Section 3.2. Due to the better robustness of the switched capacitor (SC) circuit to voltage and process variations and clock jitter [20], a discrete-time (DT) modulator is used, where the switched-capacitor adder that implements the feedforward path is embedded in the SAR quantizer. We use bootstrap switches [21] in both coarse SAR ADC and ΔΣ modulator sampling switches to ensure the linearity of the circuit. The input sampling capacitor C_S is also used as a feedback DAC capacitor array and consists of 31 unit capacitors C_{Sj}, which, along with the OSR, determines the zoom ADC's thermal noise level.

During the circuit operation, the input is sampled using a fully differential sampling structure, and the sampling time of SAR ADC and ΔΣ is kept at half-clock cycle intervals to minimize the coupling between them. At $\varphi 1$ phase, the asynchronous SAR ADC tracks the input signal and at the end of the $\varphi 1$ phase, the SAR ADC completes signal sampling. The comparison of SAR ADC is triggered on the rising edge of $\varphi 2$, because using an asynchronous clock, SAR ADC can complete the comparison and output the digital code K in a very short time. After that, the digital logic combines the digital code K and the integrator output code bs and converts them to 31 thermometer codes. After processing by the DWA algorithm, it passes to the 31 cell components of the feedback capacitor DAC to generate the appropriate feedback reference voltage.

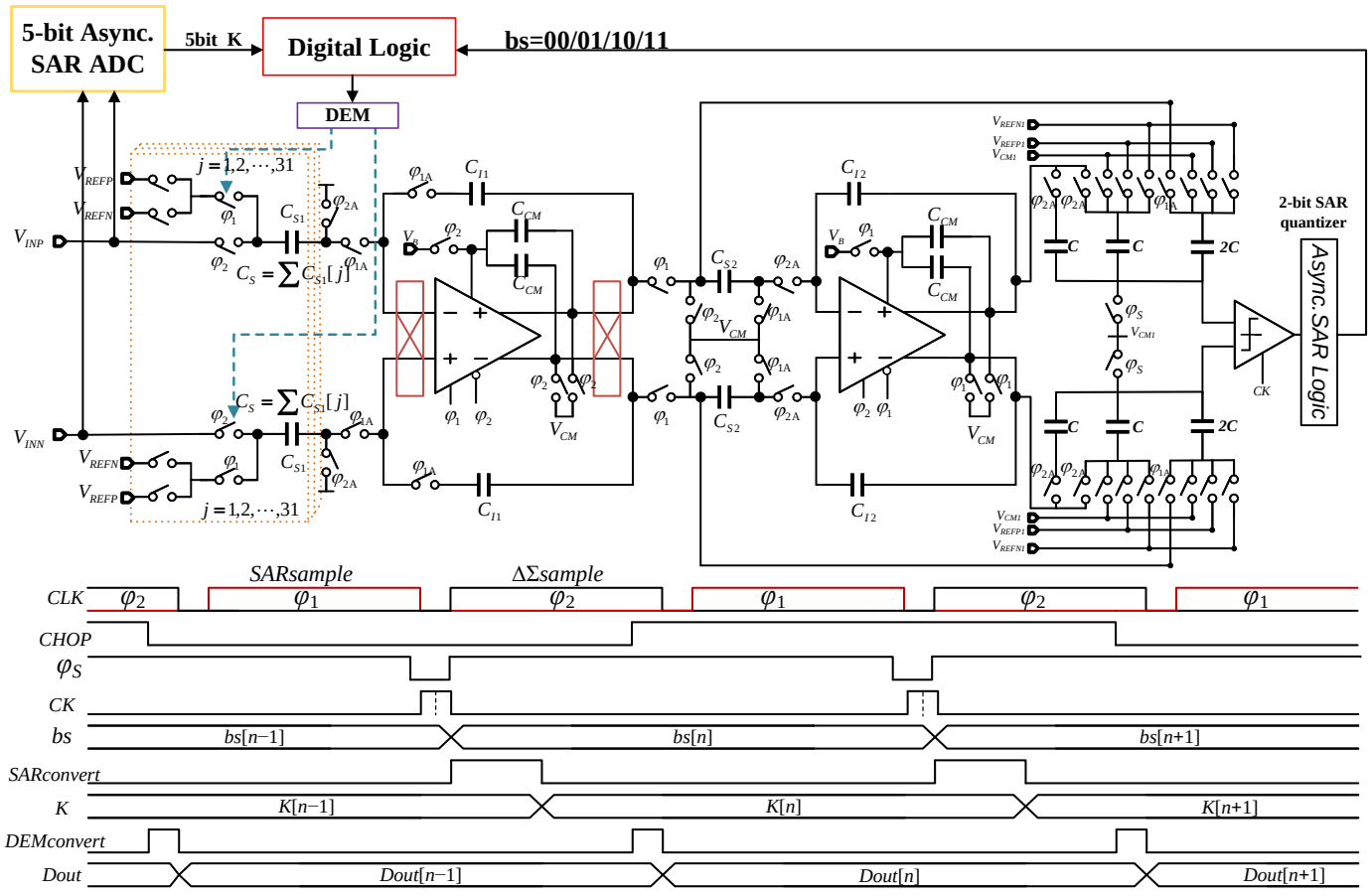


Figure 6. Simplified circuit diagram of the proposed zoom ADC and the corresponding timing diagram.

The ΔΣ ADC tracks the input signal during the $\varphi 2$ phase while the first-stage integrator is chopped to suppress the first-stage amplifier's offset and $\frac{1}{f}$ noise. At the end of $\varphi 2$,

the input is sampled to C_S. And at the $\varphi 1$ phase, the first stage integrator performs integration while completing the subtraction of the feedback result from the input signal.

Since there is no residual calculation in the zoom ADC, its thermal noise level is determined by the noise of the fine ADC only. Considering the SNDR requirement and the limitation of thermal noise kt/c, the total sampling capacitance C_S in this design is set to 8.9 pF, which is then subdivided into 31 unit capacitors and also used as the unit capacitance of the feedback DAC with a capacitance of 288 fF. The size of the first stage integrating capacitor C_{I1} is 5.7 pF. With the help of noise shaping and the high gain of the first stage, the sampling capacitance C_{S2} is relaxed to 188 fF and the integrating capacitor C_{I2} is 564 fF. In addition, the offset and kt/c noise of OTA2 and SAR comparator are similarly relaxed.

3.1. Dynamic Amplifier

Figure 7 shows the schematic diagram of the proposed dynamic amplifier circuit. The dynamic amplifier employs a folded PMOS input pair transistor to improve the input/output swing and linearity. Compared with NMOS, PMOS has lower flicker noise and is suitable as an input stage, and a cascaded output stage is used to further improve the gain of the amplifier.

In contrast to previous dynamic amplifiers [18,22,23], we use a switched tail current source instead of directly using switches or capacitors. By providing a fixed tail current source when the amplifier is operating, firstly it helps to define the output CM voltage precisely, and secondly, this avoids the sensitivity of the transconductance to the input CM level. When the amplifier does not operate, the tail current source is turned off by a switch to reduce power consumption.

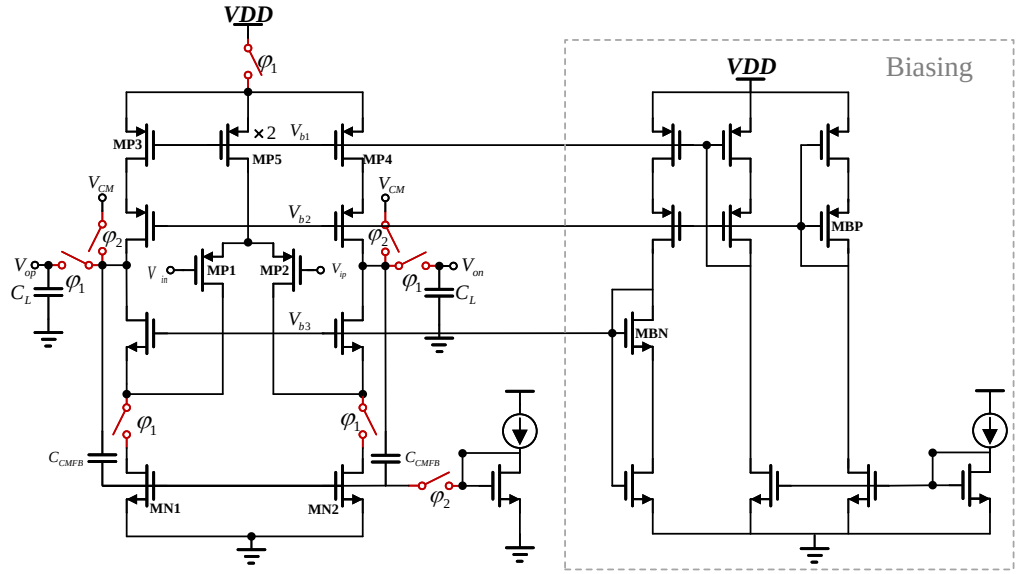


Figure 7. Schematic of a dynamic amplifier with bias circuit.

The circuits V_{b1} and V_{b2} and V_{b3} are set by static bias circuits. The amplifiers described in [11,12] are dynamically biased, but require additional switches and bias voltage storage capacitors, resulting in a complex circuit structure and not very energy efficient. In this design, the folded structure of the dynamic amplifier relaxes the input-output swing requirements, and the coarse conversion ADC reduces the output swing of the amplifier, so we use a simple static bias circuit where the head and tail current sources MP3-4 and MN1-2 bias the 40 µA current from a constant gm reference mirror when the switch is closed, thus suppressing the effects of supply voltage and temperature variations. Diode-connected transistors, MBP, are used to track threshold voltage changes and bias the amplifier cascade transistors to ensure that the entire circuit remains stable between PVT changes.

The second stage amplifier uses the same structure as the first stage, and because the high gain of the first stage amplifier relaxes the noise and linearity requirements, the second stage draws five times less current than the first stage, consuming only 8 µA during operation. Both dynamic amplifiers use the same static bias circuit, which consumes only 4 µA of current.

According to Figure 7, we can derive the small signal voltage gain of the dynamic amplifier. For simplicity, think of it as a single-pole system, the average values $g_{m1,2}$ and R_{out} are used to model the transconductance and output resistances at different MOS drain voltages. The gain can be derived as:

$$Gain = g_{m1,2}R_{out}(1 - e^{-\frac{t}{\tau}}) \tag{12}$$

where $\tau = R_{out}C_L$ is the time constant of this single-pole system and $R_{out} \approx (g_{mN}r_{ON}^2) \parallel (g_{mP}r_{OP}^2)$ is the output resistance of the entire circuit. For different amplification times, the gain of Equation (12) can be approximated in two different forms:

When $t \ll \tau$:

$$Gain \approx \frac{g_{m1,2}}{C_L}t \tag{13}$$

And when $t \gg \tau$:

$$Gain \approx g_{m1,2}R_{out} \tag{14}$$

Equations (12)–(14) reveal the dynamic characteristics of the amplifier. Initially, the voltage gain varies linearly with (13), in accordance with the exponential law in (12), and eventually reaches the final value in (14). According to the condition in (14), it can be seen that when used for low-speed applications, the dynamic amplifier will show a voltage gain commensurate with that of a conventional amplifier. The difference is that the CM output voltage of the dynamic amplifier will vary instead of the constant value of the conventional amplifier. In fact, a dynamic amplifier can produce normal amplification as long as the value of the CM output voltage is not so low as to bring the transistor into the linear region.

As shown in Figure 8a, dynamic amplifier operation can be divided into two processes, the reset phase, and the amplification phase. In the reset phase (φ1 low, φ2 high) the amplifier stops operating and the amplifier output is reset to the common-mode voltage V_{CM}. And in the amplification phase (φ1 high, φ2 low) the amplifier starts operating and charges the load capacitor C_L at the output, after which the output voltage V_{op}/V_{on} will remain constant until the next reset phase starts.

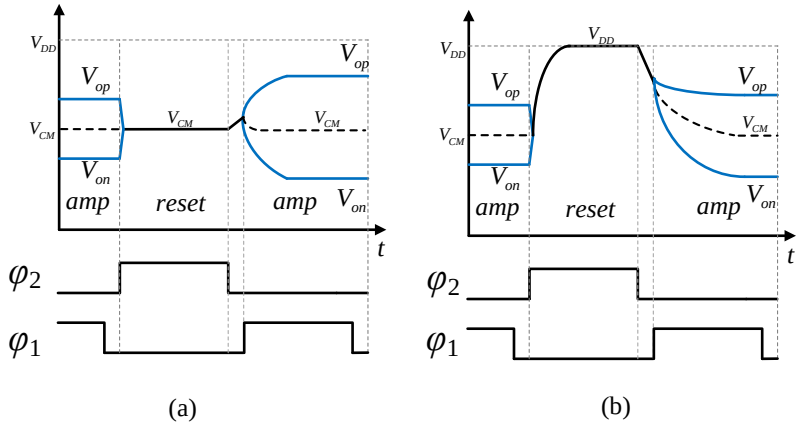


Figure 8. (**a**) Proposed dynamic amplifier timing and output voltage variation. (**b**) The associated CM voltage drop effects proposed in [18,22].

Compared to the previous dynamic amplifier [18,22], as shown in Figure 8b. In the reset phase, the outputs are all pulled to V_{DD}. In the amplification phase, the output voltage

will start to drop from V_{DD} towards V_{CM}, and the amplifier is not working properly when it is not dropped to the V_{CM} range, which severely limits the amplification time in the integration phase. In the proposed dynamic amplifier, the output voltage no longer drops rapidly from V_{DD} to V_{CM}, but operates directly from the common-mode voltage V_{CM}, and the whole amplifier can enter the amplification state quickly, which allows the proposed amplifier to stabilize faster and the amplification time can be longer to achieve the amplified state shown in Equation (14).

As shown in Figure 9, the integrator switching logic using dynamic amplifiers differs from that of conventional integrators in that firstly. As shown in Figure 9a, in the first stage reset/sampling phase, the amplifier is reset off, one pole plate of C_{CM1} and C_{CM2} is connected to V_{CM} and the other pole plate is connected to the gate of bias circuit transistor MB, and each capacitor voltage is charged to $V_{CM} - V_B$ by bias current; at the same time the output V_{op}, V_{on} are pulled to V_{CM}. Although this reset operation clears the output voltage of the integrator, the charge information remains on the gates of amplifiers $MP1$ and $MP2$ and on the top plate of the integrator capacitor C_{I1} due to charge conservation. Therefore, the periodic reset operation never destroys the integrated charge in C_{I1} and C_{I2}, ensuring proper integrator operation.

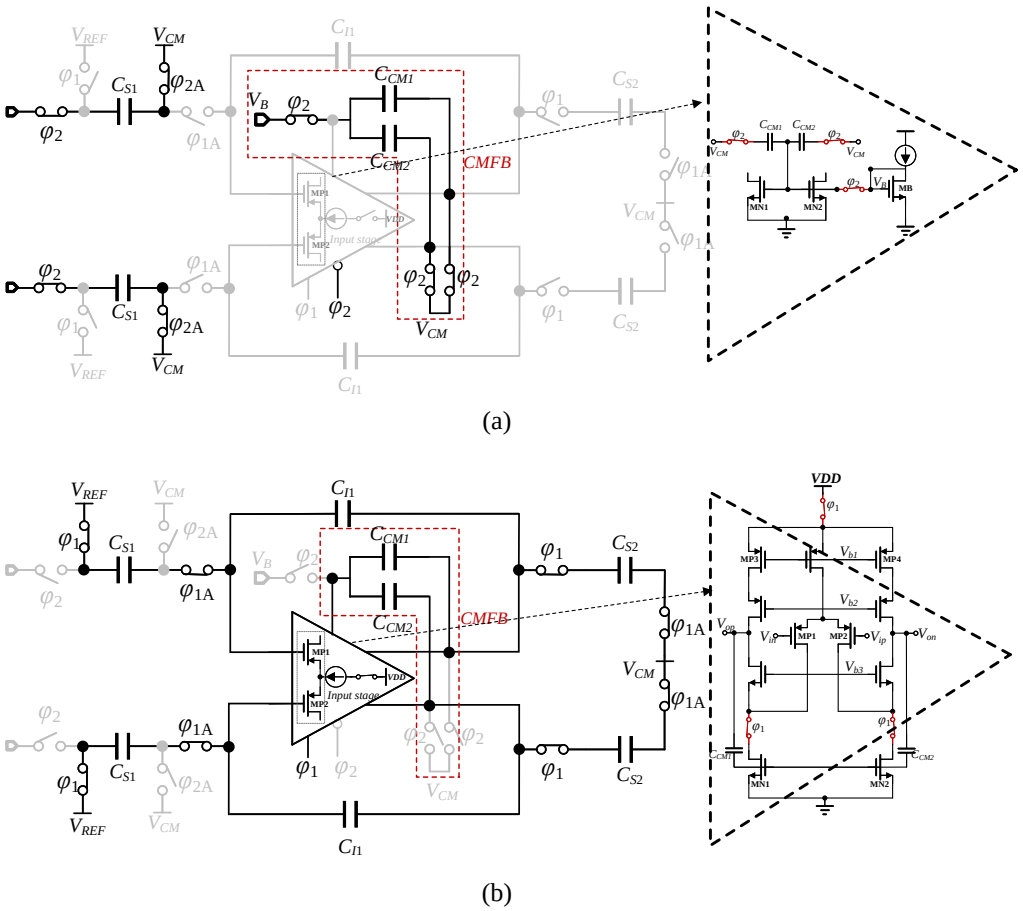


Figure 9. Working principle based on dynamic amplifier integrator: (**a**) sample/reset; (**b**) integrate/amplify.

And in the first stage amplification/integration phase, as shown in Figure 9b, the dynamic amplifier starts amplification, and the $\varphi 2$ switch is opened. The output common-mode level generated at the output of the amplifier is equal to $V_{CM} - V_B + V_{GSN1,2}$, and we make the output common-mode level equal to V_{CM} by ensuring that $V_B = V_{GSN1,2}$, which is very easy to achieve with the fixed tail current source provided in the dynamic amplifier. Also, during the amplification phase, the sampling capacitor of the second stage integrator

is connected to the output of the first stage to sample the integration result of the first stage, while the second stage dynamic amplifier is in the reset phase. By operating the two amplifiers periodically, unnecessary quiescent currents are eliminated, resulting in a significant increase in integrator energy efficiency.

As shown in Equation (12)–(14), in a dynamic amplifier, the characteristics change with time. For this purpose, we simulated the variation of the DC gain and phase margin of the proposed amplifier for different PVT variations when the amplifier is operating stably during the integration process, as shown in Figure 10, where VDD = 2.5 V and the equivalent load capacitance size is 4 pF, the simulation results show that the DC gain of the amplifier can reach more than 80 dB under different PVT variations, and the unit gain bandwidth and phase margin can also remain stable.

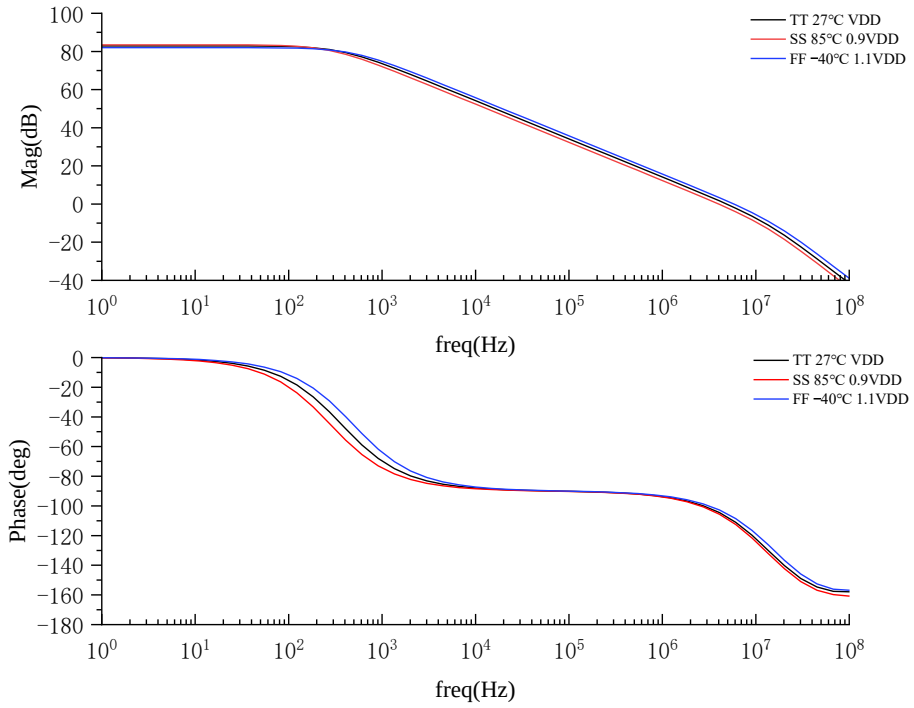


Figure 10. Gain and phase bode diagram of the amplifier in integrated/amplified phase.

3.2. Coarse Conversion Asynchronous SAR ADC

The method of updating the ΔΣ modulator reference for each clock cycle using asynchronous SAR improves the tracking capability of the signal and also relaxes the input swing of the integrator in the loop filter. In this paper, a modified asynchronous SAR ADC based on the VCM scheme, also known as the merged capacitor switch (MCS) scheme [24] is used with the circuit structure shown in Figure 11.

The switching scheme uses top plate sampling, so the signal is sampled in $\varphi 1$ cycle with the input connected to the top plate of the capacitor array and the bottom plate connected to the V_{CM} voltage. The MSB is determined by comparison immediately after sampling without consuming any energy in the capacitor array. Further, 'UP' and 'DOWN' transitions are symmetrical and consume equal energy. Accordingly, we don't need energy from V_{CM} in each bit-cycling. Although the generation of the common mode voltage requires additional circuitry compared to the traditional switching scheme, in the zoom ADC we can share a V_{CM} with the fine ΔΣ modulator, and the MCS scheme requires only half the capacitor array of the conventional switching scheme for the same accuracy.

The asynchronous logic uses self-timed control logic. The operation is triggered by the rising edge of $\varphi 2$. These five comparisons of the asynchronous SAR ADC occupy only a small portion of the $\varphi 2$ cycle; the DEM and thermometer decoding will occupy the rest of $\varphi 2$.

As mentioned in Section 2.1, the redundancy relaxes all the constraints of the SAR ADC such as noise, offset, and linearity. Since 1 V_{LSBSAR} redundancy is used, the total SAR error should be limited to 1 V_{LSBSAR}. the cell capacitor of the SAR DAC in the design is chosen to be 85 fF with more than 10 bits of accuracy. Because this design is mainly for low frequency and high precision applications, the circuit frequency is not high. The use of large capacitors in the coarse SAR ADC, compared to the resulting increase in power consumption, we think that smaller noise and higher linearity are more important. The asynchronous SAR ADC completes the conversion in less than 20% of the zoom ADC sampling period (across PVT variations). To mitigate kickback noise due to fast asynchronous operation, a dynamic comparator with a constant current bias preamplifier is used [25]. The power consumption of the preamplifier is minimized by keeping it off during the signal sampling phase.

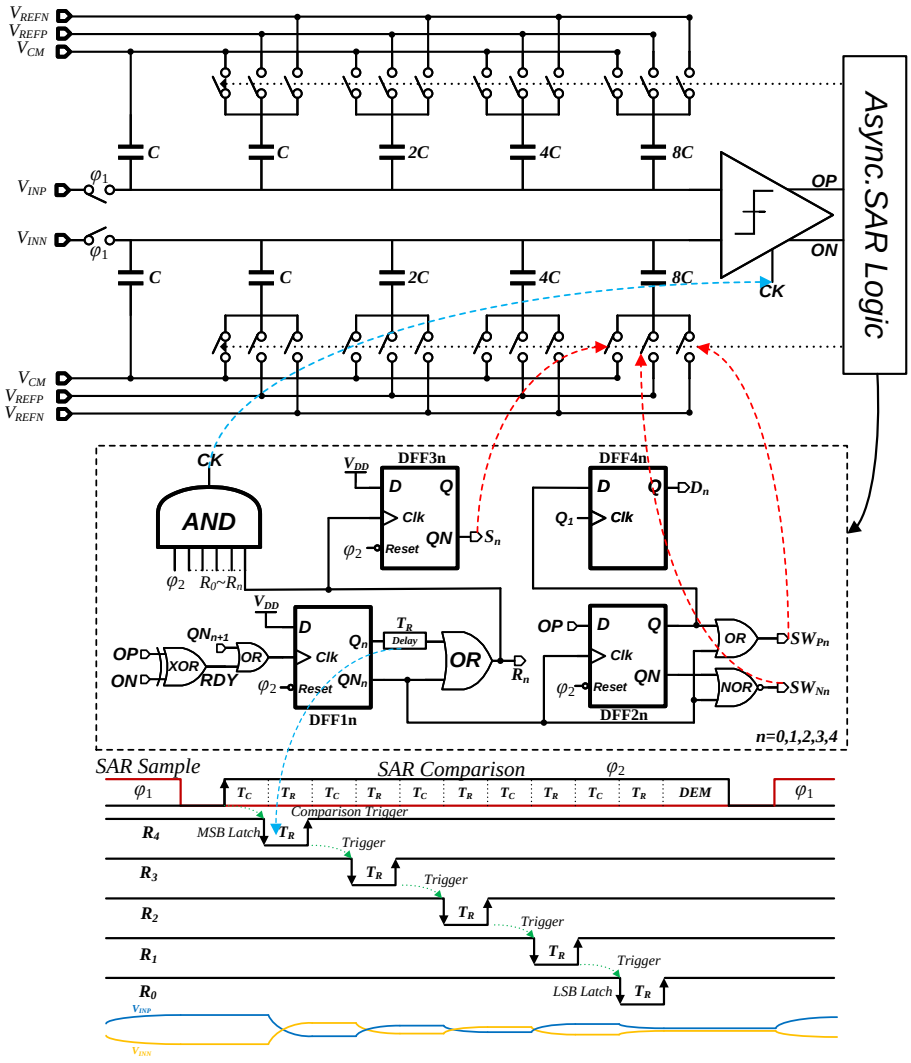


Figure 11. Schematic of 5-bit asynchronous SAR ADC and asynchronous logic, timing diagram.

3.3. Feedforward Adder Embedded 2-Bit SAR Quantizer

Figure 12 shows the two operating modes of the 2-bit asynchronous SAR quantizer half equivalent circuit with embedded adder. In the sampling mode, the bottom plate of the sampling capacitor is connected to the input signals of V_{IN1} and V_{IN2}, respectively, and the top plate is connected to the V_{CM1} signal, as shown in Figure 12a, then the total power stored on the capacitor q_1 can be expressed as:

$$q_1 = 2C(V_{IN1} - V_{CM1}) + 2C(V_{IN2} - V_{CM1}) \tag{15}$$

In the summation mode shown in Figure 12b, the total capacitance between the input node V_{XP} and V_{CM1} of the comparator is 4C when the bottom plate of the sampling capacitor is connected to V_{CM}. The total charge on the capacitor q_2 is expressed as:

$$q_2 = 4C(V_{XP} - V_{CM1}) \tag{16}$$

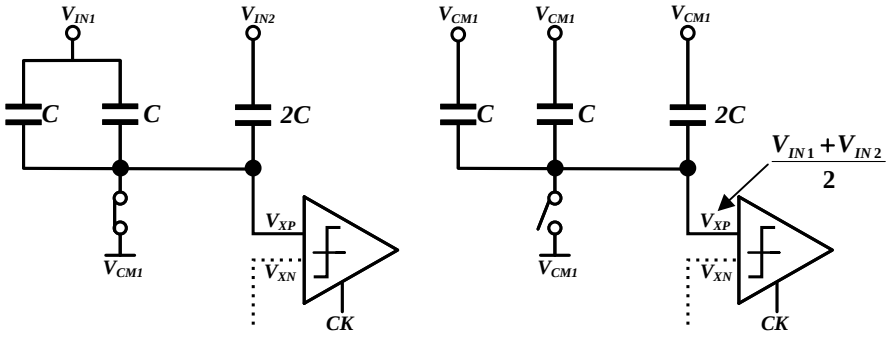
By the law of charge conservation, we have:

$$q_1 = q_2 \tag{17}$$

Thus, it can be obtained that:

$$V_{XP} = \frac{V_{IN1} + V_{IN2}}{2} \tag{18}$$

Equation (18) indicates that the summation of two input signals can be achieved by the proposed capacitor array sampling technique. After the analog input summation is completed, the SAR conversion from MSB to LSB is the same as the asynchronous logic in Section 3.2. As mentioned above, the proposed SAR ADC implements not only a 2-bit quantizer but also a feed-forward adder, which saves power and area compared to the conventional multi-bit flash quantizer.



(a) (b)

Figure 12. Equivalent circuit of SAR quantizer with embedded feedforward adder. (**a**) Sampling mode. (**b**) Summation mode.

3.4. Dynamic Element Matching and Digital Logic

The DAC capacitor array of the zoom ADC is one of its most critical modules because it directly affects the total input reference noise and total harmonic distortion (THD) of the zoom ADC, and the mismatch between the cell capacitors is one of the main factors limiting the high SNDR of the zoom adc due to the fact that it generates data-dependent nonlinear errors and is not shaped by the loop filter in the same way as quantization errors. The target linearity of the feedback DAC capacitor array of the zoom ADC is achieved by using data-weighted averaging (DWA) [26], a well-known form of DEM that suppresses the ADC in-band noise power due to mismatch by first-order noise shaping. We can achieve an initial mismatch of 0.029% by Monte Carlo simulation using a 288 fF unit capacitor made from a MIM capacitor. However, we further improve the linearity of the DAC by using a data-weighted averaging (DWA) scheme. The worst-case residual error after DWA can be estimated as:

$$E < \frac{1}{OSR} \cdot \sqrt{2^N - 1} \cdot \delta_{max} \tag{19}$$

where δ_{max} is the worst-case mismatch value [11,12], OSR = 256, N = 5, and the worst-case mismatch according to Monte Carlo simulation is 0.029%. Therefore, a theoretical error level of 6 ppm is possible for the zoom ADC. This result meets our design requirements.

The digital logic adds redundancy to the digital code K of the asynchronous SAR and combines it with the code stream bs of the quantizer output to pre-compute the 5-bit output of the zoom ADC and convert it to a 31-bit thermometer code that is presented to the DAC switch after the DWA to generate the appropriate feedback voltage. Together, these two data blocks, the digital logic, and the DWA logic constitute the main source of energy consumption in the digital back end.

4. Simulation Results

The proposed zoom ADC uses 0.35 µm standard CMOS technology approach to complete the overall circuit layout design. The supply voltage is 2.5 V. Figure 13 shows the complete layout of zoom ADC, the active area of the zoom ADC is 769 µm × 716 µm. The implementation of different size capacitors in the layout uses multiple unit capacitor cells to achieve accurate coefficient matching. The unit capacitor is a high-density capacitor on a small chip area achieved using MIM capacitors. The layout was carefully designed to keep the analog portion of the zoom ADC symmetrically aligned, while also taking care to keep sensitive analog signals away from noisy digital signal paths.

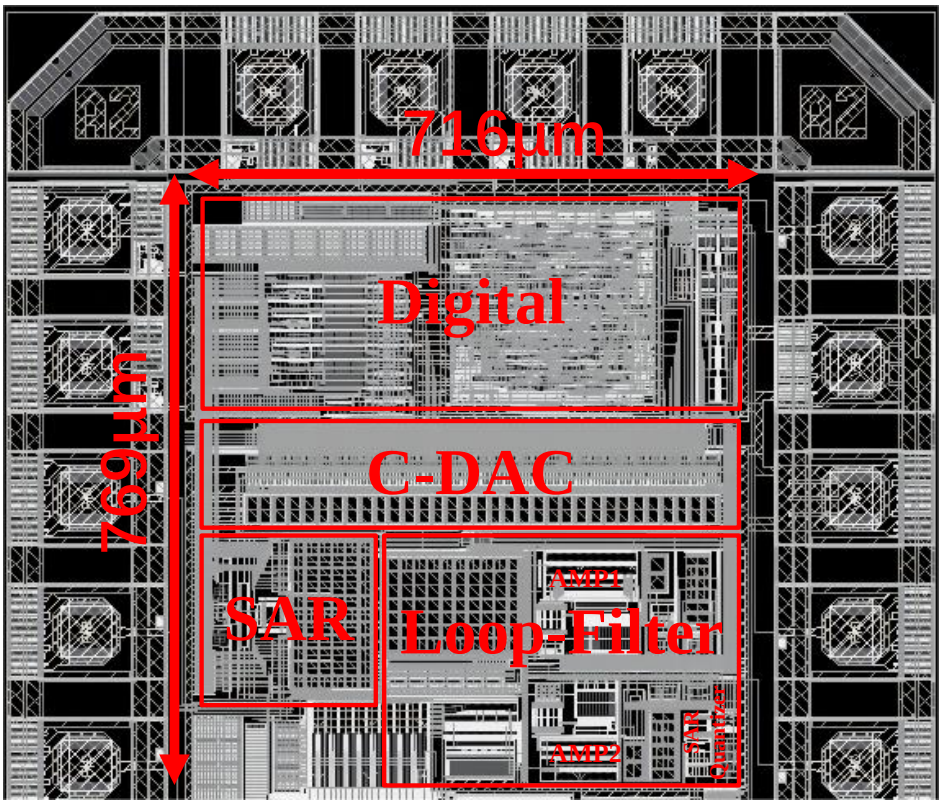


Figure 13. Layout of the proposed ADC.

In all transient simulations, the transient noise option is enabled, and the effect of circuit noise is also considered. The simulations are performed in a typical process corner with a room temperature of 27 °C. Figure 14 shows the output power spectral density of the proposed ADC at a sampling rate of 200 kHZ. A sine wave input signal of 94.6045 Hz with an amplitude of −1.1 dBFS and an oversampling rate of 256 is used. The results show that the proposed zoom ADC architecture achieves 19.83 bits of ENOB and 121.1 dB of SNDR at an input frequency of 94.6045 Hz.

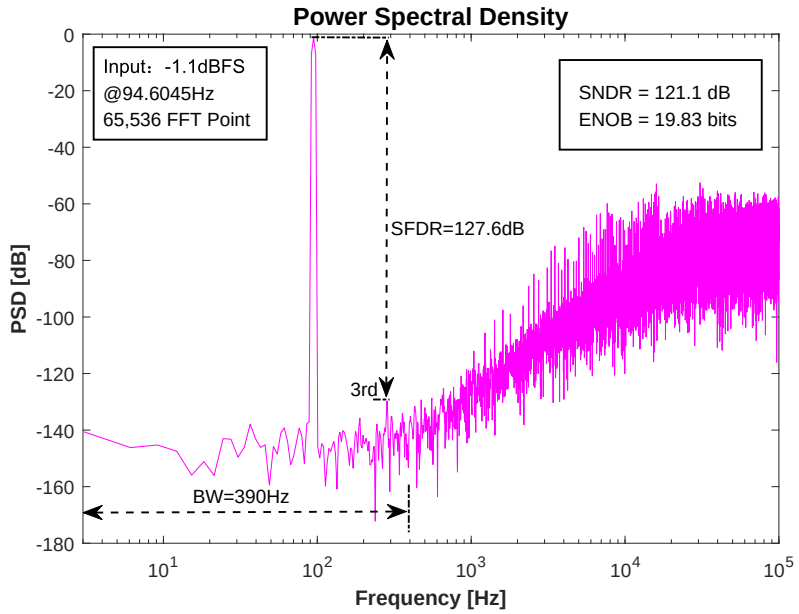


Figure 14. Simulated power spectral density (PSD) of the proposed ADC.

Figure 15 shows the SNDR versus input frequency for the simulation at a 200 kHz sampling rate. It can be seen that flat results are obtained in the bandwidth range of less than 390 Hz and the maximum SNDR variation is less than 3 dB. This frequency range basically covers the needs of most low-frequency and high-precision applications.

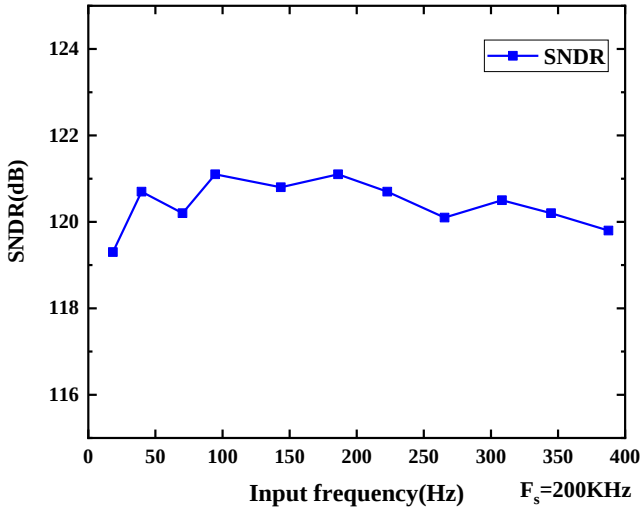


Figure 15. SNDR versus input signal frequency at −1.1 dBFS input level.

We also compared the offset of the first stage amplifier before and after chopping. As shown in Figure 16, after chopping, the offset mean value estimated over 200 Monte Carlo runs is 3.6 µV, and the standard deviation σ is 94.2 µV, demonstrating the effectiveness of chopper technology.

Table 1 summarizes the simulation results of different process corners, and variations of supply voltage and temperature (PVT) to verify the robustness of the proposed structure. It can be seen that zoom ADC obtains almost the same SNDR with different PVT characteristics.

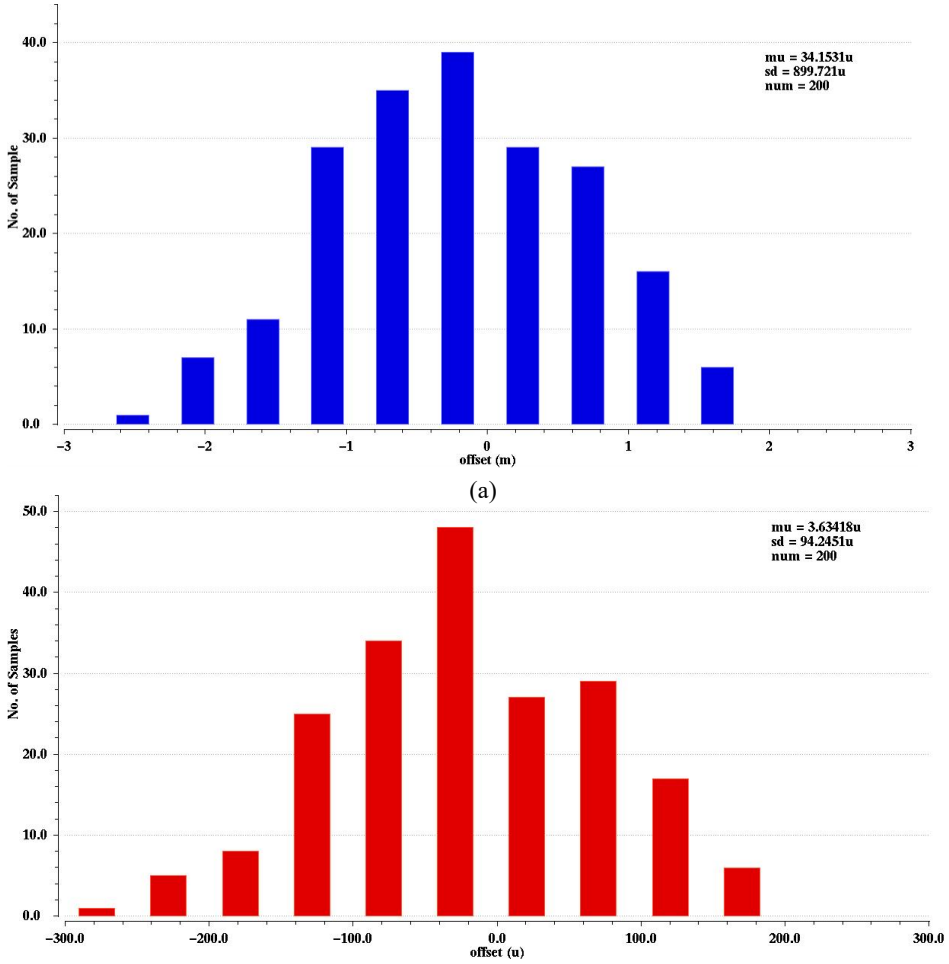


Figure 16. (**a**) Monte Carlo simulation of the first stage amplifier offset spread; (**b**) Monte Carlo simulation of the first stage amplifier offset spread after chopping.

The total power consumption is 170 µW with a 2.5 V supply. Based on simulations, the ADC power breakdown is shown in Figure 17. Among them, the dynamic amplifier consumes 70 µW of power, which can save more than 45% of power compared to the traditional static amplifier with the same structure, and the digital part (including asynchronous logic, DWA, and non-overlapping clock) consumes 62.5 µW of power, and the CDAC consumes 25 µW as a result of the noise-limited total capacitance.

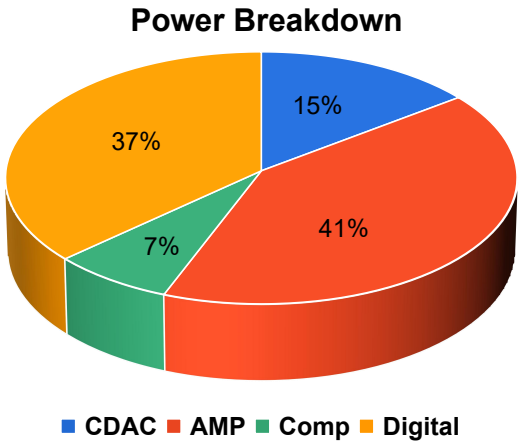


Figure 17. Power consumption breakdown.

Table 1. PVT simulation results at −1.1 dBFS input level and F_s = 200 kHz.

Parameter	SS, 85 °C, 0.9 VDD	TT, 27 °C, VDD	FF, −40 °C, 1.1 VDD
SNDR (dB)	120.4	121.1	121.6
ENOB (bit)	19.70	19.83	19.90

Based on these results, the Schreier Figure of Merit (FoM) can be calculated as:

$$FoM_{SNDR} = SNDR + 10log_{10}(\frac{BW}{Power}) = 184.7 \text{ dB} \quad (20)$$

Table 2 summarizes the performance of the proposed ADC and compares it to other state-of-the-art hybrid architecture ADCs with similar resolution (SNDR > 96 dB). Compared to previous zoom ADCs [11,12], the ADC proposed in this paper achieves higher energy efficiency (FoM_{SNDR}) at a lower oversampling rate, demonstrating the effectiveness of the technique used in this design. The ADC in [1] uses a lower oversampling rate to achieve a similar SNDR as the proposed ADC, but this comes at the cost of a higher order sigma-delta modulator and higher power consumption. The ADCs in [27,28] have lower power consumption, but they also have relatively low SNDR, and they are implemented with more advanced technology as well as lower supply voltages, resulting in significantly lower power consumption and area in the digital section.

Table 2. Performance comparison.

Parameter	This Work	[11]	[12]	[1]	[27]	[29]	[28]
Architecture	Zoom (SAR + ΔΣ + SAR)	Zoom (SAR + ΔΣ)	Zoom (SAR + ΔΣ)	Multi-bitΔΣ (ΔΣ + SAR)	IADC1 +Multi-Slope	IADC2 +Exp. Count	IADC1 +Binary Counting
Technology (nm)	350	160	160	180	180	65	180
Area (mm^2)	0.55	0.375	0.16	2.3	0.5	0.134	0.27
Supply voltage (V)	2.5	1.8	1.8	3.3	1.5	1.2	1.5
F_s (MHz)	0.2	0.0256	11.29	3.072	0.642	10.24	0.642
BW (kHz)	0.39	0.0125	20	24	1	20	1.2
Power (μW)	170	6.3	1120	20,000	34.6	550	33.2
OSR	256	1024	282	64	321	256	268
SNDR (dB)	121.1	119.8	103	120	96.8	100.8	96.6
SFDR (dB)	127.6	–	–	125.2	–	121	111
FoM_{SNDR} (dB)	184.7	182.7	175.5	180.8	171.4	176.4	172.2
Result	Simulated	Measured	Measured	Simulated	Measured	Measured	Measured

5. Conclusions

This paper presents a zoom ADC that achieves ultra-high resolution and low power consumption. The combination of a fast 5-bit asynchronous SAR coarse conversion and a two-order sigma-delta modulator fine conversion achieves good energy efficiency and high resolution. In addition, a 1-bit redundancy factor is added to correct the errors caused in the SAR ADC during coarse conversion. To reduce the quantization noise increase caused by redundancy, we use a 2-bit SAR quantizer with an embedded passive feedforward adder in the modulator quantizer section instead of an active adder and quantizer to fully utilize the DAC level and reduce the quantization noise. An integrator circuit using a high-gain dynamic amplifier is proposed to extend the dynamic range of the modulator to achieve higher SNDR, and the periodic working of the dynamic amplifier further improves the

energy efficiency of the ADC. Simulation results show that the proposed architecture is feasible to convert low bandwidth signals with high energy efficiency and high resolution.

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