A 125 to 143 GHz frequency-reconfigurable BiCMOS compact LNA using a single RF-MEMS switch

Julio Heredia, Miquel Ribó, *Member, IEEE*, Lluís Pradell, *Member, IEEE*, Selin Tolunay Wipf, Alexander Göritz, Matthias Wietstruck, Christian Wipf, and Mehmet Kaynak, *Member, IEEE*

***Abstract*— In this letter, a 125 to 143 GHz frequency-reconfigurable BiCMOS compact low-noise amplifier (LNA) is presented for the first time. It consists of two cascode stages and was fabricated using a 0.13-μm SiGe:C BiCMOS process which integrates RF-MEMS switches. A systematic general design procedure to obtain a balanced gain and noise figure in both frequency states is proposed. The LNA size is minimized by using only one RF-MEMS switch to select the frequency band and a multimodal three-line microstrip structure in the input matching network. The measured gain and noise figure are 18.2/16.1 dB and 7/7.7 dB at 125/143 GHz. The power consumption is 36.8 mW. Measured results are in good agreement with simulations.**

***Index Terms*—frequency-reconfigurable LNA, multimodal circuit, RF-MEMS switch.**

I. Introduction

THE SiGe BiCMOS technology is an attractive option to implement wireless systems and sensors in the millimeter-wave D-band (110–170 GHz) [1]. An advantage of this technology is its compatibility with RF-MEMS switch integration to provide system reconfiguration [2].

To optimize the receiver architecture, size, cost and power consumption in multi-band applications, frequency-reconfigurable LNAs are highly desirable. The D-band LNAs reported in this technology are not-reconfigurable [1], [3]–[7]. Only a few mm-wave LNAs are frequency-reconfigurable [8], [9], but at considerably lower frequencies (60/77 GHz in [8], and 24/79 GHz in [9]), and use two RF-MEMS switches. To reduce the size, the number of RF-MEMS switches should be minimized since, in D-band, the switch area may be comparable to that of the rest of the amplifier [2]. A further size reduction is possible by using multimodal waveguides, such as three-line-microstrip (TLM), which allow the propagation of more than one mode in the same circuit area. These additional modes increase the equivalent electrical length of the circuit and result in compact-size designs [10].

In this letter, a 125 to 143 GHz frequency-reconfigurable compact D-band BiCMOS LNA is presented. In contrast to [8], [9], it features a reduced chip area by using a single RF-MEMS switch and a multimodal TLM input matching network (IMN). A systematic general design procedure is proposed, and is validated by comparing simulation results to measurements. The selected frequencies can accommodate bands assigned to D-band fixed communications, with application to versatile point-to-point or point-to-multipoint backhaul systems [11]. To this end, a balanced gain and noise figure were also required to achieve an homogeneous LNA behavior in both frequency states.

II. LNA Design and Implementation

The proposed LNA consists of two cascode stages (Fig. 1). The inter-stage matching network (ISMN) is frequency reconfigurable and was designed to balance the power gain of each stage, G_{p1} and G_{p2} (and thus the LNA power gain G_p) in both frequency states (125/143 GHz bands), at the expense of being slightly lower than G_{pmax}. A single RF-MEMS switch selects the length of a short-circuited two-segment stub between L_6 for the 143-GHz band ("down" state) and L_6+L_9 for the 125-GHz band ("up" state). A second stub (L_5) is used to allow a shorter L_6, which adequately places the RF-MEMS switch to achieve a compact design. C_{11} was set to 30 fF so that its area allows the required RF current flow. The output matching network (line L_7 and stub L_8) synthesizes a load reflection coefficient Γ_L chosen for G_{p2} = 11.6/9.1 dB at 125/143 GHz. Γ_{L1} (Fig. 2) was synthesized, through C_{11}, L_5, L_6 and C_{10} (and L_9 at 125 GHz), to achieve G_{p1} = 11.2/9.9 dB at 125/143 GHz. The computed LNA G_p is 19.5/18.5 dB at 125/143 GHz, 2.4/2.9 dB lower than G_{pmax}. Simulated results were obtained from circuit/electromagnetic co-simulation, using manufacturer circuit models for HBTs, passives and the MEMS switch.

The IMN was designed to simultaneously attain low LNA noise figure (F) and $|\Gamma_{IN}|$, both balanced at the two frequency states. The geometrical locus in the Γ_{L1} plane of constant $|\Gamma_{IN}|$ and F (for a given Γ_S) is a circle. These circles, for $|\Gamma_{IN}|$ = –13.3/–15.4 dB and F = 5/5.4 dB at 125/143 GHz (0.3/0.1 dB

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J. Heredia and L. Pradell are with the Department of Signal Theory and Communications, Universitat Politècnica de Catalunya (UPC), 08034, Barcelona, Catalonia, Spain (e-mail: pradell@tsc.upc.edu).

M. Ribó is with the Electronics and Telecommunications Department, La Salle –Ramon Llull University (URL), Barcelona, Catalonia, Spain (email: mrp@salleurl.edu).

S. Tolunay Wipf, A. Göritz, M. Wietstruck, C. Wipf, M. Kaynak are with IHP – Leibniz-Institut für innovative Mikroelektronik, Im Technologiepark 25, 15236 Frankfurt (Oder), Germany.

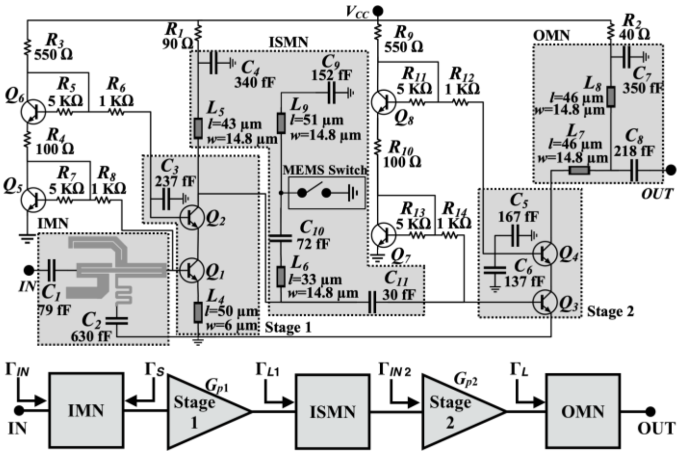

Fig. 1. Schematic and block diagram of the 125 to 143 GHz frequency-reconfigurable LNA. V_{CC} = 2.5 V. All lines L_i are microstrip.

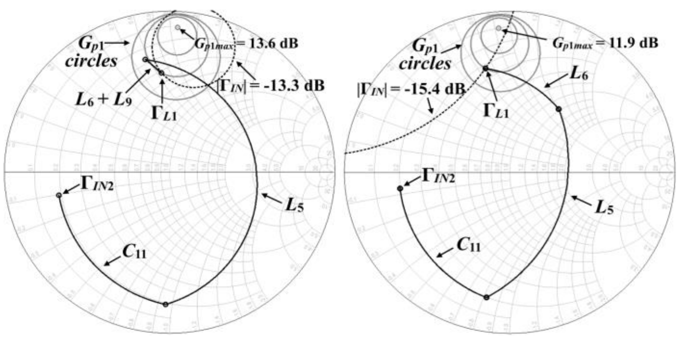

Fig. 2. ISMN Γ_{L1} reflection coefficients, circles of constant G_{p1}, and circles of constant $|\Gamma_{IN}|$ and F, for 125 GHz (left) and 143 GHz (right).

higher than F_{min}), are plotted in Fig. 2. As can be seen, they intersect the Γ_{L1} required for G_{p1}. Therefore, by using the proposed IMN and ISMN, the above requirements for the LNA $|\Gamma_{IN}|$, F and G_p are simultaneously met, and for both states. The LNA design is stable at all frequencies for both frequency states, with a simulated μ-factor $\mu > 1$ above 3 GHz. The RF-MEMS switch loss has a negligible effect on F, lower than 0.08 dB in either frequency state.

The IMN was implemented with a multimodal TLM section with two series outer-strip gaps loaded with a short-circuited, an open-circuited, and a coupled open-circuited microstrip stub (Fig. 3). The TLM simultaneously propagates three fundamental modes, *ee*, *oo* and *oe* [12] that interact at any asymmetry or transition, thus attaining a large equivalent electrical size in a compact circuit area. The *oo* and *oe* modes are excited at the loaded gaps by the *ee* mode. The dimensions in Fig. 3 were optimized to synthesize the required Γ_S by using modal equivalent circuits [13]. Compared to a standard line-plus-stub microstrip matching network, the proposed structure achieves a 72.3% area reduction (132 μm × 114 μm vs. 240 μm × 227 μm), and exhibits better simulated LNA $|S_{21}|$ (increase of 2.9/1.9 dB at 125/143 GHz) and $|S_{11}|$ (decrease of 6.8 dB at 143 GHz), with only a slight increase in F (0.4 dB in both states).

The LNA was fabricated in SG13G2 0.13-μm SiGe:C BiCMOS technology using HBTs with f_T/f_{max} of 300/500 GHz and 0.9-μm emitter length, from IHP [2]. The back-end-of-line

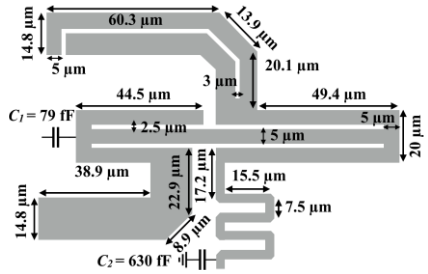

Fig. 3. IMN implemented with a TLM structure.

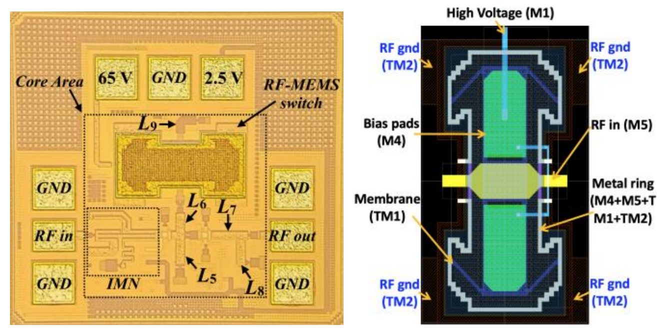

Fig. 4. Micrograph of the fabricated LNA (left) and schematic top view of the RF-MEMS switch layout in the IHP SG13G2 design kit (right). Chip area: A_{CHIP} = 536 μm × 480 μm. Core area: A_{CORE} = 327 μm × 326 μm.

(BEOL) consists of five metal layers (M1–M5) and two top-metal layers, TM1 and TM2, and integrates the RF-MEMS switch [2] with switch contact–air capacitances C_{UP}/C_{DOWN} = 9.8/211.6 fF. The LNA ground plane was fabricated on M1, the IMN and L_5, L_6, L_7, L_8 on TM2, and L_9 on TM1. Fig. 4 shows a micrograph of the fabricated LNA and a schematic view of the RF-MEMS switch, whose (external) actuation voltage is 65 V. (This voltage could be generated on-chip if stacked BEOL charge/discharge capacitors were used as a capacitive charge pump [14].) Table I lists the number of emitter fingers N_x, the emitter area, the current density and HBT area for HBTs in stages 1 and 2. They are biased using current mirrors (Q_5/Q_6 and Q_7/Q_8). Increasing N_x of Q_1 to 7 would reduce the simulated LNA F in 0.2 dB; this option was discarded since it increased the power consumption a 9.5%.

TABLE I
EMITTER DATA OF HBTS IN STAGES 1 AND 2

HBTs (Stages1 and 2)	$Q1$	$Q2$	$Q3$	$Q4$
No. of emitter fingers (N_x)	5	10	10	10
Emitter area (μm^2)	0.315	0.63	0.63	0.63
Current density (mA/μm^2)	14.70	7.39	12.76	12.76
HBT area (μm^2)	100.25	166.02	166.02	166.02

III. EXPERIMENTAL RESULTS

Figs. 5/6 compare the measured and simulated LNA S parameters and F for the 125/143 GHz states. F was measured using the Y-factor method, with a setup consisting of a noise diode, a subharmonic mixer with amplifier-multiplier chain (IF = 50 MHz), and a noise-figure analyzer. The LNA features a measured $|S_{21}|$, $|S_{11}|$, $|S_{22}|$ and F of 18.2/16.1 dB, –9.7/–12.2 dB, –5.6/–2.5 dB and 7/7.7 dB at 125/143 GHz. The power consumption is P_{DC} = 36.8 mW. The results are in good agreement with the simulations, thus validating the proposed LNA concept and design methodology. The measured $|S_{21}|$ is 1.4/0.8 dB lower than that simulated at 125/143 GHz. This is

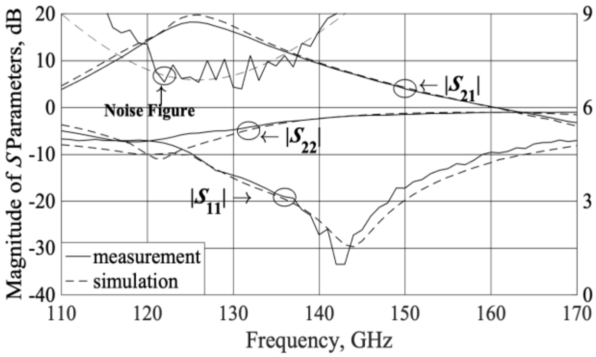

Fig. 5 Measured and simulated LNA *S*-parameters and *F* (125-GHz state).

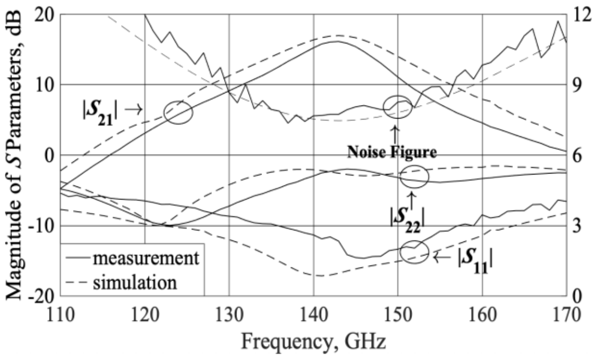

Fig. 6. Measured and simulated LNA *S*-parameters and *F* (143-GHz state).

attributed to small differences between simulated and real switch C_{UP}/C_{DOWN}. The simulated LNA input 1-dB compression point is P_{1dB} = –17.3/–15.9 dBm at 125/143 GHz.

Table II compares the fabricated-LNA performance to other reconfigurable and not-reconfigurable cascaded SiGe BiCMOS mm-wave LNAs. A *FoM* is used to evaluate the performance. The proposed LNA exhibits the smallest area *A* (both A_{CHIP} and A_{CORE}) and the highest *FoM* (save [4], with a similar *FoM*). Compared to the frequency-reconfigurable LNAs with two RF-MEMS switches [8], [9], it is more compact (because the bias and RF-MEMS circuits barely scale with frequency), and exhibits a simpler configuration and a lower P_{DC}. It is also considerably more compact than the (not-reconfigurable) LNAs in [1], [3]–[5], [7], which operate at comparable frequencies. The proposed LNA was designed to feature a well-balanced gain and noise figure in both states at the expense of lower gain and higher P_{DC}. Even so, its *F* compares well to or betters those of [1], [4], [5], which were optimized for low-noise performance.

TABLE II
COMPARISON WITH OTHER CASCADED SIGE BICMOS MM-WAVE LNAS

	Tech. (μm)	f_0 (GHz)	G ($\|S_{21}\|$) (dB)	P_{1dB} (dBm)	F (dB)	P_{DC} (mW)	A_{CHIP} / A_{CORE} (mm^2)	FoM^{**}
[1]†	0.13	158	24.1	-25.9	8.2	28	0.342/0.18^{++}	12.31/23.38
[3]	0.13	140	23.3	-33^{+}	5.5	12	0.393/0.231^{++}	8.92/15.17
[4]	0.13	130	24.3	-17.3	6.8	84	0.301/0.192^{++}	52.35/82.07
[5]	0.13	145	21		8.5	14.5	0.36/0.270^{++}	
[6]	0.09	140	30		6.2	45	0.525/0.115	
[7]	0.13	144.5	32.6	-37.6	5.1^{++}	28	1/0.6	5.05/8.42
[8]	0.25	60	20*	-18^{+}	7*	40	0.788/0.317^{++}	12.53/31.2
[8]	0.25	77	22*	-18^{+}	8*	40	0.788/0.317^{++}	15.01/37.31
[9]	0.25	24	25	-27^{+}	4.3^{+}	40	0.770/0.476^{++}	12.11/19.6
[9]	0.25	74	18	-18^{+}	8.5^{+}	40	0.770/0.476^{++}	5.34/8.63
This	**0.13**	**125**	**18.2**	**-17.3^{+}**	**7**	**36.8**	**0.257/0.107**	**32.42/78.17**
This	**0.13**	**143**	**16.1**	**-15.9^{+}**	**7.7**	**36.8**	**0.257/0.107**	**22.65/54.6**

†Cascode *Averaged $^{+}$Simulated $^{++}$Estimated ** $FoM = \dfrac{1000 \cdot G \cdot P_{1dB}}{(F-1) \cdot P_{DC} \cdot A}$

IV. CONCLUSION

A 125 to 143 GHz frequency-reconfigurable 0.13-μm SiGe:C BiCMOS D-band compact LNA has been presented for the first time. A systematic general design procedure that can be applied to any integrated technology, based on using a single switch in the IMN, has been proposed to obtain a balanced power gain and noise figure at both frequency states. The LNA size is minimized by using, in addition to a single RF-MEMS switch, a multimodal three-line-microstrip IMN. The measured gain and noise figure are 18.2/16.1 dB and 7/7.7 dB at 125/143 GHz, respectively, in very good agreement with circuit/electromagnetic co-simulations. The chip and core areas are very compact (0.257/0.107 mm^2). The experimental results validate the design procedure and its analysis.

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