A 130-dB CMRR Instrumentation Amplifier With Common-Mode Replication

Sanfeng Zhang[ID], *Graduate Student Member, IEEE*, Xiong Zhou[ID], *Member, IEEE*, Chen Gao, *Member, IEEE*, and Qiang Li[ID], *Senior Member, IEEE*

Abstract—High common-mode rejection ratio (CMRR) of an analog front end (AFE) requires high intrinsic CMRR of the front-end amplifier with high input common-mode (CM) impedance. This article presents a common-mode replication (CM-REP) technique, which replicates the input CM voltage over the front-end amplifier. By eliminating the CM current flow and its mismatch effect, CM-REP improves CMRR and input CM impedance simultaneously. Implementation considerations regarding the input CM range, on-chip, and off-chip parasitics have been discussed with practical techniques incorporated with the proposed CM-REP. Fabricated in a 0.18-μm CMOS technology, the measured instrumentation amplifier (IA) exhibits >130-dB CMRR and 50-GΩ input CM impedance at 50/60 Hz concurrently. The >110-dB CMRR is achieved with input CM up to 900 mV$_{pp}$ and >102-dB total CMRR (TCMRR) is obtained with 1-M$\Omega \parallel$ 10-nF mismatch of source impedance. The prototype consumes 1.86 μA from a 1.8-V supply and occupies an active area of 0.227 mm^2.

Index Terms—Common-mode (CM) impedance, common-mode rejection ratio (CMRR), impedance mismatch, input common-mode range, instrumentation amplifier (IA), shielding, total CMRR (TCMRR).

I. INTRODUCTION

REJECTION of common-mode (CM) interference is a fundamental requirement in precision analog design. For sensor interface applications, e.g., wearable bio-potential acquisition [1]–[6] and bridge readout [7]–[9], the analog front end (AFE) often sees large CM interference that has to be accommodated by large common-mode rejection ratio (CMRR). For example, for a 0.5-mV electrocardiograph (ECG) signal with 500-mV CM interference to the AFE, a minimum of 120-dB CMRR is required for 60-dB SNR. In practice, however, it is extremely challenging to achieve high CMRR when the imbalance of source impedance is taken into consideration [2]–[5]. In [2], with the electrode-impedance mismatch increased from 0 to 800 kΩ, the CMRR of the overall system was degraded from 102 to 42 dB. Moreover, higher CMRR is required in two-electrode acquisition systems where

much larger CM interference has to be considered [10]–[12]. The total CMRR (TCMRR) is determined by the intrinsic CMRR of the front-end instrumentation amplifier (IA) as well as the mismatch of source impedance, while the latter has to be accommodated by large input CM impedance.

Chopper-stabilization technique enhances CMRR by modulating the low-frequency errors to a chopping frequency [13]. However, it is found that chopping induces considerable input current noise due to charge injection and clock feed-through, which may dominate the overall noise contribution for high-impedance front ends [14]. Meanwhile, the input differential-mode (DM) impedance is degraded significantly by the chopping process [15], resulting in signal attenuation in high-impedance readout. Similarly, auto-zero technique mitigates the low-frequency errors at the cost of noise folding and switching induced current noise [13]. Moreover, the matching of passive components can be improved with trimming or tuning on-chip [16] or externally [3].

To mitigate the effect of source impedance mismatch, high input impedance is required for the front-end IA. The buffer-based AFE exhibits high input impedance at the cost of power and area consumed by the active buffers [17], [18]. Positive feedback technique boosts the input DM impedance effectively to prevent signal attenuation [15], [19]. However, the input CM impedance is degraded, resulting in the degradation of the TCMRR. Pre-charging technique improves both CM and DM impedance [20], [21]. However, this structure involves chopping, which induces current noise.

The traditional three-opamp implementation of IA is able to provide good CMRR with high input impedance [22]. However, it is usually power-hungry with three opamps driving resistive loads. By sharing the output stage, current-feedback IA consumes less power and the CMRR is no longer limited by the mismatch of passive components [7], [23]. The matching of the input transconductor determines the CMRR, and the mismatch between the two transconductors affects gain accuracy. The power efficiency of current balancing IA is further improved with only one transconductor [24]–[26]. It is also shown that supply regulation is able to enhance the TCMRR [5], [6], [27], while the extra power regulator is less efficient for systems with a fewer number of channels.

This work proposes a concise approach to high-CMRR design with concurrent high input CM impedance. By replicating the input CM voltage along with the DM signal, the CM current flow is eliminated, which improves both CMRR and input CM impedance. The detailed analysis on the

This article has been accepted for inclusion in a future issue of this journal. Content is final as presented, with the exception of pagination.

2   IEEE JOURNAL OF SOLID-STATE CIRCUITS
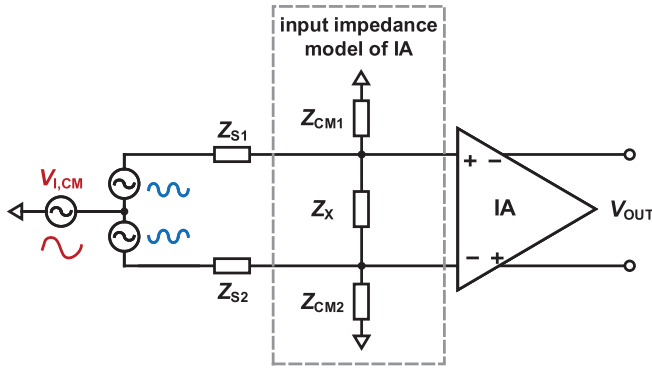

Fig. 1.   Interface model for the analysis of the TCMRR.

mechanism and design considerations of the common-mode replication (CM-REP) technique are studied. The proposed design accommodates a wide range of input CM with robustness to parasitics on-chip and off-chip. Due to the reuse of the traditional common-mode feedback (CMFB) loop, the implementation is compact. The demonstrated two-stage IA achieves >130-dB CMRR with 50-GΩ input CM impedance simultaneously, consuming only 1.86 μA from 1.8 V.

This work was first introduced in [28]. The complete study with additional details and considerations is presented here. Section II describes the principle of the proposed CM-REP technique with a discussion on the design considerations. Section III presents the circuit design of the core OTA, and Section IV discusses the overall implementation of the IA. Section V shows the measurement results. Also, this article is concluded in Section VI.

## II. CM-REP: PRINCIPLE AND CONSIDERATIONS

A. Principe of CM-REP

Fig. 1 shows an interface model for the analysis of the TCMRR, where Z_S is the source impedance with Z_{S1} and Z_{S2} representing the potentially imbalanced differential paths and Z_{CM} is the input CM impedance of the IA with Z_{CM1} and Z_{CM2} for the differential paths. Assuming that the IA has much higher input impedance compared to Z_S, the TCMRR can be expressed as

$$\frac{1}{\text{TCMRR}} = \frac{Z_S}{Z_{CM}}\sqrt{\sigma_{Z_S}^2 + \sigma_{Z_{CM}}^2} + \frac{1}{\text{CMRR}_{IA}} \qquad (1)$$

where σ_{Z_S} and $\sigma_{Z_{CM}}$ are the relative mismatch of Z_S and Z_{CM}, respectively, and CMRR_{IA} is the intrinsic CMRR of the front-end IA. Z_S and σ_{Z_S} are determined by the specific application, e.g., 1-M$\Omega \parallel$ 10-nF impedance was suggested to model the dry-contact electrodes [1]. Therefore, a large Z_{CM} is required to accommodate the mismatch of source impedance. To achieve a high TCMRR, the front-end IA has to exhibit high CMRR and high input CM impedance concurrently. It is worth mentioning that the mismatch of the input CM impedance, $\sigma_{Z_{CM}}$, contributes also to the TCMRR degradation. As an on-chip imperfection, it is normally much smaller than σ_{Z_S} and can be handled in the same way by a large Z_{CM}.
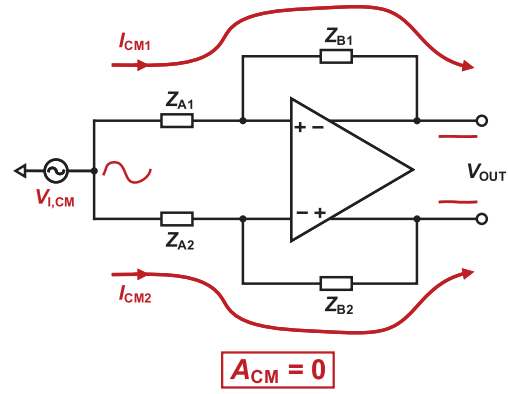
(a)
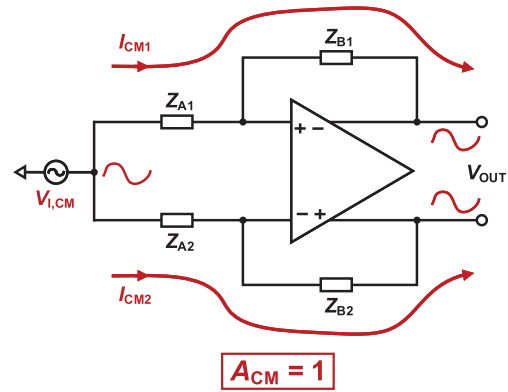
(b)

Fig. 2.   Illustration of the CM voltage and current in (a) traditional amplifier and (b) proposed amplifier with CM-REP technique.

Fig. 2 shows the idea behind the proposed CM-REP technique, where a fully differential amplifier is depicted with an ideal OTA in a feedback configuration. In the traditional design, as shown in Fig. 2(a), the output CM is stabilized at a fixed voltage by the internal CMFB. Conceptually, the output is a CM virtual ground with an ideal CMFB. The CM current flows from the input to the output through Z_A and Z_B

$$I_{CM} = \frac{V_{I,CM}}{Z_A + Z_B}. \qquad (2)$$

This CM current determines the input CM impedance

$$Z_{CM} = Z_A + Z_B. \qquad (3)$$

The mismatch in Z_A and/or Z_B results in the mismatch of the CM current, which determines the CMRR of the amplifier

$$\text{CMRR} = \frac{Z_B}{Z_A} \cdot \frac{Z_A(Z_A + Z_B)}{|Z_{A1}Z_{B2} - Z_{A2}Z_{B1}|}. \qquad (4)$$

From the current point of view, if I_{CM} can be eliminated, Z_{CM} will be enhanced to infinite. Moreover, the mismatch of I_{CM} will be eliminated as well, resulting in an infinite CMRR. As illustrated in Fig. 2(b), by replicating the input CM voltage to the output, the CM current, I_{CM}, is eliminated, improving Z_{CM} and CMRR simultaneously.
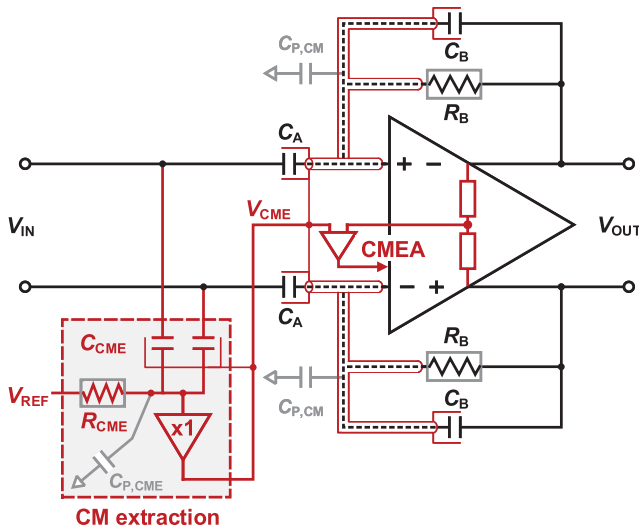
This article has been accepted for inclusion in a future issue of this journal. Content is final as presented, with the exception of pagination.

ZHANG *et al.*: 130-dB CMRR IA WITH CM-REP

3

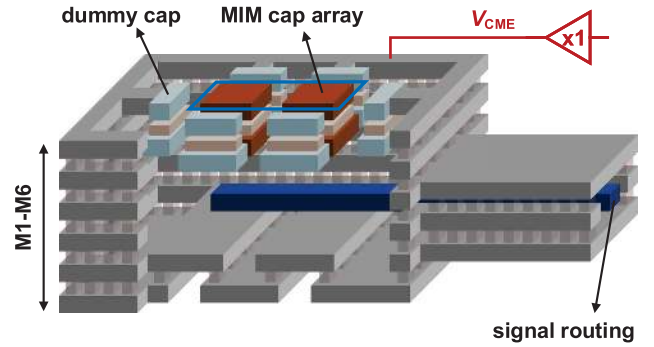Fig. 3. Implementation of CM-REP in an amplifier with capacitive feedback.

Fig. 4. 3-D view of the shielding implementation for an MIM cap with routing.

The parasitic capacitance at the input node of the OTA, $C_{P,CM}$, provides a ground path for the CM current, degrading both CMRR and Z_{CM}. Ignoring the mismatch of C_A and C_B and assuming $C_A \gg C_{P,CM}$ and $C_A \gg C_B$

$$\text{CMRR} \approx \frac{C_A}{\Delta C_{P,CM}} \tag{7}$$

$$Z_{CM} \approx \frac{1}{s C_{P,CM}}. \tag{8}$$

In general, the performance of CM-REP is limited by the parasitics at these sensitive nodes. Ideally, any CM current path through the parasitics should be prohibited. This can be achieved by shielding the parasitics with the global CM. As shown in Fig. 3, CM shielding is exploited for C_{CME}, C_A, C_B, and the routing lines at the input of the OTA. Fig. 4 shows a 3-D view of the implementation for an MIM cap array with a routing line. The cap array is placed inside a cavity constructed by metal layers, shielding both vertically and horizontally. The routing line is shielded by the adjacent metals. A unity-gain buffer is exploited to ensure sufficient driving of all shielding cavities.

Consequently, the CM performance of the amplifier will be determined by the design of the OTA, where the parasitics at internal nodes and active devices cannot be accommodated by straightforward shielding.

This intuition can be proofed theoretically by incorporating the CM gain, $A_{CM} = V_{O,CM}/V_{I,CM}$, into a general derivation

$$Z_{CM}' = \frac{Z_A + Z_B}{1 - A_{CM}} = \frac{Z_{CM}}{1 - A_{CM}} \tag{5}$$

$$\text{CMRR}' = \frac{Z_B}{Z_A} \cdot \frac{Z_A(Z_A + Z_B)}{|Z_{A1}Z_{B2} - Z_{A2}Z_{B1}|} \cdot \frac{1}{1 - A_{CM}}$$

$$= \frac{\text{CMRR}}{1 - A_{CM}}. \tag{6}$$

In the traditional amplifier, $A_{CM} = 0$, and thus, (5) becomes (3) and (6) becomes (4), while for the amplifier with replicated CM voltage, $A_{CM} = 1$, resulting in infinite Z_{CM} and CMRR.

Comparing with existing techniques that are mostly trying to improve the matching, e.g., by sophisticated trimming or tuning [16], [22], the proposed CM-REP technique provides a conceptually different approach, which allows a concurrent improvement on CMRR as well as input CM impedance.

B. Circuit Implementation and Considerations

Fig. 3 shows an implementation of the CM-REP in an amplifier with capacitive feedback, where the input CM is extracted by the two capacitors (C_{CME}) and buffered to an input of the CM error amplifier (CMEA). The other input of the CMEA is the extracted output CM of the amplifier. Therefore, the feedback loop sets the output CM in a way similar to the traditional CMFB loop with a dc reference, comparing to which, only an extra CM extraction circuit is exploited. As a result, a global CM is established, eliminating any CM current.

The accuracy of the CM-REP is primarily determined by the CM extraction, where the parasitic capacitance, $C_{P,CME}$, attenuates the CM by a factor of $2C_{CME}/(2C_{CME} + C_{P,CME})$. As a result, 1% parasitics will limit the CMRR improvement to 40 dB. Similar consideration applies at the other input of the CMEA.

III. OTA DESIGN

Fig. 5 shows the detailed schematic of the main OTA with CMEA. For higher power efficiency, the N-P complementary input is used, and the input transistors are biased in the subthreshold region [29]. As discussed in Section II, it is important to prevent any CM current flow at the sensitive nodes or, equivalently, to bias those nodes at the global CM replicated from the input. Therefore, in this design, the impedance-boosted tail current sources are exploited, and all cascode transistors are bootstrapped by the self-regulating bias (SRB).

A. Self-Shielding With SRB

Fig. 6 shows the CM equivalent circuit of a cascode stage with SRB. Intuitively, the source CM of M_1, $V_{S,CM}$, follows the input CM, $V_{G,CM}$; and $V_{D,CM}$ follows the gate CM of the

This article has been accepted for inclusion in a future issue of this journal. Content is final as presented, with the exception of pagination.

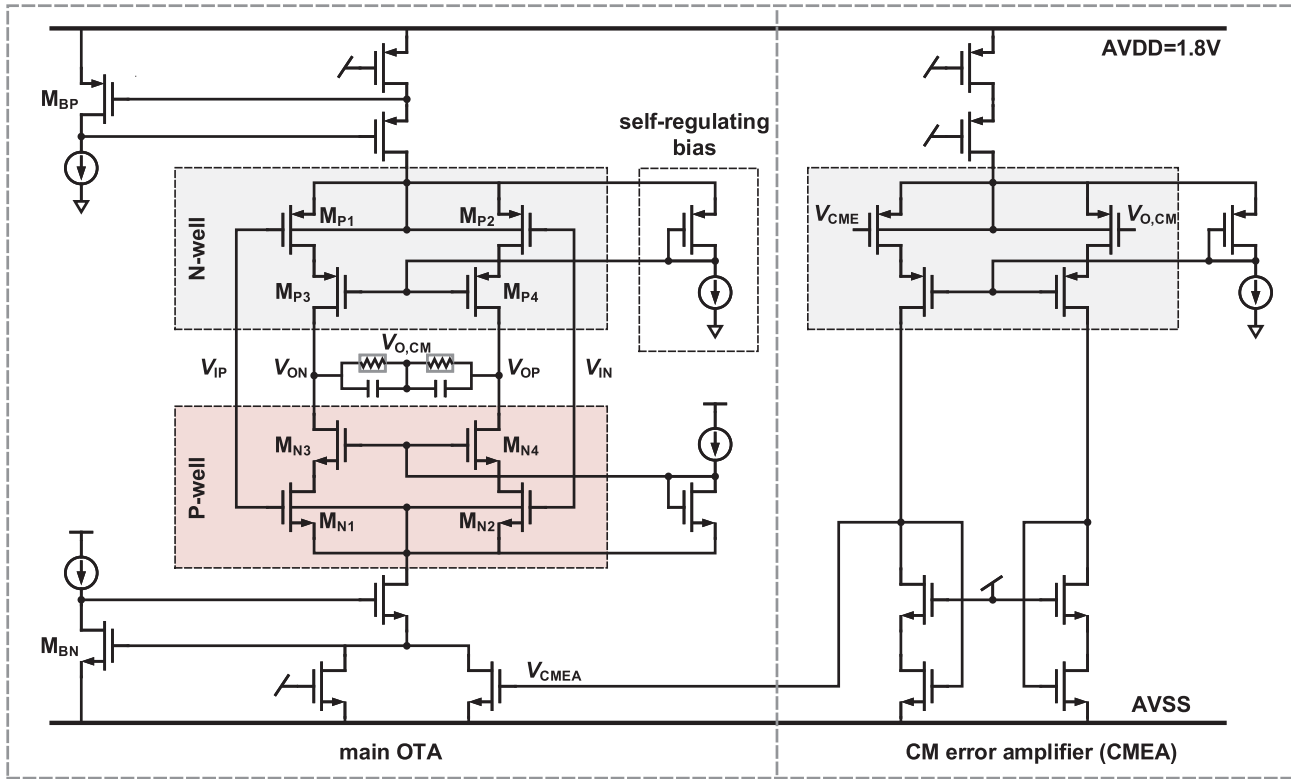4   IEEE JOURNAL OF SOLID-STATE CIRCUITS

Fig. 5. Schematic of the main OTA with CMEA.

cascade transistor M_3, which in turn follows $V_{S,CM}$ by the self-regulating process. As a result, both $V_{D,CM}$ and $V_{S,CM}$ are bootstrapped to $V_{G,CM}$, shielding the parasitics C_{GS} and C_{GD}.

The CM gain can be derived mathematically from Fig. 6, giving

$$\frac{V_{S,CM}}{V_{G,CM}} = \frac{(A_{CM}' + A_1 + A_1 A_3)R_T}{r_{o1} + r_{o3} + A_3 r_{o1} + R_T + A_1 R_t + A_1 A_3 R_T} \quad (9)$$

$$\frac{V_{D,CM}}{V_{G,CM}} = \frac{A_{CM}' r_{o1} - A_1 r_{o3} + (A_{CM}' + A_{CM}' A_1 + A_1 A_3)R_T}{r_{o1} + r_{o3} + A_3 r_{o1} + R_T + A_1 R_T + A_1 A_3 R_T} \quad (10)$$

where A_1 and A_3 are the intrinsic gain of M_1 and M_3, respectively. $A_1 = g_{m1} r_{o1}$ and $A_3 = g_{m3} r_{o3}$, where r_{o1} and r_{o3} are the drain–source impedance of M_1 and M_3, respectively. R_T is the boosted impedance of the tail current source, $R_T = (1 + A_B A_{T2})r_{o,T1} + r_{o,T2}$. Without loss of generality, A_{CM}' is the CM gain determined by the common-mode loop, which is 0 with traditional CMFB and tends to be 1 with CM-REP. Due to the large R_T, the last term dominates over both the numerators and the denominators in (9) and (10), resulting in a CM gain of 1 in both cases. Assuming 40-dB intrinsic gain of a single transistor with equal r_o, the error is less than 10^{-4}. Therefore, with SRB, all internal CM voltages of the cascade stage are bootstrapped to the input CM.

It is worth mentioning that the self-shielding effect of the SRB does not rely on the CM-REP, as suggested by (9) and (10), where the contribution of A_{CM}' is negligible. To cope with the imperfections associated with the body, e.g., body effect, parasitics, the input and cascade transistors are
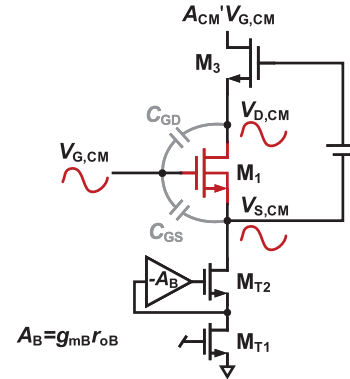

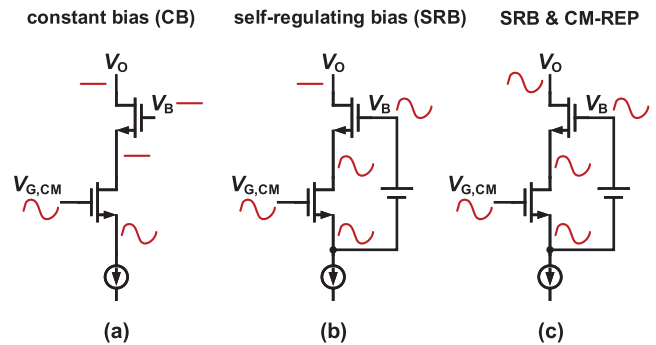Fig. 6. CM equivalent circuit of a cascade stage with SRB.

Fig. 7. CM voltage illustration of a cascade stage with (a) constant-voltage bias, (b) SRB, and (c) SRB together with CM-REP.

placed in the same well, as shown in Fig. 5. The SRB has also been exploited in the CMEA and the CM buffer.

This article has been accepted for inclusion in a future issue of this journal. Content is final as presented, with the exception of pagination.
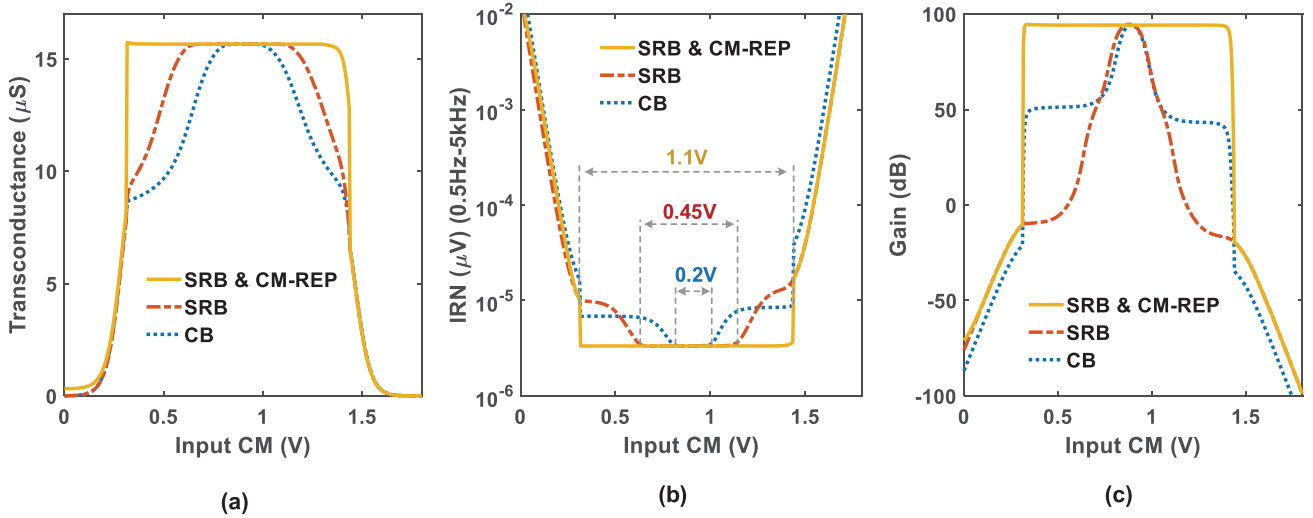
ZHANG *et al.*: 130-dB CMRR IA WITH CM-REP

5

Fig. 8.   Input CM range simulation of the main OTA with the biasing schemes described in Fig. 7 for (a) input transconductance, (b) IRN, and (c) dc gain.

B. Input CM Range of OTA

With SRB and CM-REP, a comparative study suggests an additional benefit on the enhanced input CM range. For the standard constant-voltage bias, as shown in Fig. 7(a), the gate–drain and source voltages of the cascode transistor are all fixed, and therefore, the input transistor might be pushed into the linear region with a large input CM voltage. For the SRB shown in Fig. 7(b), the gate and source voltages of the cascode transistor are following the input CM. Compared with the fixed bias, SRB guarantees the input transistor's operation, allowing a more stable input transconductance and input-referred noise (IRN) performance under input CM variations. However, since the drain voltage of the cascode transistor is still fixed by the CMFB, the cascode transistor can still be pushed into the linear region with a large input CM. Incorporating CM-REP into the SRB, as shown in Fig. 7(c), the voltages at all terminals are able to follow the input CM, guaranteeing the stable operation of both input and cascode transistors as long as the voltage headroom for the tail current source is sufficient.

Fig. 8 simulates the input CM range with the three biasing schemes described in Fig. 7. It is shown that with a traditional constant bias, the input CM range is only 0.2 V, which can be improved to 0.45 V with SRB. Significant enhancement is observed when SRB and CM-REP are exploited together, where 1.1-V input CM range is achieved. The simulation result matches very well with the above analysis.

IV. TWO-STAGE IA

A two-stage IA is implemented to demonstrate the proposed techniques, as shown in Fig. 9. The first stage employs CM-REP, offering high CMRR with high input CM impedance concurrently. The replicated CM at the output of the first stage is canceled by the chopper-stabilized second stage, which also serves for programmable gain control. For practical considerations, neutralization of ESD parasitics and shielding of PCB parasitics are implemented.

The input DM impedance is also enhanced with the positive feedback.

A. Accuracy of CM-REP

From Fig. 9, the CM gain A_{CM} from the input to the output of the first stage can be written as

$$A_{CM} = \frac{\frac{s}{\omega_{p1}}}{1 + \frac{s}{\omega_{p1}}} \cdot \frac{1}{1 + \frac{1}{A_{CMB}} + \frac{s}{\omega_{p2}}} \cdot \frac{1}{1 + \frac{1}{A_{CMFB}} + \frac{s}{\omega_{p3}}} \quad (11)$$

where $\omega_{p1} = 1/(R_{CME}C_{CME})$ and ω_{p2} and ω_{p3} are the unity-gain bandwidth of the CM buffer and the CMFB loop, respectively. A_{CMB} and A_{CMFB} are the open-loop gain of the CM buffer and CMFB loop, respectively.

The dc zero due to ω_{p1} results in a low-frequency error in A_{CM}, which degrades the accuracy of CM-REP. To mitigate this effect, a very large bias resistor, R_{CME}, is required. Fig. 10 shows the circuit implementation of R_{CME} using the switch-off resistance of the PMOS transistors. According to simulation, 2-TΩ resistance can be obtained. With this large resistance, however, even a sub-pA leakage current results in a voltage drop of hundreds of mV. In this design, a leakage-biased buffer is adopted to compensate for the leakage current through the substrate diode. The buffer consumes only 7 nA at room temperature. It has also been shown that the leakage bias is able to adjust adaptively with temperature [30].

It is worth mentioning that the CM-REP can be turned off when V_{SET} is set to high, as shown in Fig. 10, then the CMEA sees a fixed voltage V_{REF}, and in turn, the CMFB loop becomes conventional. This setup allows a measurement comparison.

A large gain of A_{CMB} and A_{CMFB} is also required for accurate replication. From (11) and (6), a 40-dB CMRR improvement is expected with 46-dB gain of A_{CMB} and A_{CMFB}, which can be easily obtained in 0.18-μm CMOS technology. In this work, the CMFB loop shown in Fig. 5 exhibits 104-dB A_{CMFB} with a unity-gain bandwidth of 220 kHz. Fig. 11 shows the schematic of the CM buffer, which exhibits 95-dB A_{CMB} and 65-kHz unity-gain bandwidth with 5-pF load. Moreover,

This article has been accepted for inclusion in a future issue of this journal. Content is final as presented, with the exception of pagination.

6
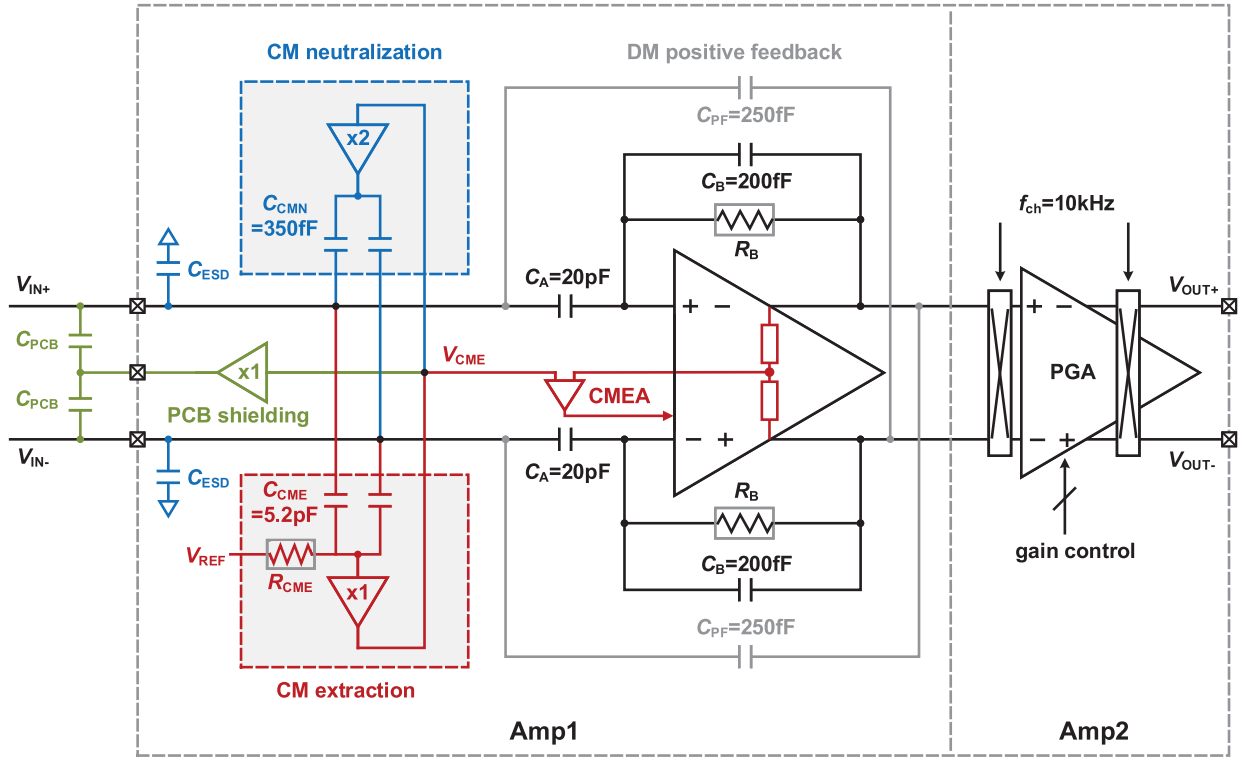
IEEE JOURNAL OF SOLID-STATE CIRCUITS

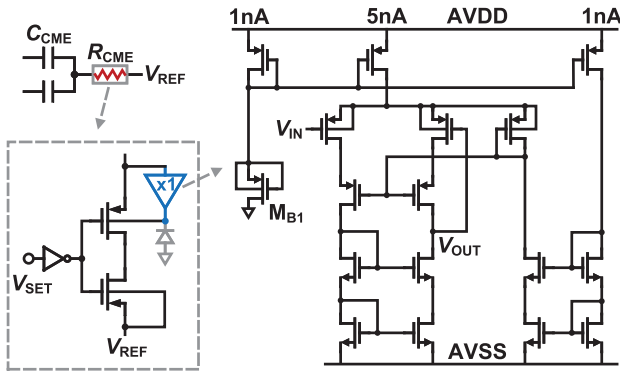Fig. 9.   Schematic of the proposed two-stage IA with CM-REP.

Fig. 10.   Implementation of large resistance with substrate leakage compensation.

the input parasitics at the CM buffer, CMEA, and the CMFB loop also affect the accuracy of CM-REP. According to (6), 40-dB CMRR improvement requires $\leq 1\%$ parasitics in the CM path, which is ensured by the shielding and SRB techniques with small-sized input transistors.

B. Pseudo-Resistors

Very large pseudo-resistors are typically employed in capacitive feedback IAs to bias the input of the OTA and provide a sufficiently small high-pass corner [31]. With globally replicated CM, however, as shown in Fig. 12(a), there is a CM current path through the substrate diode of the pseudo-resistor, degrading CMRR. In this design, the substrate is driven by the replicated CM, V_{CME}, as shown in Fig. 12(b), preventing the diode leakage from affecting the CM-REP while keeping the source-body parasitics shielded.
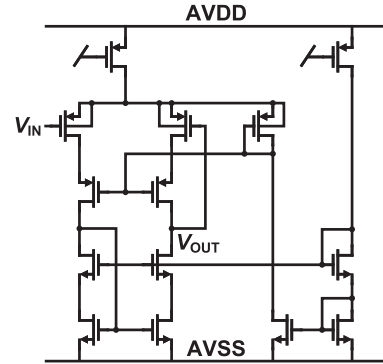

Fig. 11.   Schematic of the CM buffer.

The noise of the pseudo-resistor can be analyzed from Fig. 13. The IRN contributed by R_B can be written as

$$\overline{V_{n,R_\text{B}}^2} = \frac{8kT}{R_\text{B}} \frac{1}{(2\pi f C_\text{A})^2} = \frac{8kT R_\text{B}}{f^2} \left(\frac{f_{\text{HPF}}}{A_{\text{DM}}}\right)^2 \quad (12)$$

where f_{HPF} denotes the high-pass corner frequency and equals $1/(2\pi R_\text{B} C_\text{B})$ and A_{DM} is the mid-band gain and equals C_A/C_B. Therefore, the noise is of $1/f^2$ characteristic. The root-mean-square (RMS) noise voltage can be derived as

$$\overline{V_{n,\text{rms},R_\text{B}}} = \sqrt{\int_{f_{\text{HPF}}}^{f_{\text{BW}}} \frac{8kT R_\text{B}}{f^2} \left(\frac{f_{\text{HPF}}}{A_{\text{DM}}}\right)^2 df} \approx \frac{1}{A_{\text{DM}}} \sqrt{\frac{4kT}{\pi C_\text{B}}} \quad (13)$$

where f_{BW} is the noise bandwidth under consideration and is often much larger than f_{HPF}. It is shown that with a fixed A_{DM}, the noise contribution of the pseudo-resistor is determined by the feedback capacitor C_B, which is further limited by the gain and area considerations.
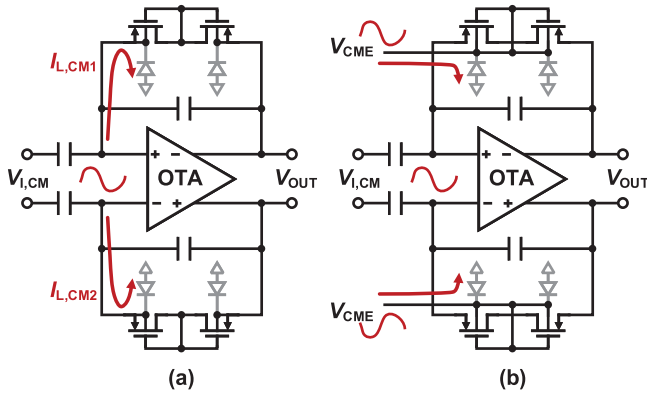
Fig. 12. Substrate diode-induced CM current leakage of (a) conventional pseudo-resistor and (b) proposed pseudo-resistor with CM driven substrate.
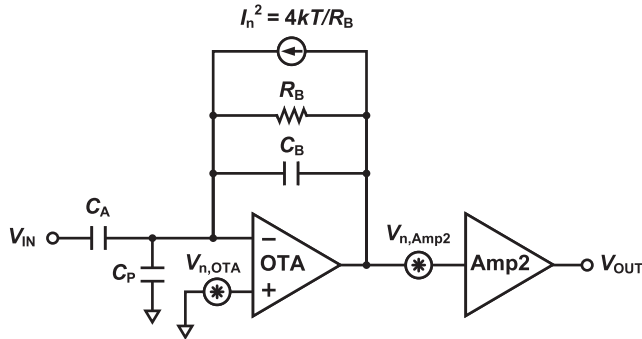

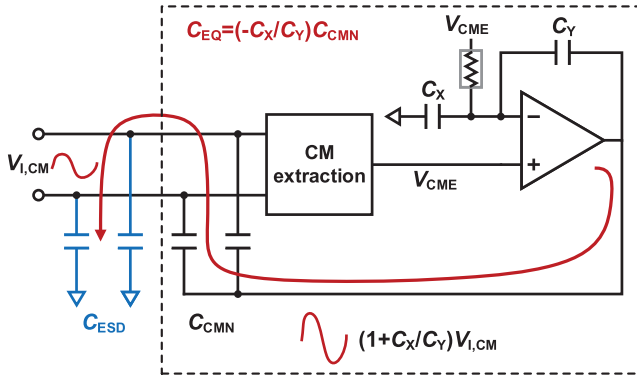Fig. 13. Single-ended circuit model for noise analysis.

Fig. 14. CM current neutralization for ESD parasitics.

With A_{DM} of 100 and C_B of 200 fF, as used in this design, the calculated RMS noise from (13) is about 1.6 μV_{rms}, dominating the low-frequency noise contribution.

C. ESD and PCB Parasitics

As the front end, the parasitic capacitance around the input path degrades the input CM impedance and consequently, as discussed with (1), the TCMRR. The parasitics are mainly contributed by the on-chip ESD and the off-chip input traces on PCB.

In this work, CM neutralization is exploited to deal with the ESD parasitics. Fig. 14 shows the detailed CM current neutralization implemented in Fig. 9. By connecting the bottom
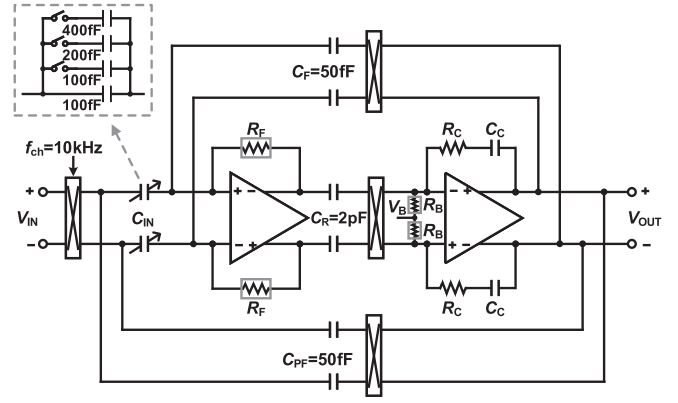

Fig. 15. Schematic of the second-stage amplifier with programmable gain control.
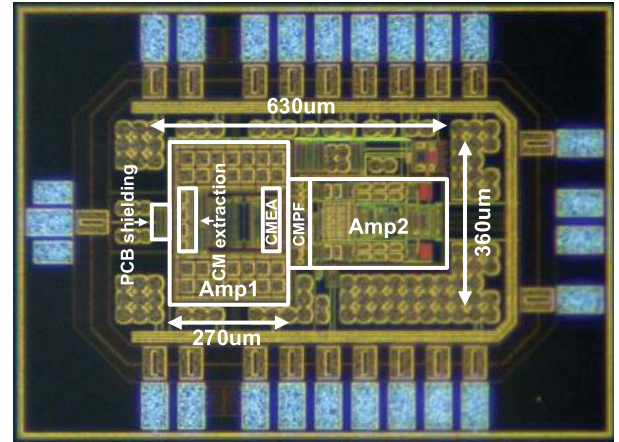

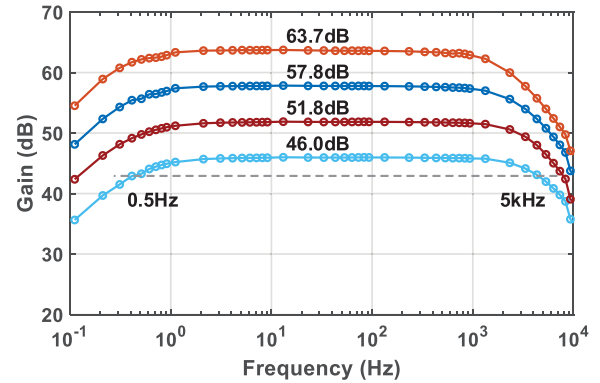Fig. 16. Die microphotograph of the fabricated amplifier.

Fig. 17. Measured gain with PGA control.

plate of C_{CMN} to the amplified V_{CME}, an equivalent negative capacitance, C_{EQ}, is generated

$$C_{EQ} = -\frac{C_X}{C_Y} C_{CMN}. \tag{14}$$

This negative capacitance compensates for the ESD parasitics from the capacitance point of view [3] or provides the C_{ESD}-induced current from the current point of view. As a result, the input loading from ESD parasitics is mitigated.

In this design, the estimated C_{ESD} is 400 fF, and C_{EQ} is set as -350 fF to avoid over compensation. Operating in CM, the neutralization loop does not result in noise degradation.
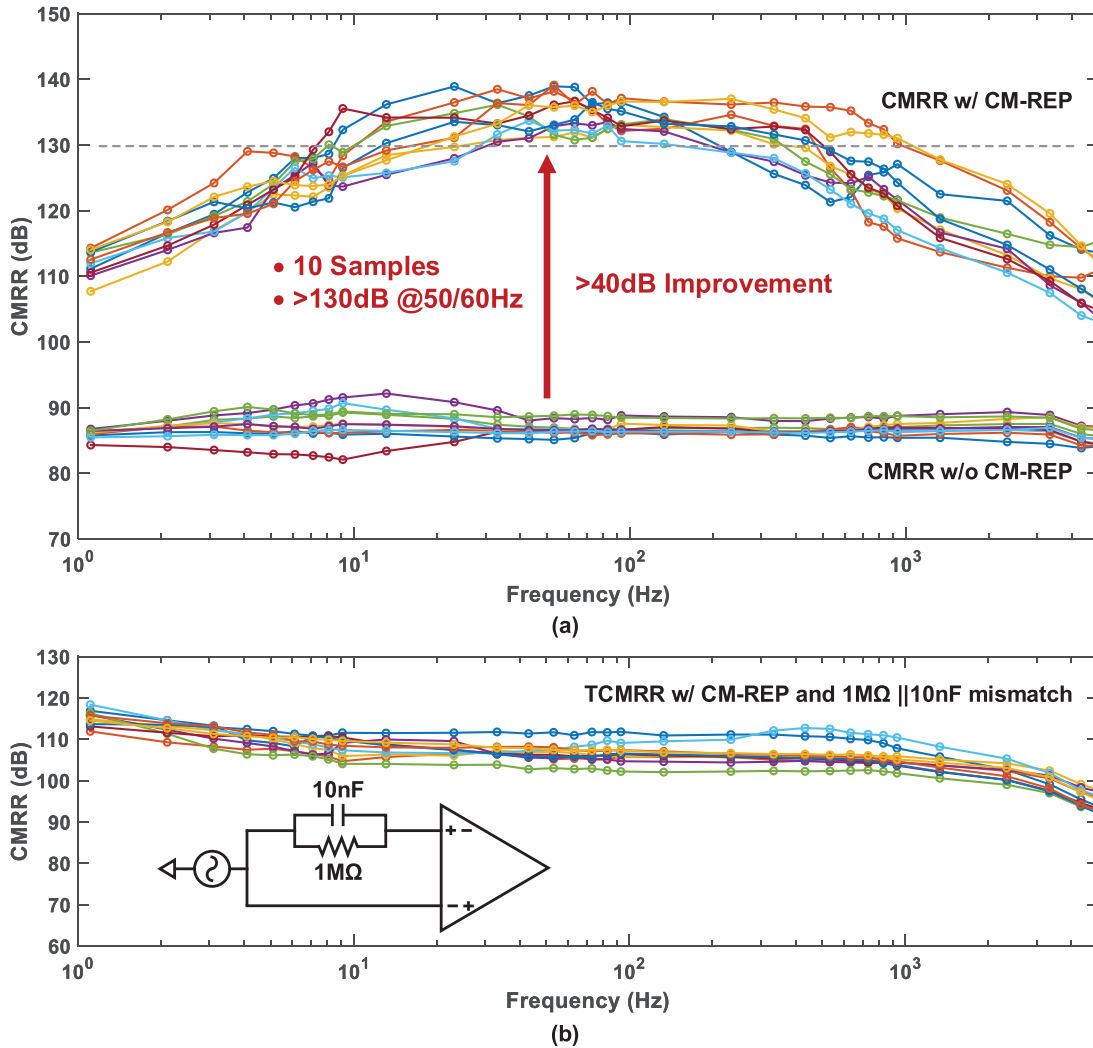
This article has been accepted for inclusion in a future issue of this journal. Content is final as presented, with the exception of pagination.

8   IEEE JOURNAL OF SOLID-STATE CIRCUITS

Fig. 18.   Measured CMRR of ten samples. (a) CMRR w/ and w/o CM-REP. (b) TCMRR with 1-MΩ ‖ 10-nF mismatch of source impedance.

Therefore, the current requirement is relaxed. With a basic five-transistor OTA, the CM neutralization consumes 160 nA in total.

Moreover, a dedicated CM buffer is employed to shield the PCB parasitics, as shown in Fig. 9, consuming 200 nA.

D. Second-Stage Amplifier

As discussed earlier, a programmable-gain amplifier (PGA) is employed as the second stage, which cancels the replicated CM from the first stage. The CMRR of the IA can be written as

$$\frac{1}{\mathrm{CMRR_{IA}}} = \frac{1}{\mathrm{CMRR_{Amp1}}} + \frac{A_{\mathrm{CM}}}{A_{\mathrm{DM}}} \cdot \frac{1}{\mathrm{CMRR_{Amp2}}}. \quad (15)$$

The CMRR of the second stage, $\mathrm{CMRR_{Amp2}}$, is scaled down by a factor of $A_{\mathrm{DM}}/A_{\mathrm{CM}}$. In this design, for a target of 140-dB $\mathrm{CMRR_{IA}}$ with 40-dB A_{DM}, $\mathrm{CMRR_{Amp2}}$ is designed to be larger than 100 dB. A chopper-stabilized capacitively coupled IA is adopted here, as shown in Fig. 15, where the chopping frequency is 10 kHz. A dc blocking capacitor, C_{R}, is placed before the output chopper to mitigate the output

ripple [20]. Meanwhile, a positive feedback capacitor, C_{PF}, is adopted to improve the input DM impedance. The gain control is implemented by configuring the input capacitance, providing 6–24-dB programmable gain with a 6-dB step.

E. Noise Analysis

From Fig. 13, the IRN of the overall IA can be calculated as

$$\overline{V_{n,\mathrm{total}}^2} = \left(\frac{C_{\mathrm{A}} + C_{\mathrm{B}} + C_{\mathrm{P}}}{C_{\mathrm{A}}}\right)^2 \overline{V_{n,\mathrm{OTA}}^2}$$

$$+ \frac{8kT}{R_{\mathrm{B}}} \frac{1}{(2\pi f C_{\mathrm{A}})^2} + \left(\frac{C_{\mathrm{B}}}{C_{\mathrm{A}}}\right)^2 \overline{V_{n,\mathrm{Amp2}}^2} \quad (16)$$

where $\overline{V_{n,\mathrm{OTA}}^2}$ and $\overline{V_{n,\mathrm{Amp2}}^2}$ are the IRN of the first-stage OTA and the second-stage amplifier, respectively, and C_{P} is the DM parasitics at the virtual ground of the OTA. With 40-dB gain at the first stage, the noise contributed by the second stage is negligible. The second term represents the noise contribution of the feedback pseudo-resistors, which is of $1/f^2$ characteristic and exists mainly at lower frequencies, as discussed in Section IV-B.

This article has been accepted for inclusion in a future issue of this journal. Content is final as presented, with the exception of pagination.

ZHANG *et al.*: 130-dB CMRR IA WITH CM-REP

9

TABLE I

CURRENT-CONSUMPTION BREAKDOWN

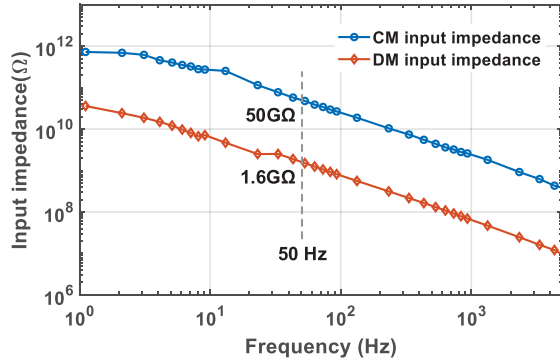| Blocks	Current (nA)
Main OTA in Amp1	860
Amp2	440
CM extraction	200
ESD CM neutralization	160
PCB shielding	200
Total	**1860**

Fig. 19. Measured input CM and DM impedance.

Fig. 20. Measured input CM impedance at 50 Hz over ten samples.

Fig. 21. Measured CMRR versus input CM amplitude at 50 Hz.
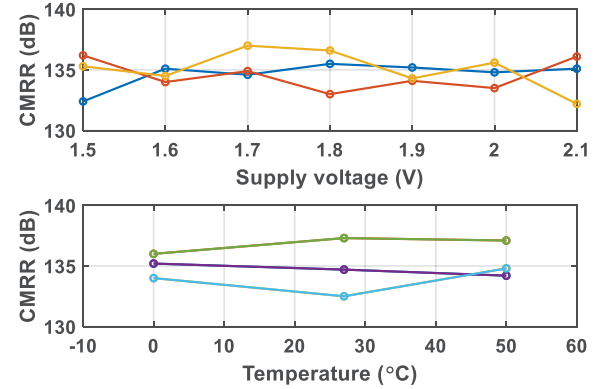
Fig. 22. Measured 50-Hz CMRR with supply and temperature variations.

The OTA contributes flicker noise as well as white noise. In this work, the flicker noise is designed smaller than the $1/f^2$ noise of the pseudo-resistors. The white noise is optimized with the current reuse and deep sub-threshold biasing of the input transistors.

V. MEASUREMENT RESULTS

The two-stage IA with the proposed CM-REP technique has been fabricated in a 0.18-μm standard CMOS technology, occupying an active area of 630×360 μm^2, as shown in Fig. 16. The IA draws 1.86 μA from a single 1.8-V supply. Table I gives the detailed breakdown of the current consumption, where the CM extraction consumes only 200 nA. This can be considered a dedicated cost for the proposed CM-REP loop since all other blocks are basically reused from the traditional CMFB loop.
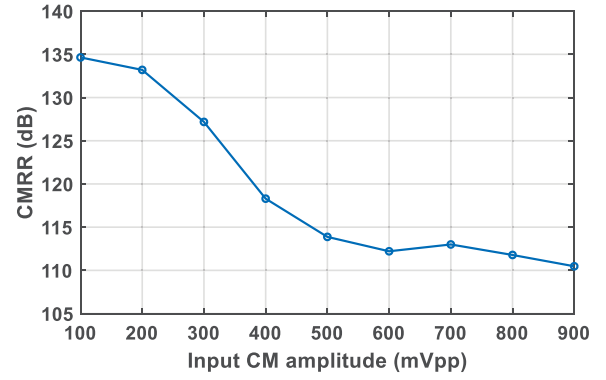
Fig. 17 shows the measured gain of the IA prototype, where the gain is configurable from 46 to 64 dB with a 6-dB step, and the bandwidth is from 0.5 to 5 kHz.

Fig. 18 shows the measured CMRR of ten samples, where the CMRR of the amplifier is given in Fig. 18(a). Without CM-REP, the CMRR is 85–90 dB at 50/60 Hz. The proposed CM-REP is able to enhance the CMRR to the level above 130 dB at 50/60 Hz, where >40-dB improvement is achieved. At lower frequencies, the CMRR enhancement is limited by the high-pass behavior of the CM extraction, as discussed in Section IV-A, whereas at higher frequencies, the finite bandwidth of the CM buffer and CMEA degrades the effect of CM-REP. 200-mV$_{PP}$ input CM amplitude is used in the measurement, unless otherwise stated.

Fig. 18(b) shows the TCMRR with 1-MΩ ∥ 10-nF mismatch of source impedance, as adopted from the impedance model of dry-contact electrodes in bio-signal acquisitions [1]. With 100% mismatch of input impedance, >102-dB TCMRR is able to be achieved across the measured ten samples. As discussed in Section II-A, this is guaranteed by the high input CM impedance.

Fig. 19 shows the measured input impedance, where 50-GΩ input CM impedance at 50 Hz is achieved due to the proposed CM-REP technique with ESD CM neutralization. The measured input DM impedance is 1.6 GΩ at 50 Hz. Fig. 20 shows the measured input CM impedance at 50 Hz over ten samples.

Fig. 21 shows the measured CMRR at 50 Hz over different input CM amplitudes. Due to the SRB exploited together with

TABLE II

PERFORMANCE SUMMARY AND COMPARISON WITH PREVIOUS WORK

Parameter	TBCAS 2012 [3]	JSSC 2015 [2]	JSSC 2017 [21]	JSSC 2018 [32]	JSSC 2018 [19]	ISSCC 2018 [27]	JSSC 2021 [16]	**This work**
Technology (nm)	180	180	40	65	180	180	180	**180**
Supply (V)	1.2	1.8	1.2	1.2	0.8	1.5	1.2	**1.8**
Current (μA)	5	58	2.33	4.9	0.285	2.15	2.3	**1.86**
Area (mm^2/channel)	3.15[a]	–	0.069	2.01[a]	0.35[a]	0.075	1.57	**0.227**
Mid-band Gain (dB)	37-50	43-63	25.7	60-94	34	39.8	40	**46-64**
IRN (μV$_{rms}$)	1.3 (0.5-100 Hz)	0.65 (0.5-100 Hz)	5.3 (200-5k Hz)	0.48 (0.5-100 Hz)	8.26 (1-400 Hz)	3.0 (10-10k Hz)	3.2 (0.5-400 Hz)	**3.14 (0.5-5kHz)**
NEF/PEF	11.24/151.69	19.15/660.1	4.4/23.23	4.09/20.1	8.43/56.85	1.69/4.28	9.4/105.3	**2.34/9.86**
THD	–	–	0.016% @80mV$_{PP}$	–	–	0.37% @2mV$_{PP}$	0.12% @5mV$_{PP}$	**0.25% @3mV$_{PP}$**
PSRR (dB)	–	–	>76	–	69	101@1k Hz	>83	**>102**
DM input impedance (Ω)	–	100M @50Hz	1.6G	1G @60Hz	50G @50Hz	–	53M @50Hz	**1.6G @50Hz**
CM input impedance (Ω)	1G[b] @87Hz	100M @50Hz	–	–	–	–	122M @50Hz	**50G @50Hz**
CMRR@50Hz (dB)	120[b]	102	86	>110	66	>110	>110	**>130**
TCMRR w/ imp. mismatch (dB)	90[b] @51kΩ‖47nF	42 @800kΩ	–	–	–	–	64 @100kΩ‖10nF	**>102 @1MΩ‖10nF**
Block under consideration	IA	IA+ PGA+ADC[c]	IA	IA+ PGA	IA+ PGA	IA+ DR^{3}E	IA	**IA+ PGA**

[a] estimated from literature   [b] with off-chip tuning   [c] with ETI monitoring

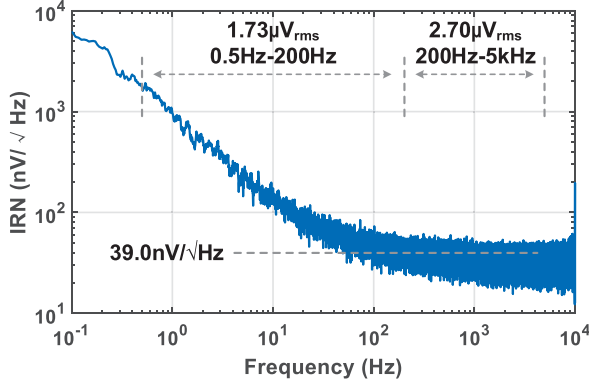Fig. 23.   Measured IRN.

Fig. 24.   Measured THD versus input DM amplitude.

CM-REP, as discussed in Section III-B, >110-dB CMRR has been achieved with input CM up to 900 mV$_{PP}$. The 20-dB degradation is mainly due to the limited CM range of the telescopic CM buffer.

The measurement has also been carried out under variations over 1.5–2.1-V supply and 0–50 °C temperature, and the measured CMRR at 50 Hz is given in Fig. 22.

Fig. 23 shows the measured IRN. The integrated noise is 1.73 μV$_{rms}$ over 0.5–200 Hz and 2.70 μV$_{rms}$ over 200–5 kHz. The total IRN over 0.5–5 kHz is 3.14 μV$_{rms}$. The thermal noise floor is 39 nV$\sqrt{\text{Hz}}$. The low-frequency noise is of $1/f^2$ characteristic, implying the dominant contribution from the feedback pseudo-resistors, as discussed in Section IV-B.

Fig. 24 shows the measured total harmonic distortion (THD) versus input DM amplitude over 0.8–3.2 mV$_{PP}$. Fig. 25 shows the measured PSRR, which is >102 dB over 0.5–5-kHz bandwidth.
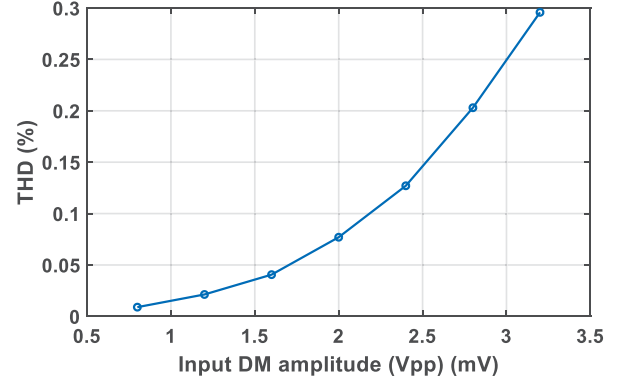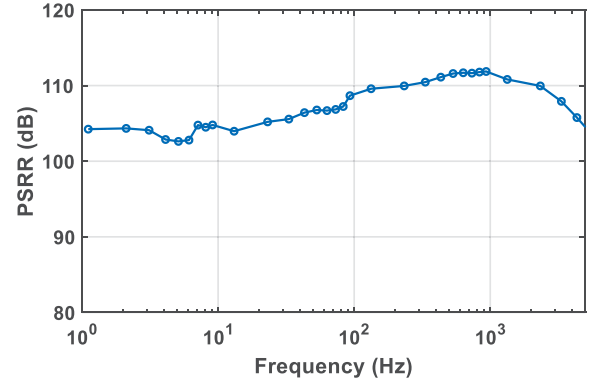

Fig. 25.   Measured PSRR.

Finally, Table II summarizes the measured performance with comparison with the state-of-the-art IAs. It is shown that the IA with the proposed CM-REP excels in terms

of the CMRR of the IA, the TCMRR with strong imbalance of source impedance, and input CM impedance simultaneously.

VI. Conclusion

In this article, the CM-REP technique was proposed and demonstrated by the fabricated IA achieving high CMRR and high input CM impedance concurrently. It was shown from the analysis that, high TCMRR of an AFE requires high CMRR of the front-end amplifier as well as high input CM impedance, which accommodates the potential imbalance of source impedance. The proposed CM-REP replicates the input CM along with the DM signal, preventing CM current flow and, consequently, the mismatch of CM current, which improves both CMRR and input CM impedance. The circuit implementation of CM-REP is concise due to the reuse of the traditional CMFB loop, where only a CM extraction is additionally exploited. Practical considerations on the imperfections, including parasitics at sensitive nodes, input CM range, ESD, and PCB parasitics, have been discussed. The fabricated IA prototypes demonstrate $>$130-dB CMRR and $>$102-dB TCMRR with 1-MΩ $\parallel$ 10-nF mismatch of source impedance and 50-GΩ input CM impedance at 50/60 Hz simultaneously. The performance excels state-of-the-art IAs.

References

[1] Y. M. Chi, T.-P. Jung, and G. Cauwenberghs, "Dry-contact and noncontact biopotential electrodes: Methodological review," *IEEE Rev. Biomed. Eng.*, vol. 3, pp. 106–119, 2010.

[2] J. Xu, B. Busze, C. Van Hoof, K. A. A. Makinwa, and R. F. Yazicioglu, "A 15-channel digital active electrode system for multi-parameter biopotential measurement," *IEEE J. Solid-State Circuits*, vol. 50, no. 9, pp. 2090–2100, Sep. 2015.

[3] N. Van Helleputte, S. Kim, H. Kim, J. P. Kim, C. Van Hoof, and R. F. Yazicioglu, "A 160 μA biopotential acquisition IC with fully integrated IA and motion artifact suppression," *IEEE Trans. Biomed. Circuits Syst.*, vol. 6, no. 6, pp. 552–561, Dec. 2012.

[4] T. Degen and H. Jäckel, "Continuous monitoring of electrode-skin impedance mismatch during bioelectric recordings," *IEEE Trans. Biomed. Eng.*, vol. 55, no. 6, pp. 1711–1715, Jun. 2008.

[5] K. A. Ng and Y. P. Xu, "A low-power, high CMRR neural amplifier system employing CMOS inverter-based OTAs with CMFB through supply rails," *IEEE J. Solid-State Circuits*, vol. 51, no. 3, pp. 724–737, Mar. 2016.

[6] M. Guermandi, E. F. Scarselli, and R. Guerrieri, "A driving right leg circuit (DgRL) for improved common mode rejection in bio-potential acquisition systems," *IEEE Trans. Biomed. Circuits Syst.*, vol. 10, no. 2, pp. 507–517, Apr. 2016.

[7] R. Wu, K. Makinwa, and J. Huijsing, "A chopper current-feedback instrumentation amplifier with a 1 mHz $1/f$ noise corner and an AC-coupled ripple reduction loop," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3232–3243, Dec. 2009.

[8] R. Wu, Y. Chae, J. H. Huijsing, and K. A. A. Makinwa, "A 20-b $\pm$40-mV range read-out IC with 50-nV offset and 0.04% gain error for bridge transducers," *IEEE J. Solid-State Circuits*, no. 9, pp. 2152–2163, Sep. 2012.

[9] H. Jiang, S. Nihtianov, and K. A. A. Makinwa, "An energy-efficient 3.7-nV/$\sqrt{\text{Hz}}$ bridge readout IC with a stable bridge offset compensation scheme," *IEEE J. Solid-State Circuits*, vol. 54, no. 3, pp. 856–864, Mar. 2019.

[10] N. Koo and S. Cho, "A 27.8μW biopotential amplifier tolerant to 30V$_{pp}$ common-mode interference for two-electrode ECG recording in 0.18μm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2019, pp. 366–368.

[11] T. Tang *et al.*, "34.6 EEG dust: A BCC-based wireless concurrent recording/transmitting concentric electrode," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2020, pp. 516–518.

[12] N. Koo, H. Kim, and S. Cho, "A 22.6μW biopotential amplifier with adaptive common-mode interference cancelation achieving total-CMRR of 104 dB and CMI tolerance of 15V$_{pp}$ in 0.18μm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2021, pp. 396–398.

[13] C. C. Enz and G. C. Temes, "Circuit techniques for reducing the effects of op-amp imperfections: Autozeroing, correlated double sampling, and chopper stabilization," *Proc. IEEE*, vol. 84, no. 11, pp. 1584–1614, Nov. 1996.

[14] J. Xu, Q. Fan, J. H. Huijsing, C. Van Hoof, R. F. Yazicioglu, and K. A. A. Makinwa, "Measurement and analysis of current noise in chopper amplifiers," *IEEE J. Solid-State Circuits*, vol. 48, no. 7, pp. 1575–1584, Jul. 2013.

[15] Q. Fan, F. Sebastiano, J. H. Huijsing, and K. A. A. Makinwa, "A 1.8 μW 60 nV/$\sqrt{\text{Hz}}$ capacitively-coupled chopper instrumentation amplifier in 65 nm CMOS for wireless sensor nodes," *IEEE J. Solid-State Circuits*, vol. 46, no. 7, pp. 1534–1543, Jul. 2011.

[16] S. Zhang, X. Zhou, C. Gao, and Q. Li, "An AC-coupled instrumentation amplifier achieving 110-dB CMRR at 50 Hz with chopped pseudoresistors and successive-approximation-based capacitor trimming," *IEEE J. Solid-State Circuits*, vol. 56, no. 1, pp. 277–286, Jan. 2021.

[17] Y. M. Chi, C. Maier, and G. Cauwenberghs, "Ultra-high input impedance, low noise integrated amplifier for noncontact biopotential sensing," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 1, no. 4, pp. 526–535, Dec. 2011.

[18] X. Zhou, Q. Li, S. Kilsgaard, F. Moradi, S. L. Kappel, and P. Kidmose, "A wearable ear-EEG recording system based on dry-contact active electrodes," in *Proc. IEEE Symp. VLSI Circuits (VLSI-Circuits)*, Jun. 2016, pp. 260–261.

[19] J. Lee, G.-H. Lee, H. Kim, and S. Cho, "An ultra-high input impedance analog front end using self-calibrated positive feedback," *IEEE J. Solid-State Circuits*, vol. 53, no. 8, pp. 2252–2262, Aug. 2018.

[20] H. Chandrakumar and D. Markovic, "A high dynamic-range neural recording chopper amplifier for simultaneous neural recording and stimulation," *IEEE J. Solid-State Circuits*, vol. 52, no. 3, pp. 645–656, Mar. 2017.

[21] H. Chandrakumar and D. Marković, "An 80-mV$_{pp}$ linear-input range, 1.6-GΩ input impedance, low-power chopper amplifier for closed-loop neural recording that is tolerant to 650-mV$_{pp}$ common-mode interference," *IEEE J. Solid-State Circuits*, vol. 52, no. 11, pp. 2811–2828, Nov. 2017.

[22] C. Kitchin and L. Counts, *A Designer's Guide to Instrumentation Amplification*, 3rd ed. Norwood, MA, USA: Analog Devices, 2006.

[23] B. J. van den Dool and J. K. Huijsing, "Indirect current feedback instrumentation amplifier with a common-mode input range that includes the negative roll," *IEEE J. Solid-State Circuits*, vol. 28, no. 7, pp. 743–749, Jul. 1993.

[24] R. F. Yazicioglu, P. Merken, R. Puers, and C. Van Hoof, "A 60 μW 60 nV/$\sqrt{\text{Hz}}$ readout front-end for portable biopotential acquisition systems," *IEEE J. Solid-State Circuits*, vol. 42, no. 5, pp. 1100–1110, May 2007.

[25] R. F. Yazicioglu, S. Kim, T. Torfs, H. Kim, and C. Van Hoof, "A 30 μW analog signal processor ASIC for portable biopotential signal monitoring," *IEEE J. Solid-State Circuits*, vol. 46, no. 1, pp. 209–223, Jan. 2011.

[26] A. Worapishet and A. Demosthenous, "Generalized analysis of random common-mode rejection performance of CMOS current feedback instrumentation amplifiers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 9, pp. 2137–2146, Sep. 2015.

[27] S. Lee *et al.*, "A 110 dB-CMRR 100 dB-PSRR multi-channel neural-recording amplifier system using differentially regulated rejection ratio enhancement in 0.18 μm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2018, pp. 472–474.

[28] S. Zhang, C. Gao, X. Zhou, and Q. Li, "23.7 A 130 dB CMRR instrumentation amplifier with common-mode replication," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2020, pp. 356–358.

[29] L. Shen, N. Lu, and N. Sun, "A 1-V 0.25-μW inverter stacking amplifier with 1.07 noise efficiency factor," *IEEE J. Solid-State Circuits*, vol. 53, no. 3, pp. 896–905, Mar. 2018.

[30] I. Lee, D. Sylvester, and D. Blaauw, "Subthreshold voltage reference with nwell/psub diode leakage compensation for low-power high-temperature systems," in *Proc. IEEE Asian Solid-State Circuits Conf. (A-SSCC)*, Nov. 2017, pp. 265–268.

[31] R. R. Harrison and C. Charles, "A low-power low-noise CMOS amplifier for neural recording applications," *IEEE J. Solid-State Circuits*, vol. 38, no. 6, pp. 958–965, Jun. 2003.

[32] U. Ha, J. Lee, M. Kim, T. Roh, S. Choi, and H.-J. Yoo, "An EEG-NIRS multimodal SoC for accurate anesthesia depth monitoring," *IEEE J. Solid-State Circuits*, vol. 53, no. 6, pp. 1830–1843, Jun. 2018.

Chen Gao (Member, IEEE) received the B.S. and M.S. degrees in microelectronics from the University of Electronic Science and Technology of China, Chengdu, China, in 2017 and 2020, respectively.

His research interests include biomedical recording systems, low-noise amplifiers, and analog front-end circuits.

Sanfeng Zhang (Graduate Student Member, IEEE) received the B.S. degree from the School of Microelectronics and Solid-State Electronics, University of Electronic Science and Technology of China, Chengdu, China, in 2015. He is currently pursuing the Ph.D. degree with the Institute of Integrated Circuits and Systems, University of Electronic Science and Technology of China.

His current research interests include high-precision analog and mixed-signal circuits for biomedical and sensor interfaces.

Qiang Li (Senior Member, IEEE) received the B.Eng. degree in electrical engineering from the Huazhong University of Science and Technology (HUST), Wuhan, China, in 2001, and the Ph.D. degree from Nanyang Technological University (NTU), Singapore, in 2007.

He has been working on analog/RF design since 2001, with industrial and academic experiences as an Engineer, the Project Leader, and the Technical Consultant in Singapore, and an Associate Professor in Denmark. He is currently a Full Professor and the Founding Chair of the Institute of Integrated Circuits and Systems (IICS), University of Electronic Science and Technology of China (UESTC), Chengdu, China. His research interests include low-voltage and low-power analog/RF circuits, data converters, and mixed-mode circuits for biomedical and sensor interfaces.

Dr. Li serves as the Distinguished Lecturer for the IEEE Solid-State Circuits Society (SSCS) and on the Technical Program Committee of international conferences, including IEEE Custom Integrated Circuits Conference (CICC), European Solid-State Circuits Conference (ESSCIRC), and IEEE Asian Solid-State Circuits Conference (ASSCC). He was the TPC Chair of the 2018 IEEE Asia Pacific Conference on Circuits and Systems (APCCAS). He served/serves as a Guest Editor for IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I: REGULAR PAPERS (TCAS-I) and an Associate Editor for IEEE OPEN JOURNAL OF CIRCUITS AND SYSTEMS (OJCAS). He is the Founding Chair of IEEE Chengdu SSCS/CASS Joint Chapter. He was a recipient of the Young Changjiang Scholar Award in 2015, the UESTC Teaching Excellence Award in 2011, and the Service Excellence Award in 2018.
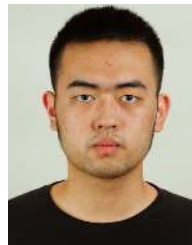
Xiong Zhou (Member, IEEE) received the B.S. degree from the School of Microelectronics and Solid-State Electronics, University of Electronic Science and Technology of China, Chengdu, China, in 2011, and the Ph.D. degree from the Department of Engineering, Aarhus University, Aarhus, Denmark, in 2016.

He has been an Associate Professor with the Institute of Integrated Circuits and Systems and the School of Electronic Science and Engineering, University of Electronic Science and Technology of China, since 2017. His current research interests include analog-to-digital converters, biopotential amplifiers and acquisition systems, and low-power analog and mixed-signal circuits.

Dr. Zhou serves as a reviewer for several international journals and conferences.