# A 131 GHz Push-push VCO in 90-nm CMOS Technology

Ping-Chen Huang, Ren-Chieh Liu, Hong-Yeh Chang, Chin-Shen Lin, Ming-Fong Lei, Huei Wang, Chia-Yi Su†, and Chia-Long Chang†

Department of Electrical Engineering and Graduate Institute of Communication Engineering, National Taiwan University, Taipei, 106, Taiwan, R. O. C.

†Taiwan Semiconductor Manufacturing Company, Hsinchu, 300, Taiwan, R. O. C.

*Abstract* — **A 131 GHz cross-coupled push-push voltage controlled oscillator (VCO) is realized in 90nm CMOS technology. It can be tuned from 129.8 to 132 GHz, with an estimated phase noise of -108.4 dBc/Hz at 10 MHz offset. The oscillator provides a push-push output power of -15.2 dBm and a fundamental output power of +0.33 dBm, under core current of 20 mA from a 1-V supply voltage. Maximum push-push and fundamental output powers are -11.4 dBm and +2.1 dBm, respectively. To the authors' knowledge, this is the highest frequency CMOS VCO ever reported.**

*Index Terms* — **CMOS, MMIC, millimeter-wave (MMW), cross-coupled, push-push, voltage-controlled oscillator (VCO), phase noise.**

## I. INTRODUCTION

There are growing demands in upper millimeter-wave (MMW) electronics for various applications. The use of frequency bands beyond 100 GHz offers advantages such as smaller antenna and chip sizes. VCO is one of the key components in MMW systems. Integrated VCOs with operating frequencies beyond 100 GHz have been reported in previous literatures [1]-[5]. They were realized using III-V compound devices [1]-[3] or SiGe HBT [4]-[5]. Recently, the trend is to advance the CMOS technology from RF into millimeter-wave range to take the advantage of low production cost and integration with baseband circuits. Many millimeter-wave VCOs were realized in CMOS technology [6]-[17]. The highest fundamental oscillation frequency ever reported was 100 GHz [16], but the output power is low since the oscillation frequency is close to $f_{max}$. To achieve higher oscillation frequency, push-push VCO are reported [8], [15], [17]. Although it has been pointed out that differential cross-coupled pair cannot achieve high frequency oscillation due to the maximum attainable oscillation frequency [17]-[18], it has the advantage of obtaining compact circuit size and the ease of design due to the inherently differential fundamental signals.

In this paper, we present a CMOS push-push VCO using a cross-coupled pair as the VCO core. The central oscillation frequency is 131 GHz and the tuning range is 1.7%. At each of the fundamental frequency differential ports, up to +2.1dBm output power can be obtained. To the authors' knowledge, this push-push VCO demonstrates the highest frequency CMOS VCO to date and provides V-band differential signals, which also have the highest output power compared with previously reported CMOS V-band VCOs. A comparison of recently reported CMOS VCOs is given in Table I.

## II. CIRCUIT DESIGN

Push-push principle can be used for MMW VCO design with the advantage of exploiting the higher device gain and passive component and varactor Q-factors available at lower frequencies [1]. Most push-push VCOs are implemented by combining anti-phase balanced structures and extracting the second harmonic signal from the virtual ground where the anti-phase fundamental signals cancel out. Also, the even mode oscillation needs to be suppressed in the design [1]-[4], [17]. In this paper, we employed a cross-coupled pair to implement the push-push VCO, similar to those reported in [8], [15], and [19].

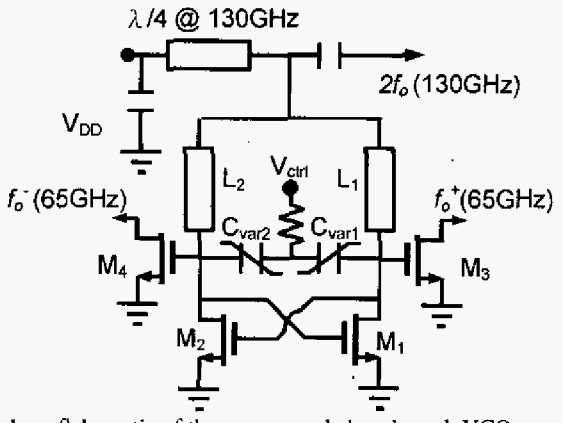


Fig. 1. Schematic of the cross-coupled push-push VCO.

The circuit schematic is shown in Fig. 1. Transistors $M_1$ and $M_2$ form the cross-coupled VCO core. The transmission lines, $L_1$ and $L_2$, and varactors $C_{var1}$ and $C_{var2}$

serve as the LC tank to determine the fundamental oscillation frequency. $M_3$ and $M_4$ are the output buffers for the differential fundamental signals. The second-harmonic signal is extracted from the center of $L_1$ and $L_2$. The supply current is fed through the $\lambda/4$-line at 131 GHz to the VCO core.

The VCO was fabricated using TSMC's 90nm CMOS technology featuring a single poly layer for the gates of the MOS and nine copper metal layers for inter-connection (1P9M). The device with gate width of 32 μm yields a $f_T$ of 142 GHz and $f_{max}$ of 160 GHz at 1-V drain bias. MIM capacitors of 1fF/mm$^2$ are available using oxide inter-metal dielectric. Two types of polysilicon resistors are provided with individual dose of ion-implantation.

Both the transistors $M_1$ and $M_2$ are NMOS of 8 fingers with total gate width of 32 μm. The negative resistance of the cross-coupled pair approaches to zero as the frequency approaches to maximum attainable oscillation frequency [18]. To ensure the oscillation, it is necessary to take into account the variation of the device parameters, i.e., $C_{gs}$, $C_{gd}$, $C_{ds}$, $R_{gs}$, etc., such that the transistors operate in a region where the cross-coupled pair generates enough negative resistance regardless of the process variation. The center fundamental oscillation frequency is designed at 65.5 GHz, where the sum of the real parts of the cross-coupled pair and the LC-tank remains negative even if the device parameters vary ±40% from the nominal values.

The fine-tuning frequency is determined by the bias of varactors from the node $V_{ctrl}$. The NMOS varactors are laid out as a multi-finger structure to maximize $Q$-factor. In order to avoid the decrease in $Q$ of the transmission line inductors due to the lossy substrate, the transmission lines are implemented as a coplanar waveguide (CPW) series with shunted asymmetric coplanar slots (ACPS) [15] rather than thin-film microstrip lines. The shunted ACPSs provide the inductances $L_1$ and $L_2$, while the CPW is used as the interconnection between the push-push output, $L_1$ and $L_2$. The CPW is designed to have characteristic impedance of 50 Ω. The line width and gap of the CPW is chosen to be 20 and 5 μm, respectively. Each of the ACPS is designed to have an inductance of 0.03 nH, with line width and gap of 5 μm and 15 μm, respectively. Figure 2 shows the chip photo, and the chip size is 0.55 mm × 0.65 mm, including RF testing pads.

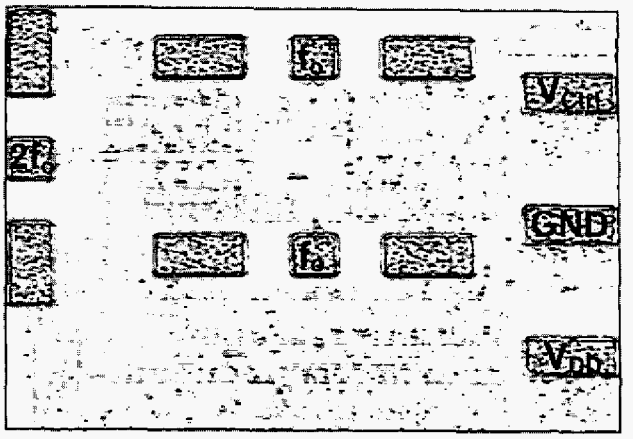

Fig. 2. Chip photo (0.55 mm × 0.65 mm).

## III. MEASUREMENT RESULTS

The chip was measured via on-wafer probing. The VCO starts to oscillate at 20-mA bias current from a 1-V supply. The fundamental and second harmonic output ports were measured by two MMW spectrum analyzer systems. A GGB W-band probe, Agilent 11970W harmonic mixer, and E4448A spectrum analyzer were used for harmonic output port. The harmonic mixer features a conversion loss of 43.5 dB at 110 GHz. For the fundamental output ports, two GGB V-band probes were used for on-wafer probing. One port was terminated with a 50-Ω load, and the other port was connected to the V-band spectrum analyzer system which consists of an Agilent 11974V pre-selection harmonic mixer and an 8565EC spectrum analyzer. Waveguide connections were used for connections between harmonic mixers and probes.

The output spectrum of the push-push port is shown in Fig. 3. Under core supply current of 20-mA from a 1-V supply voltage, the output power at the push-push port measured using a D-band power sensor is -15.2 dBm, while the output power at the fundamental port measured via the V-band spectrum analyzer system is +0.33 dBm. Each buffer consumes 8 mA from 1-V supply. The measured power on the spectrum analyzer is lower than that on the power sensor because of the excessive conversion loss of the harmonic mixer. The maximum push-push and fundamental output power are -11.4 dBm and +2.1 dBm, respectively, with 23-mA core supply current from a 1.2-V supply.

Figure 4 shows the output frequency versus the control voltage ($V_{ctrl}$), where $V_{dd}$ fixed at 1 V. The output frequency covers from 129.8 to 132 GHz, with tuning range of 1.7%. Figure 5 shows that the measured phase noise at the fundamental port is -114.4dBc/Hz at 10 MHz offset, and the phase noise at the push-push port is expected to be 6 dB higher.

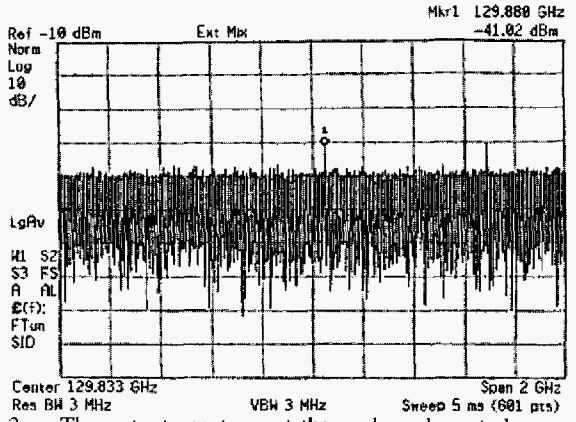


Fig. 3. The output spectrum at the push-push port shown on the W-band spectrum analyzer.

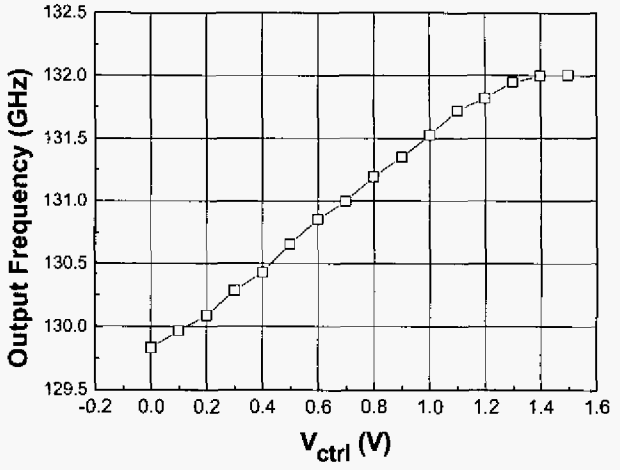


Fig. 4. Output frequency at push-push port versus the control voltage ($V_{ctrl}$).

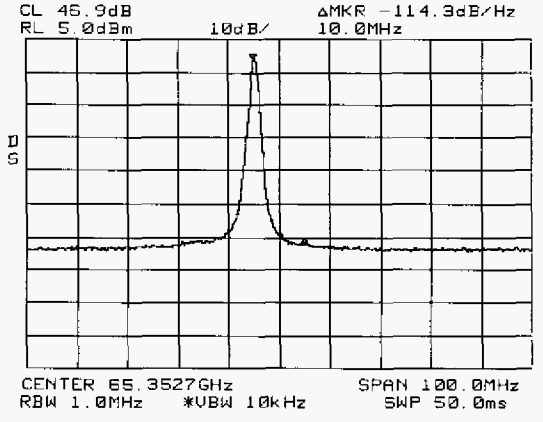


Fig. 5. Output spectrum at the fundamental port.

## IV. CONCLUSION

A 131 GHz cross-coupled push-push VCO is designed, fabricated, and tested. It can be tuned from 129.8 to 132 GHz with an estimated phase noise of -108.4 dBc/Hz at 10MHz offset. To the authors' knowledge, the oscillation frequency is the highest among CMOS VCOs. It also provides up to +2.1 dBm output power at the V-band fundamental differential ports.

## ACKNOWLEDGEMENTS

This work is supported by NTU-TSMC Joint-Development Project and National Science Council of Taiwan, R. O. C. (NSC 93-2752-E-002-002-PAE, NSC 93-2219-E-002-016, NSC 93-2213-E-002-033, and NSC 93-2219-E-002-024).

## REFERENCES

[1] K. W. Kobayashi, A. K. Oki, L. T. Tran, J. C. Cowles, A. Gutierrez-Aitken, F. Yamada, T. R. Block, and D. C. Streit, "A 108-GHz InP-HBT monolithic push–push VCO with low phase noise and wide tuning bandwidth," *IEEE Journal of Solid-State Circuits*, vol. 34, no. 9, pp. 1225 – 1232, Sep. 1999.

[2] Y. Baeyens, C. Dorschky, N. Weimann, Q. Lee, R. Kopf, G. Georgiou, J.-P. Mattia, R. Hamm, and Y.-K. Chen, "Compact InP-Based HBT VCOs with a Wide Tuning Range at W- and D-Band," *IEEE Trans. on Microwave Theory and Techniques*, vol. 48, no. 12, pp. 2403-2408, Dec. 2000.

[3] S. Kudszus, W. H. Haydl, A. Tessmann, W. Bronner, and M. Schlechtweg, "Push-push oscillators for 94GHz and 140GHz applications using standard pseudomorphic GaAs PHEMT," *IEEE MTT-S Int. Microwave Symp. Dig.*, vol. 3, pp.1571-1574, May. 2001.

[4] Y. Baeyens and Y. K. Chen, "A monolithic integrated 150GHz SiGe HBT push-push VCO with simultaneous V-band outputs," *IEEE MTT-S Int. Microwave Symp. Dig.*, vol. 2, pp. 877-880, Jun. 2003.

[5] M. Steinhauer, H. Irion, M. Schott, M. Thiel, H.-O. Ruoss, and W. Heinrich, "SiGe-based circuits for sensor applications beyond 100GHz," *IEEE MTT-S Int. Microwave Symp. Dig.*, vol. 1, pp. 223-226, Jun. 2004.

[6] C.-M. Huang, L. Shi, I. Laguado, and K. K. O, "A 25.9GHz voltage-controlled oscillator fabricated in a CMOS process," *Symp. VLSI Circuits Dig. Tech. Papers*, pp. 100-101, Jun. 2000.

[7] J.-O. Plouchart , J. Kim, N. Zamdmer, M. Sherony, Y. Tan, M. Yoon, M. Talbi, A. Ray, and L. Wagner, "A 31GHZ CML ring VCO with 5.4 ps delay in a 0.12-μm SOI CMOS technology," *IEEE European Solid-State Conf.*, pp. 357-360, Sep. 2003.

[8] C.-C. Chang, R.-C. Liu, and H. Wang, "A 40-GHz push-push VCO using 0.25-mm CMOS technology," in 2003 *Asia-Pacific Microwave Conference Proceedings*, vol. 1, pp. 73-76, 2003.

[9] N. Fong, J. Kim, J.-O. Plouchart, N. Zamdmer, D. Liu, *IEEE*, L. Wagner, C. Plett, and G. Tarr, "A low–voltage 40-GHz complementary VCO with 15% frequency tuning range in SOI CMOS technology," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 5, pp. 841-846, May 2004.

[10] A. P. van der Wel, S. L. J. Gierkink, R. C. Frye, V. Boccuzzi, and B. Nauta, "A robust 43-GHz VCO in CMOS for OC-768 SONET applications," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 7, pp. 1159-1163, Jul. 2004.

[11] H. M. Wang, "A 50 GHz VCO in 0.25 μm CMOS," *IEEE ISSCC Dig. Tech. Papers*, pp.372-373, Feb. 2001.

[12] M. Tiebout, H. D. Wohlmuth, and W. Simburger, "A 1V 51GHz fully-integrated VCO in 0.12μm CMOS," *IEEE ISSCC Dig. Tech. Papers*, pp.238-239, Feb. 2002.

[13] H. Shigematsu, T. Hirose, F. Brewer, and M. Rodwell, "CMOS circuit design for millimeter-wave applications," *IEEE RFIC Symp. Dig. Tech. Papers*, pp. 123-126, Jun. 2004.

[14] F. Ellinger, T. Morf, G. Buren, C. Kromer, G. Sialm, L. Rodoni, M. Schmatz, and H. Jackel, "60GHz VCO with wideband tuning range fabricated on VLSI SOI CMOS technology," *IEEE MTT-S Int. Microwave Symp. Dig.*, vol. 3, pp. 1329-1332, Jun. 2004.

[15] R.-C. Liu, H.-Y. Chang, C.-S. Wang, and H. Wang, "A 63GHz VCO using 0.25μm CMOS," *IEEE ISSCC Dig. Tech. Papers*, vol. 1, pp.446-447, Feb. 2004.

[16] L. M. Franca-Neto, R. E. Bishop, and B. A. Bloechel., "64GHz and 100GHz VCOs in 90nm CMOS using optimum pumping method," *IEEE ISSCC Dig. Tech. Papers*, vol.1, pp. 444-538, Feb. 2004.

[17] P.-C. Huang, M.-D. Tsai, and H. Wang, "A 114 GHz VCO in 0.13μm CMOS," *IEEE ISSCC Dig. Tech. Papers*, vol. 1, pp. 404-405, Feb. 2005.

[18] H. Veenstra, E. van der Heijden, "A 35.2-37.6GHz LC VCO in a 70/100GHz $f_T/f_{max}$ SiGe technology," *IEEE ISSCC Dig. Tech. Papers*, vol. 1, pp. 394-534, Feb. 2004.

[19] J. Jeong and Y. Kwon, "Injection-Locked push-push oscillator at 72GHz band using cross-coupled HEMTs," 2003 *European Microwave Conference*, vol. 2, pp. 587-590, Oct. 2003.

TABLE I

PERFORMANCE OF RECENTLY REPORTED CMOS VCOS

| Ref. | Process | Center Frequency (GHz) | Output Power (dBm) | Phase Noise (dBc/Hz) | Phase Noise offset (MHz) | Tuning Range (GHz) | Core Power Consumption (mW) | Chip Size($mm^2$) |
|---|---|---|---|---|---|---|---|---|
| [6] | 0.1-μm CMOS | 25.9 | -22 | -96 | 1 | 0.6 | 28.5 | 1.04 |
| [7] | 0.12-μm CMOS SOI | 31 | -16 | -75 | 1 | 3.1 | 4.5 ( per stage ) | 0.25 |
| [8] | 0.25-μm CMOS | 40 | -15 | -83 | 1 | 1.3 | 224 | N/A |
| [9] | 0.13-μm CMOS SOI | 40 | -8 | -97 | 1 | 6 | 11.3 | 0.01 |
| | | 40.7 | -8 | -89 | 1 | 6.1 | 11.3 | 0.01 |
| [10] | 0.13-μm CMOS | 43 | -24 | -90 | 1 | 1.8 | 14 | 0.06 |
| [11] | 0.25-μm CMOS | 50 | -12.5 | -100 | 1 | 1.1 | 13 | N/A |
| [12] | 0.12-μm CMOS | 51 | -30 | -85 | 1 | 0.7 | 1 | 0.4 |
| [13] | 0.18μm CMOS | 52.5 | -8 | -86 | 1 | N/A | 41 | 0.8 |
| [14] | 0.09-μm CMOS SOI | 60 | -6.8 | -89 | 1 | 8.3 | 21 | 0.1 |
| [15] | 0.25-μm CMOS | 63 | -4 | -85.3 | 1 | 1 | 118.1 | 0.32 |
| [16] | 0.09-μm CMOS | 100 | -65 | -85 | 10 | N/A | 30 | N/A |
| [17] | 0.13-μm CMOS | 114 | >-22.5 | -107.6 | 10 | 2.4 | 8.4 | 0.2 |
| This Work | 0.09-μm CMOS | 131 | -11.4 | -108.4 | 10 | 2.2 | 27.6 | 0.36 |