A 135Mbps DVB-S2 Compliant Codec Based on 64800-bit LDPC and BCH Codes (ISSCC Paper 24.3)

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ABSTRACT
A DVB-S2 compliant codec is implemented in both 130nm-8M and 90nm-7M low-leakage CMOS technologies. The system includes encoders and decoders for both Low-Density Parity Check (LDPC) codes and serially concatenated BCH codes. All requirements of the DVB-S2 standard are supported including code rates between 1/4 and 9/10, block sizes of either 16,200 bits or 64,800 bits, and four digital modulation options. The 130nm core design occupies 49.6mm2 and operates at 200MHz, while the 90nm core design occupies 15.8mm2 and operates at 300MHz.

Categories and Subject Descriptors
31.1 [**Design**]: *Best of wireless at ISSCC'05.* An example of high-complexity algorithm implemented in two different silicon technologies using an original Matlab-2-RTL methodology.

General Terms
Algorithms, Performance, Design, Experimentation, Verification.

Keywords
DVB-S2, LDPC, FEC (forward error correction).

1. INTRODUCTION
The design of the first published Broadcast Service 2nd Generation Digital Video Broadcast (DVB-S2) [1] codec with optional requirements is presented. The system includes a BCH [2] codec, a Low-Density Parity Check (LDPC) codec [3], and a channel (de)interleaver. In particular, the inclusion of the 64,800-bit LDPC decoder represents a pioneering adoption of these high-performance codes in any commercial communication standard. We demonstrate a near-Shannon limit LDPC codec in 130nm CMOS technology and a commercially viable solution in 90nm CMOS due to the reduced area. Though LDPC codes have existed since 1962, they have never been suitable for field application until recently due to their implementation complexity. This is evident because the only other published silicon implementation [4] of a LDPC decoder to-date uses a significantly smaller block code with 1024 bits.

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2. CODEC ARCHITECTURE
The LDPC decoder is comprised of 360 single-instruction multiple-data (SIMD) parallel processors that compute both check-to-variable and variable-to-check messages. Each processor uses a pipelined structure with a single arithmetic logic unit, and has access to small SRAMs operating as scratch memory. An intricate control structure prevents any duplicate computation..

3. DESIGN
3.1 Asics realized
A first test chip has been fabricated in a 1.2V, 130nm, 8M layer CMOS technology. It uses 185 memory (RAM and ROM) macros occupying a total area of 16.7mm2. Power consumed is 1.5W at an operating frequency of 200MHz with random input values. The chip consists of 8.5M transistors (2M gates).

A second test chip, built in a 1.0V, 90nm, 7M layer low-leakage CMOS technology is able to operate faster with fewer blocks of custom high-speed wide-bit memories. A total of 65 memory macros (RAM and ROM) occupy an area of 5.2 mm2. The use of a 7M process proved to be sufficient to address all routing congestion issues when coupled with a new generation routing tool. The physical implementation has been performed using a STMicroelectronics RTL-to-GDS methodology. This integrates a proprietary signal integrity checker with commercial tools that include Synopsys and Sierra Design Automation tools.

3.2 Design flow
The design was realized using a Matlab-to-RTL [6] flow for direct mapping of the datapath description into RTL. In order to respond quickly to further standard revisions, the RTL of this implementation is generic and parameterized. It is verified by formal methods against the high level description [7]. Since this verification goal far exceeds the capacity of BDD based, formal verification methods, the ACL2 theorem prover [8] is used to prove that both models are equivalent, regardless of the choice of parameters. The RTL methodology also allows the LDPC codec to support additional parity-check matrices, and different levels of parallelism, which is currently fixed at 360 by the collection of DVB-S2 matrices. This allows designers to transcend the typical difficulties associated with technology migration. Two different emulators (Cadence-Palladium and EVE-ZebuZV) were used to simulate bit-true decoder performance down to 10-7 BER. We use full scan and BIST for both designs as the test strategy. Additional self-tests use the embedded channel model and on-chip BER measurement circuit.

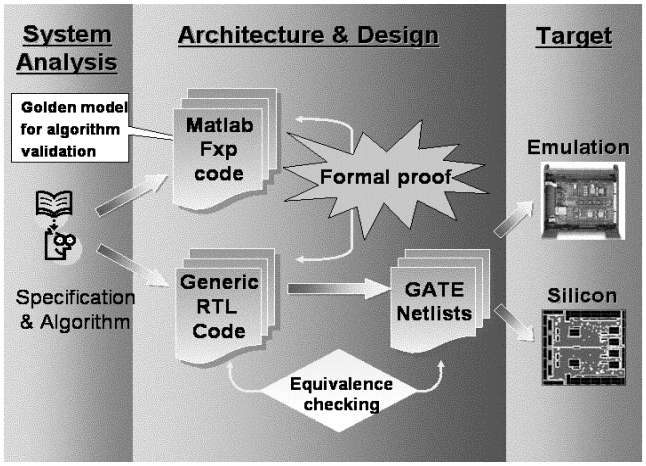

Figure 1. Matlab-to-RTL flow used for these Asics

4. CONCLUSION

Two generations of a Broadcast Service compliant DVB-S2 codec have been described. The first implementation (in 130nm) has been demonstrated to operate at 200MHz (90Mbps) with a codec area of 49.6 mm2. The second implementation (in 90nm) benefits from smaller and faster memory macros. As a result, the codec size has been reduced to 15.8 mm2 while performance has been improved by 50% to 300MHz (135Mbps). A summary of both chip implementations is provided in Table 1. Some more information is available in original ISSCC paper [9].

5. ACKNOWLEDGMENTS

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6. REFERENCES

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Design Parameter	RTL	Chip 130 nm	Chip 90 nm
LDPC Block size	Programmable	16200 / 64800 bits	
LDPC and BCH code rates	Matrix and polynomial programmable	100% DVBS2 broadcast services + few options long frames: 1/4 , 1/3 , 2/5 , 1/2 , 3/5 , 2/3 ,3/4 ,4/5 ,5/6 ,8/9 , 9/10 short frames : 2/5 , 3/5 , 2/3 , 8/9	
LDPC number of iterations	Programmable	Programmable per coderate & modulation, up to 1023	
Staggered (optional), [5]	25%, 33%, 50%	50%	
Core area		49.6 mm2	15.8 mm2
Memory capacity (Mb) / area (mm2) / number of cuts		2.921 / 16.8 / 185	2.832 / 5.2 / 65
Process technology (CMOS)		130nm 1.2V 8M	90nm 1.0V 7M HVT
Nominal clock frequency (measured on silicon)		200MHz	300MHz
Input LDPC throughput at nominal clock frequency		90 Mbps	135 Mbps
Average Power measured on silicon (nominal frequency, 25°C)		1.54W @ 1.2V	720mW to 980mW @ 1.0V (depending on matrix)
Best figure of merit with BER respecting DVBS2 specification		216pJ/iteration/Hz	67pJ/iteration/Hz
Computational energy efficiency		**46 Mops/mW**	**110 to 150 Mops/mW (depending on matrix)**

Table 1. Summary of the DVB-S2 codec