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A 14.8 dBm 20.3 dB Power Amplifier for D-band Applications in 40 nm CMOS

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***Abstract* — This paper presents a high output power, high gain, class-AB power amplifier (PA) in 40 nm CMOS technology for D-band applications. Two-way transformer-based power-combining is implemented in order to increase output power. The supply voltage of the designed PA is 1 V. The PA achieves a P_{SAT} of 14.8 dBm, small-signal gain of 20.3 dB and maximum PAE of 8.9 % at 140 GHz.**

***Index Terms* — power amplifiers, D-band, mm-Wave, high output power, CMOS, GSG pad.**

I. Introduction

With the possibilities that it offers, D-band frequency range (110 GHz-170 GHz) is very promising for wireless applications like high-speed short-range communications, high resolution imaging systems (medical, chemical and industrial sensors) and automotive radar. One of the essential blocks to develop any of these systems is the power amplifier, used as either a block before the antenna or as a driving circuit for mixers and frequency multiplier chains. However, D-band PA performance in CMOS is limited by small transistor power gain and low break-down voltage. This typically results in amplifiers with low efficiency and output power.

Conventional ways to increase output power, at lower frequency bands, are (1) cascoding, (2) increasing the size of the output transistor and (3) power combining. With cascoding, since there are two or more transistors stacked on top of each other, there is a possibility of increasing the power supply. The main drawback of this topology at D-band is the uncertainty of the bulk effect, which increases uncertainty of the whole design. Moreover, stability issues from the cascode transistor gate node can appear. Increasing the width of the output transistor indeed increases output power, but after a certain dimension the interconnect parasitics become too big, reducing the mm-wave performance. The most harmful effects are the increases of gate interconnect resistance, gate-source capacitance and gate-drain capacitance, which are lowering the power gain and efficiency. On the other hand, in the case of power combining, there is no need for too large output transistors, but the power combiner structure brings additional insertion loss. This loss decreases both amplifier gain, efficiency and output power. Clearly, there is a power limit at which combining becomes more efficient than increasing transistor size. That limit is achieved when the loss in additional interconnect becomes larger then the additional insertion loss of the power combining structure. Another drawback of the power combining approach are increased chip area and circuit complexity, but at D-band PAs are usually not the biggest area consumers. In our work, a two way parallel power combining power amplifier has been designed in order to achieve output power grater than 10 dBm at 140 GHz.

II. Circuit implementation

The schematic of the proposed amplifier is shown in Fig. 1. Each branch consists of three cascoded stages, biased in class AB. The basic unity cell is a pseudo-differential NMOS pair with neutralization capacitors. Transistor layout and dimensions are shown in the same figure. Widths of the output stage transistors are determined by the desired output power, while the input and driver stages are sized in order to improve efficiency while not affecting linearity, which is achieved by avoiding input and driver compression up to 1dB compression point of the PA stage itself. The widths of input and driver stages are chosen to be the smallest ones which fulfill this condition, reducing power consumption. Neutralization capacitors can be implemented by using transistors or MOM-like structures. The advantage of the first solution is better matching with amplifying transistors, while Q-factors of the capacitors themselves are higher in the second case. As the gain of the transistors is already quite limited in the working frequency band, the latter solution is used in this design. Since the available PDK RF model of the capacitors is tested for frequencies up to 30 GHz, custom made parallel plate capacitors, shown in the Fig. 1, have been implemented. Parallel plate structure has been chosen because it offers better accuracy while simulating with 2.5D EM simulators in comparison with the interdigitated one, since vast majority of the electric field is beamed in the vertical direction. All matching structures have been realized using stacked transformers and additional transmission lines.

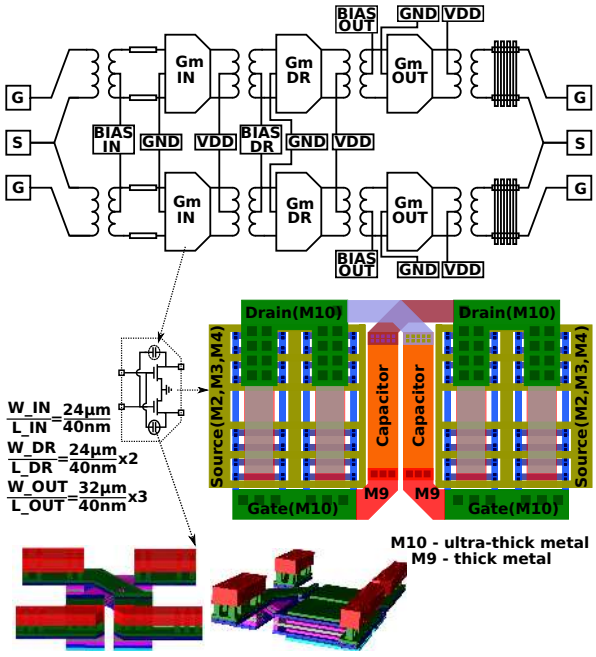

Fig. 1: Simplified schematic of the designed PA, together with single stage layout floor plan and neutralization capacitors 3D display

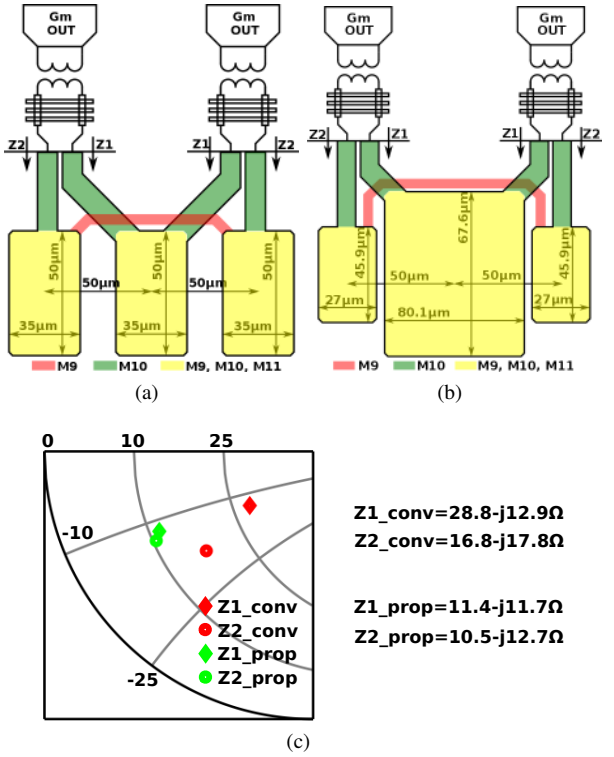

Fig. 2: GSG pad impedance analysis: (a) Conventional pad (b) Proposed pad (c) Conventional and proposed pads impedance values at 140 GHz

This way of matching ensures a compact design and easy routing of the DC connections. Stacked structure has been used for all transformers, since it improves coupling between inductors. Power supply at all stages is 1 V, which eases system level integration.

To increase the output power of the amplifier, parallel power combining is implemented. Since the GSG pads are not electrically symmetrical, the transistors of the output stages don't have the same single-ended load impedances. This imbalance causes a deviation from the ideal load impedance of the output stage and consequently a reduction of the performance. Notice that the ground of the GSG pad is isolated from the transistors ground. In order to solve the imbalance problem, the geometry of the pad has been modified. The geometry of the conventional 50 μm GSG pad, with dimensions of 50 μm $\times$ 35 μm for all three pads, is shown in Fig. 2a. Fig. 2b shows the geometry of the proposed 50 μm GSG pad, used in design, with dimensions of 80.1 μm $\times$ 67.6 μm for the signal pad and 45.9 μm $\times$ 27 μm for the ground pads. Impedances Z1 and Z2, noted in those two figures, present single-ended impedances seen by individual metal line nodes and thus subsequently seen by the drain of the transistors. They should be the same in order to make the load of the differential PA balanced. Values of those impedances at 140 GHz are shown in Fig. 2c. As we can see, unlike the conventional pad, the pad used in design is almost perfectly balanced. The key in making the pad balanced is the equalization of signal and ground pads parasitics, mainly the inductance and capacitance to the substrate. Another positive feature of the proposed pad is the lower total impedance, which makes it more suitable for matching with the PA output stage and accordingly decreases the transformation factor in the subsequent impedance transformation network. The drawback of the increased pad dimensions is the increased parasitic capacitance to the substrate and higher insertion loss. Simulated loss of the designed pad itself is 0.27 dB, while the simulated loss of the conventional pad from the Fig. 2a is 0.14 dB. However, the additional loss is, in the end, smaller due to the fact that the proposed pad results in smaller insertion loss in the impedance transformation network. Impedance of the pad is matched to the output stage, using transformers and slow-wave transmission lines, in order to achieve maximum output power. Total loss of the output combining network is 1.9 dB. The input pad has also been designed as a balanced structure, with slightly different dimensions, although it has smaller impact on the overall PA performance.

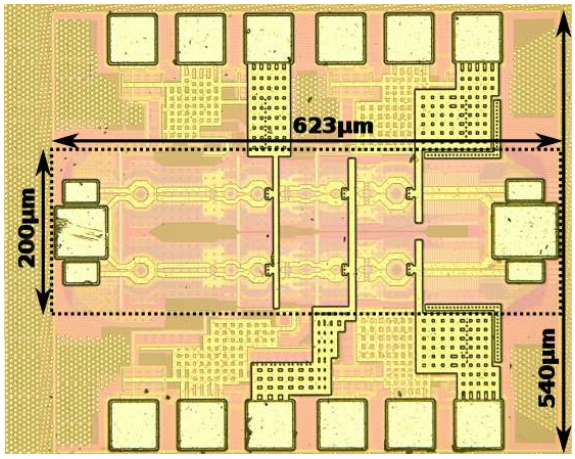

Fig. 3: Die photo of the realized PA

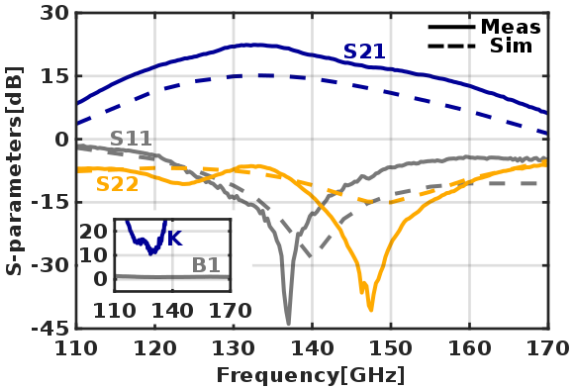

Fig. 4: Measured S-parameters and stability factors versus frequency

III. Measurements

The amplifier is fabricated in standard 40 nm CMOS technology and the die photo is shown in Fig. 3. Dimensions of the whole chip are 0.623 mm × 0.54 mm, while the area of the core is only 0.125 mm^2, including input and output pads. The supply and biasing pads are wire-bonded on an FR4 substrate and 50 μm GSG probes are used to contact input and output pads.

A R&S VNA together with the R&S D-Band extension modules are used to measure small signal parameters. The measured S-parameters together with K and B1 stability factors are shown in Fig. 4. The peak small signal gain is equal to 22.4 dB at 133 GHz, with 3-dB bandwidth of 17 GHz and 20.3 dB gain at 140 GHz. Input and output reflection coefficients are smaller then -10 dB at 140 GHz, despite to small frequency shift to lower frequencies. Reverse isolation is better than -40 dB at 140 GHz and lower than -33 dB over the entire D-band. The relatively big discrepancy between simulated and measured S-parameters is mainly caused by inaccuracies in high frequency transistor models.

For large signal measurements the Agilent PSG and the R&S extender are used as signal source. The Erickson PM5 power meter is used to sense the output signal. The

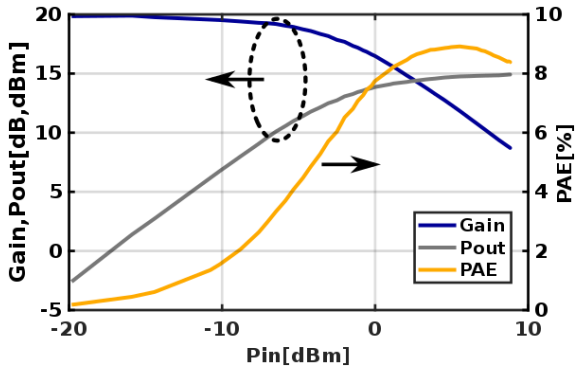

Fig. 5: Measured gain, Pout and PAE against input power at 140 GHz

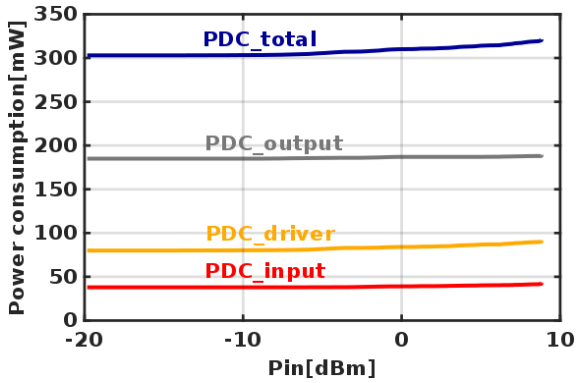

Fig. 6: Measured DC power consumption of the PA and different stages versus input power at 140 GHz

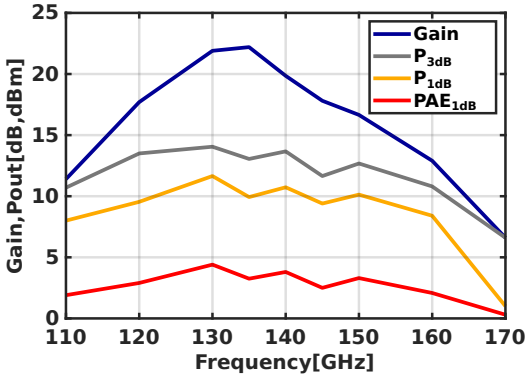

Fig. 7: Measured gain, P_{3dB}, P_{1dB} and PAE_{1dB} against frequency

TABLE I: Comparison of silicon based state-of-the-art D-band PAs

	This work	**[1]**	**[2]**	**[3]**	**[4]**	**[5]**	**[6]**
Technology	**40 nm CMOS**	65 nm CMOS	40 nm CMOS	65 nm CMOS	40 nm CMOS	120 nm SiGe	90 nm SiGe
Vdd[V]	**1**	1.2	1.1	1.1	1	3.5	1.5
Frequency[GHz]	**140**	140	133	150	160	124	116
BW[GHz]	**17**	>30	13	27	24	17.2	15
Fractional BW[%]	**12.1**	>21.4	9.8	18	15	13.9	12.9
Gain[dB]	**20.3**	15	16.8	8.2	11.6	32	15
P_{1dB}[dBm]	**10.7**	9.9	6.8	1.5	1.5	13.5	17
P_{SAT}[dBm]	**14.8**$^{\#}$	13.2$^{\#\#}$	8.6$^{\#\#}$	6.3$^{\#\#}$	4.1	17.8$^{\#\#}$	20.8$^{\#\#}$
PAE_{MAX}[%]	**8.9**	14.6	7.4	10^{+}	2.6^{+}	4.3	7.6
Area[mm^2]	**0.34*****(0.125******)**	0.38*	0.3*(0.11**)	0.41*(0.16**)	0.063**	1.92***	4.95*
DC Power[mW]	**305**$^{@}$	115.2	89.1	25.5	42	560	1520$^{@@}$
FOM$^{\%}$	**87.5**	82.8	76.6	68	63.9	98	85.9

$^{\#}$power where PAE is at maximum value $^{\#\#}$highest measured output power
$^{+}$graphically estimated
*whole chip area **core area ***whole chip area, together with doubler
$^{@}$at 1dB compression point $^{@@}$at saturation
$^{\%}$FOM=P_{SAT}[dBm]+Gain[dB]+20log(freq[GHz])+10log(PAE_{MAX}[%])

loss of the probes and interconnect waveguides is measured using the same signal source and power meter with help of the CS-5 calibration substrate. Measured large-signal performance versus input power at 140 GHz is shown in Fig. 5. The achieved P_{1dB} is 10.7 dBm, while P_{SAT} is equal to 14.8 dBm. Due to the high amplifier gain, the efficiency is also high for the given band with the maximum PAE of 8.9 % at 140 GHz. This PAE includes the power consumption of the input and driver stages. The power consumptions of all three stages and total power consumption of the PA is shown in Fig. 6. Fig. 7 shows the dependency of large-signal parameters of the PA versus frequency.

Table I summarizes the performance of the designed amplifier and compares it with other state-of-the-art PAs in D-band. Thanks to the careful design of passive interconnections and the proper sizing of transistor widths, biasing levels and the output pads, the gain and PAE are maintained high, which together with achieved high output power result in the highest FOM compared to previously published CMOS based power amplifiers around 140 GHz.

IV. Conclusion

A high-output power 140 GHz two-way parallel power combining transformer-based PA in 40 nm CMOS is presented. Input and output pads of the PA are specifically designed in order to improve performance. The amplifier achieves P_{SAT} of 14.8 dBm, small-signal gain of 20.3 dB and maximum PAE of 8.9 % at 1 V supply. In comparison with other CMOS state-of-the-art solutions, this PA shows the highest output power and the best overall performance. Together with large bandwidth and small area, this PA presents a suitable solution for implementations in future D-band applications.

V. Acknowledgment

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