A 14b 200MS/s DAC with SFDR>78dBc, IM3<-83dBc and NSD<-163dBm/Hz across the whole Nyquist Band enabled by Dynamic-Mismatch Mapping

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Abstract

A 14-bit 200MS/s current-steering DAC with a novel digital calibration technique called dynamic-mismatch mapping (DMM) is presented. Compared to traditional static-mismatch mapping and dynamic element matching, DMM reduces the nonlinearities caused by both amplitude and timing errors, without noise penalty. This 0.14μm CMOS DAC achieves a state-of-the-art performance of SFDR>78dBc, IM3<-83dBc and NSD<-163dBm/Hz across the whole Nyquist band.

Keywords: DAC, mismatch, timing error and calibration

Introduction

Process variation and layout asymmetry in current sources, latches, clock distribution etc., are error sources that result in amplitude & timing mismatch errors in a DAC and limit the performance [1-6]. Existing calibration techniques only focus on amplitude errors, such as trimming current sources [1-2] and static-mismatch mapping (SMM) [3]. However, as signal and sampling frequencies increase, the effect of timing errors will dominate that of the amplitude errors. Thus, the improvement on the DAC's dynamic performance will become negligible if only amplitude errors are addressed. Moreover, unlike amplitude errors, timing errors are far more difficult to be reduced by intrinsic circuit design, even with high power consumption in latches and symmetrical layout [4]. Dynamic element matching (DEM) randomizes signal-dependent distortion caused by both amplitude and timing errors, and as such improves the time-averaged linearity, but at the cost of significantly increased noise floor [5].

In this work, a 14b 200MS/s Nyquist current-steering DAC is presented that features a novel digital calibration technique called dynamic-mismatch mapping (DMM) to improve both DAC's static and dynamic performance, without affecting the noise performance and with minimal overhead in DAC core.

Dynamic-Mismatch Mapping (DMM)

Static mismatch is well known as amplitude errors of current cells in DACs. However, in most applications, current cells are used as switched-current cells, rather than static current sources. As shown in Fig.1(a), the mismatch between the dynamic switching behaviors of current cells, including both amplitude and timing errors, is called dynamic mismatch. Obviously, compared to static mismatch, dynamic mismatch represents the matching of switched-current cells more completely and accurately. Compared to that static mismatch can be easily measured in time domain [1-2], dynamic mismatch can be measured more efficiently in frequency domain. By modulating a current cell ($cell_n$) as rectangular-wave output at a frequency (f_m), its dynamic-mismatch error, relative to a reference cell ($cell_{ref}$),

appears at all harmonic frequencies as shown in Fig.1(b). Compared to the errors at other harmonics, the errors at f_m and $2f_m$ ($e_{fm,n}$, $e_{2fm,n}$) are most dominant. Therefore, the dynamic-mismatch error of $cell_n$ can be derived by just measuring $e_{fm,n}$ and $e_{2fm,n}$. Moreover, since $e_{fm,n}$ and $e_{2fm,n}$ are vector signals, both I and Q components of $e_{fm,n}$ and $e_{2fm,n}$ have to be measured, as shown in Fig.1(c). f_m is chosen according to the weight function between amplitude and timing errors, e.g. more weight on timing errors for high sampling rate applications requires a higher f_m. In general, dynamic mismatch is not limited to amplitude and timing mismatch errors. Since it is measured as a combined mismatch effect in frequency domain, all mismatch errors are already included.

Instead of that traditional SMM optimizes the switching sequence and improves the DAC's performance by reducing the integral static mismatch (i.e. INL) based on only amplitude errors [3], the proposed DMM improves the DAC's performance by reducing the integral dynamic mismatch (dynamic-INL) so that both amplitude and timing errors can be calibrated. Similar to the INL, the dynamic-INL is defined as equation (1), where n=1~number of current cells.

$$dynamic\text{-}INL = \max\left(\sqrt{\left| \sum_{i=1}^{n} e_{fm,i} \right|^2 + \left| \sum_{i=1}^{n} e_{2fm,i} \right|^2} \right) \quad (1)$$

Since a segmented DAC's performance is typically dominated by the thermometer part (MSBs), in this work, the proposed DMM finds an optimized switching sequence of MSBs to reduce the dynamic-INL by sorting their measured dynamic-mismatch errors.
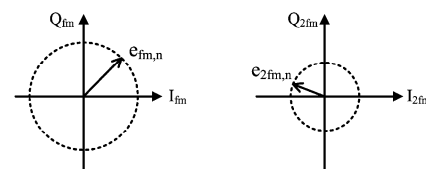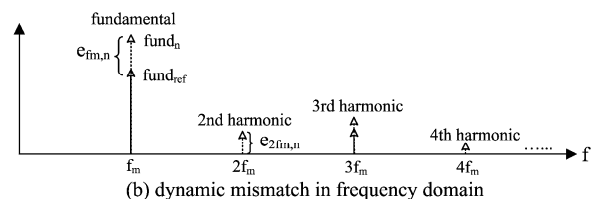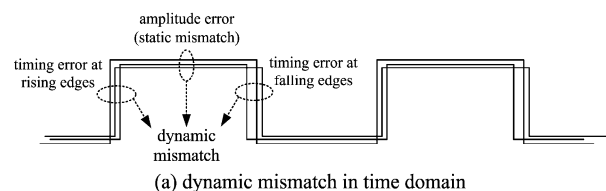

(a) dynamic mismatch in time domain

(b) dynamic mismatch in frequency domain

(c) dynamic mismatch in a I-Q plane

Fig.1 Dynamic Mismatch

Circuit Design and Measurement Results

The architecture and die photo of this 14-bit 0.14μm CMOS DAC are shown in Fig.2. It has the same current source array and two CML latch stages as [4]. An additional pair of cascode switches (M3, M4) is added to every MSB cell to measure dynamic mismatch. The MSBs are measured offline one-by-one. A memory-based decoder enables programming of the switching sequence optimized by DMM. This chip has an active area of 2.4mm^2 and consumes 270mW at 1.8V.

Fig.3 shows the circuit diagram of the on-chip dynamic-mismatch sensor which is based on a zero-IF receiver. The n-th MSB cell (cell$_n$) and the reference cell (cell$_{ref}$) are switched with opposite phases as square waves at f$_m$, which can be shifted digitally by 90° to measure I or Q, so that the ac signal at the summation node only comprises mismatch errors. A current-bleeding source takes half dc current so that a larger loading resistor can be used to increase the signal gain. Then the signal is down-converted to dc by a passive mixer followed by a low-noise trans-impedance amplifier (TIA) with RC low-pass filtering. A 5th-order CT ΣΔ ADC based on [6] is used to digitize the output.

Fig.4 shows the measured IM3 and noise power spectral density (NSD), with traditional SMM and proposed DMM. As shown, with SMM the improvement on IM3 reduces gradually with signal frequencies, which means that the benefit from only calibrating amplitude errors decreases and almost negligible above 95MHz. However, proposed DMM provides an additional benefit on IM3 by also calibrating timing errors, especially at high frequencies, resulting in a total improvement of 10dB at low frequencies and still 5dB up to Nyquist. Moreover, unlike DEM, DMM does not increase the noise floor because the mismatch effect is reduced instead of randomized. The NSD remains <-163dBm/Hz, independent on mapping. With DMM, the SFDR of the whole Nyquist band is also improved from >73dBc to >78dBc. The INL is improved from 3.2LSB to 1.7LSB with SMM and 1.8LSB with DMM. Compared to traditional SMM, DMM has a negligible less improvement on the DAC's static linearity (INL), but gains a significant more improvement on the DAC's dynamic linearity (e.g. IM3, SFDR), especially at high frequencies.
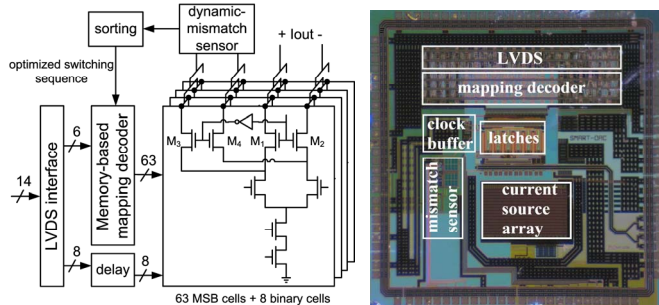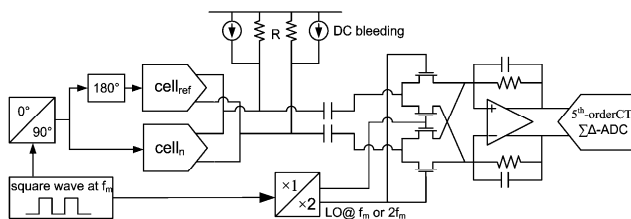
Conclusions

We concluded with a SFDR comparison with state-of-the-art CMOS DACs at similar sampling rate (f$_s$), as shown in Fig.5. Compared to the DACs with conventional calibrations [1-2], this work achieves much better SFDR and maintains above 78dBc in the whole Nyquist band. Compared to the best published DEM DAC [5], this work has 21dB better NSD and comparable SFDR. In summary, this work presents a state-of-the-art 14b 200MS/s DAC with a novel digital calibration technique called DMM that significantly improves the DAC's performance, especially the linearity at high frequencies, without increasing the noise floor.

References

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Fig.2 DAC Architecture and Die Photo

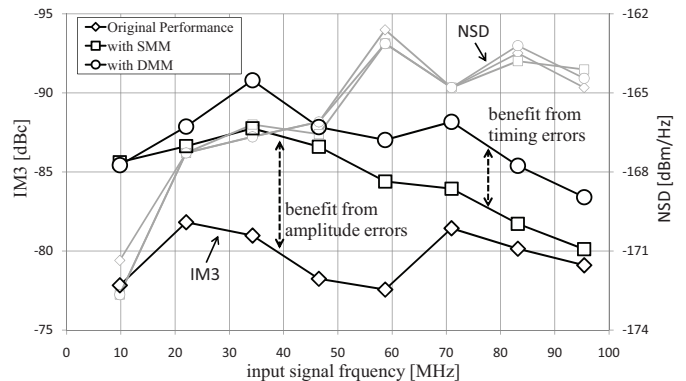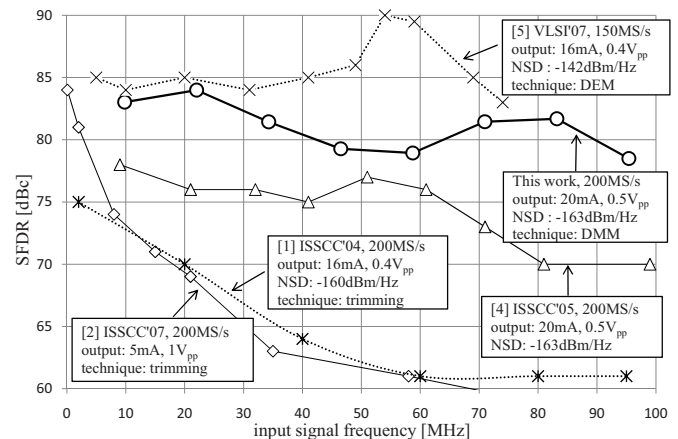Fig.3 On-chip Dynamic-Mismatch Sensor

Fig.4 Measured IM3 and NSD

Fig.5 SFDR comparison with state-of-the-art DACs at similar f$_s$