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A 16.1-bit Resolution 0.064-mm 2 Compact Highly Digital Closed-Loop Single-VCO-Based 1-1 Sturdy-MASH Resistance-to-Digital Converter With High Robustness in 180-nm CMOS — Source link

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A 16.1-bit Resolution 0.064mm^2 Compact Highly-Digital Closed-Loop Single-VCO-based 1-1 Sturdy-MASH Resistance-to-Digital Converter with high Robustness in 180nm CMOS

Elisa Sacco, *Student Member, IEEE,* Johan Vergauwen, *Member, IEEE,* and Georges Gielen, *Fellow, IEEE*

***Abstract*—A novel direct resistive-sensor-to-digital readout circuit is presented that achieves 16.1-bit ENOB while being very compact and robust. The highly-digital time-based architecture employs a single VCO, counter and digital feedback loop for the read-out of an external single-ended highly-nonlinear resistive sensor such as a NTC thermistor. In addition to the inherent 1st-order noise shaping due to the oscillator, a second loop in SMASH configuration creates 2nd-order noise shaping. Fabricated in 180nm CMOS, the readout circuit achieves 16.1 bit of resolution for 1ms conversion time and consumes only 171µW, resulting in an excellent 2.4pJ/c.s. FOM$_W$ for a resistive sensor interface, while occupying only 0.064mm^2. The specific closed-loop architecture tackles the VCO nonlinearity, achieving more than 14 bits of linearity. Multiple prototype chip samples have been measured in a temperature-controlled environment from -40°C to 125°C for the readout of commercial external NTC thermistors. A maximum temperature inaccuracy of 0.3°C is achieved with only 1-point trimming at room temperature. Since the circuit architecture decouples the sensor excitation from the feedback, high EMI immunity at the sensor node is demonstrated as well.**

***Index Terms*—VCO, VCO-based ADC, time-based ADC, delta-sigma modulation, sensor interface, sensor applications, digital readout circuits, resistive sensor readout circuit, closed loop, 1st-order noise shaping, 2nd-order noise shaping, SMASH.**

I. Introduction

$\Delta\Sigma$ architectures are generally used in low-bandwidth applications, such as sensor interfaces, biomedical, automotive, audio, etc., in order to achieve high-resolution analog-to-digital conversion at low power. Traditionally, $\Delta\Sigma$ modulators rely on conventional analog building blocks, such as high-gain operational amplifiers [1], [2] in the forward path, and high-precision DACs in the feedback path, and for sensing applications they are often preceded by a high-performance instrumentation amplifier [2], [3], [4]. By exploiting CMOS process scaling, which enables faster switching devices, $\Delta\Sigma$ ADCs have dramatically improved their achievable bandwidth [5]. However, the very same process scaling comes with lower intrinsic transistor gain, poorer matching [6], and reduced voltage headroom, thus making analog circuits more difficult to design and with an increasing need for digital calibration [7]. Therefore, analog architectures do not follow the same power reduction and area scaling as digital circuits, resulting in solutions with large power and large chip area in scaled CMOS technologies.

For all these reasons, there has been a tendency to explore time-based analog circuit solutions that exploit a highly-digital implementation, resulting in a small area, a high energy efficiency and a good process scalability [8]. Time-based solutions include various types of time-domain processing from pulse density modulation (PDM) [9], dual-slope conversion [10], [11], [12] to using voltage-controlled oscillators (VCOs) and/or gated-ring oscillators (GROs) [13]–[20] to process the signal in the time domain rather than in the voltage domain. In this paper the focus will be on VCO-based architectures. There are, however, mainly two issues that limit the performance of VCO-based readout circuits:

- *Limited resolution due to limited noise shaping order*: many of the VCO-based architectures achieve only 1st-order quantization noise shaping.
- *Nonlinearity*: the overall input-output linearity is limited by the typically nonlinear voltage-to-frequency conversion of VCOs.

Overcoming both limitations is fundamental in sensor applications, where both high resolution and high linearity are required, besides small area and high robustness.

This paper focuses on a technology-scalable solution to digitally read out resistive sensors. Integrated or external resistive sensors are used in many sensing systems, e.g. for temperature sensing. IntegratedNegative Temperature Coefficient (NTC) and/or Positive Temperature Coefficient (PTC) resistive sensors for temperature sensing are mainly used in embedded systems for temperature compensation [21], [22]. Other solutions to monitor system/chip conditions exploit the temperature dependency of different quantities, as in [23] where the temperature dependency of the VCO oscillation frequency is used as sensing element. In [21] a traditional 2nd-order CT $\Delta\Sigma$ modulator is employed for readout, thus resulting in poor process scalability due to the use of OTAs. In [22] and [23] more digital-friendly solutions are proposed, employing a VCO in a frequency-locked loop (FLL) and a

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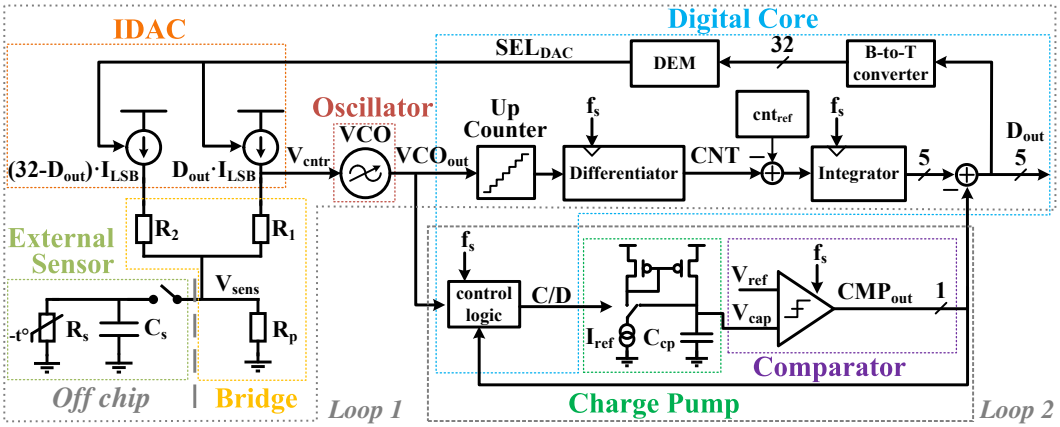

Fig. 1. Sensor readout block diagram.

VCO followed by a counter (FDC), respectively. However, these solutions require 2-point trimming and systematic error correction, resulting in increased test time and cost. Moreover, they suffer from poor linearity and only achieve 1st-order noise shaping.

As external resistive sensors, NTC thermistors are widely used as temperature sensors for high-volume products thanks to their low cost. For example, they are used in many automotive applications (e.g. HVAC (Heating, Ventilating, and Air Conditioning) systems, TMAP (Temperature and Manifold Absolute Pressure)). Challenges are the wide variation range and highly-nonlinear behavior of such thermistors. For the readout of external differential resistive sensors, [24] employs a traditional SAR architecture, while in [25] and [26] two VCOs are used in a phase-looked loop (PLL) configuration, leading to a highly digital implementation, but with only 1st-order noise shaping. These solutions all showed a limited resolution well below the typically desired 16 bits.

The goal of the presented design is to implement a compact and robust high-resolution time-based architecture for the readout of external single-ended resistive sensors with high energy efficiency. The VCO nonlinearity is tackled by placing the oscillator in a closed loop, while the noise shaping order is increased using a 1-1 Sturdy Multi-stAge noise SHaping (SMASH) configuration [27]. Thanks to these major novelties, the designed circuit's characteristics are:

- a resolution of 16.1 bits in 1ms conversion time;
- 2nd-order noise shaping by implementing a time-based 1-1 SMASH $\Delta\Sigma$ modulator;
- a high linearity above 14 bits due to the specific closed-loop configuration;
- a compact chip area and technology-scalable solution due to the highly-digital VCO-based implementation;
- operation over the whole automotive temperature range (-40°–125°C), while requiring only 1-point trimming at room temperature to achieve a high temperature accuracy;
- high EMI (Electro-Magnetic Interference) immunity as the architecture allows large low-pass filtering at the sensor input node.

Multiple prototype chips have been measured for full characterization, without and with commercial external resistive sensors.

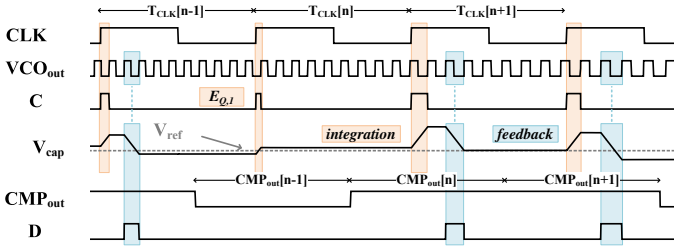

Fig. 2. *Loop 2* timing diagram.

This paper is a full extension of [28], and is organized as follows. In Section II an overview of the sensor interface architecture is given. Section III details the circuit implementation in CMOS technology. Experimental measurement results are provided in Section IV. Finally, Section V concludes the paper.

II. System-Level Overview

A. Architecture

Fig. 1 shows the block diagram and the basic building blocks of the resistive sensor readout circuit. The resistive sensor R_s is external to the chip. The proposed 1-1 SMASH architecture realizes two closed loops (*Loop 1* and *Loop 2*), one of which includes the voltage-controlled oscillator (VCO). *Loop 1* consists of the resistive bridge (R_1, R_2 and R_p), the VCO, a digital core including the counter and differentiator, and the current-steering DAC (IDAC) for feedback. The digital output D_{out}, when only *Loop 1* is considered, results from integrating the difference between two counts: the number of VCO edges in one sampling period and the constant variable $\mathrm{cnt}_{\mathrm{ref}}$. This $\mathrm{cnt}_{\mathrm{ref}}$ subtraction is performed to remove the common-mode signal generated by the central frequency f_0 of the VCO. *Loop 2* consists of control logic, a charge pump and a comparator. As shown in Fig. 2, the time difference between the sampling edge and the next VCO edge corresponds to the quantization error in the time domain. During this time the charge signal C, generated by the control logic of *Loop 2*, is up and the capacitor C_{cp} is charged by a constant current I_{ref}, performing the integration. To implement the feedback signal

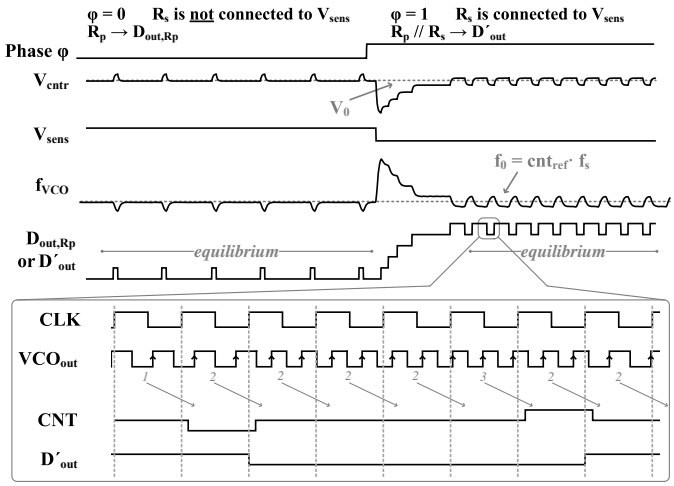

Fig. 3. Example timing diagram of the VCO-counter-based system, showing the most important signals.

of *Loop 2*, the discharge signal D is generated to discharge the capacitor C_{cp} by the current I_{ref}: D is up for a VCO period if the previous comparator decision CMP_{out} was 1, otherwise D is down. To obtain the final digital output in SMASH configuration, the 1-bit digital output $(0/1)$ of *Loop 2* is subtracted from the 5-bit digital output of *Loop 1*.

The result in Fig. 1 is a highly-digital opamp-free VCO-based closed-loop system, which achieves robust conversion, high linearity, 2nd-order noise shaping, and compact area, as will be detailed in the following sections.

B. System Operation and Input-Output Characteristic

This work focuses on interfacing and digitally reading out highly-nonlinear and wide-range resistive sensors R_{s}, such as NTC thermistors. The purpose of the parallel resistor R_{p} in Fig. 1 is twofold: 1) to obtain a rough linearization of the NTC resistance R_{s}, 2) to limit the range of resistance to be measured from 5-6 decades in case of R_{s} only, to 1-2 decades in case of $R_{\mathrm{p}} \parallel R_{\mathrm{s}}$. This comes at the expense of a reduced sensitivity $S_{R_{\mathrm{p}} \parallel R_{\mathrm{s}}}$ for large values of R_{s}, while there is a negligible effect for small values of R_{s}, as shown in Fig. 4. Due to the large nonlinearity of the NTC thermistor (see Fig. 18(a)), the sensitivity $S_{R_{\mathrm{p}} \parallel R_{\mathrm{s}}}$ is made comparable over a wide range in the architecture of Fig. 1.

Since the proposed architecture utilizes a single-ended approach, a conversion consisting of two phases is used, as shown in Fig. 3. Firstly, in phase ϕ_0, the resistive sensor R_{s} is not connected to the bridge, thus the digital output $D_{\mathrm{out,R_p}}$ is the representation of the on-chip resistor R_{p} only. Secondly, in phase ϕ_1, R_{s} is connected in parallel to R_{p}, thus the digital output $D^{'}_{\mathrm{out}}$ is the representation of $R_{\mathrm{p}} \parallel R_{\mathrm{s}}$. By subtracting $D_{\mathrm{out,R_p}}$ from $D^{'}_{\mathrm{out}}$, the final system digital output D_{out} is obtained.

Due to the closed loop, in equilibrium, the voltage V_{cntr} at the VCO input is on average equal to some operating voltage V_0, as shown in Fig. 3. By expressing the VCO characteristic as: $f_{\mathrm{VCO}} = f_0 + K_{\mathrm{VCO}} \cdot (V_{\mathrm{cntr}} - V_0)$, the VCO frequency results to be on average f_0, which is such that the number of

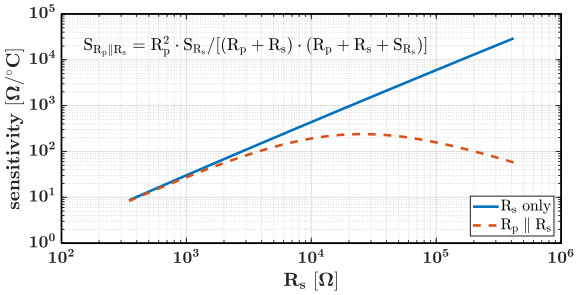

Fig. 4. Temperature sensitivity of a typical NTC thermistor with respect to the resistance value when considered standalone and in parallel with R_{p}. The equation to calculate the sensitivity of $R_{\mathrm{p}} \parallel R_{\mathrm{s}}$ is also shown in the figure.

VCO edges occurring within each sampling clock period ($T_{\mathrm{s}} = 1/f_{\mathrm{s}}$) is on average equal to the user-set reference count value $\mathrm{cnt_{ref}} = f_0/f_{\mathrm{s}}$, as shown in Fig. 3. During phase ϕ_0, only the internal resistor R_{p} is connected to the bridge. Therefore, in equilibrium, the voltage V_{cntr} can be expressed as:

$$V_0 = \overline{V}_{\mathrm{cntr}\,\phi_0} = R_{\mathrm{p}} \cdot 2^N \cdot I_{\mathrm{LSB}} + R_1 \cdot D_{\mathrm{out,R_p}} \cdot I_{\mathrm{LSB}} \quad (1)$$

where R_{p} is the internal parallel resistor at the input, R_1 is the bridge resistor, N is the number of bits in the feedback IDAC, I_{LSB} is the IDAC LSB current value and $D_{\mathrm{out,R_p}}$ is the digital output. During phase ϕ_1, both R_{p} and R_{s} are connected in parallel to the bridge. Therefore, in equilibrium, the voltage V_{cntr} can be expressed as:

$$V_0 = \overline{V}_{\mathrm{cntr}\,\phi_1} = (R_{\mathrm{p}} \parallel R_{\mathrm{s}}) \cdot 2^N \cdot I_{\mathrm{LSB}} + R_1 \cdot D^{'}_{\mathrm{out}} \cdot I_{\mathrm{LSB}} \quad (2)$$

where R_{s} is the external resistive sensor and $D^{'}_{\mathrm{out}}$ is the digital output. Assuming equilibrium, by equating the value of the voltages $\overline{V}_{\mathrm{cntr}}$ ((1) and (2)) in the two phases, ϕ_0 and ϕ_1, the system input-output equation can be expressed as follows:

$$\begin{aligned} R_{\mathrm{p}} \parallel R_{\mathrm{s}} &= \frac{R_1 \cdot D_{\mathrm{out,R_p}}}{2^N} + R_{\mathrm{p}} - \frac{R_1}{2^N} \cdot D^{'}_{\mathrm{out}} \\ &= R_{\mathrm{p}} - \frac{R_1}{2^N} \cdot (D^{'}_{\mathrm{out}} - D_{\mathrm{out,R_p}}) = \underbrace{R_{\mathrm{p}}}_{\text{offset}} \underbrace{- \frac{R_1}{2^N}}_{\text{gain}} \cdot D_{\mathrm{out}} \end{aligned} \quad (3)$$

Thanks to the closed-loop architecture, (3) depends 1) on the passive resistive components R_{p} and R_1, and 2) on the difference between the digital outputs $D^{'}_{\mathrm{out}}$ and $D_{\mathrm{out,R_p}}$, making this architecture capable of a robust readout. In fact, while the digital outputs $D^{'}_{\mathrm{out}}$ and $D_{\mathrm{out,R_p}}$ are dependent on PVT variations, the difference D_{out} is not. The value of R_{s} can easily be calculated from (3) resulting in the following equation:

$$R_{\mathrm{s_{1-p}}} = R_{\mathrm{p}} \cdot \left(\frac{R_{\mathrm{p}}}{R_1} \cdot \frac{2^N}{D_{\mathrm{out}}} - 1 \right) \quad (4)$$

As shown in Fig. 3, when switching from phase ϕ_0 to phase ϕ_1, the VCO experiences an abrupt change in the control input voltage V_{cntr}, due to the change in the input resistor from R_{p} only to $R_{\mathrm{p}} \parallel R_{\mathrm{s}}$. This causes the VCO to run at a frequency different from $\mathrm{cnt_{ref}} \cdot f_{\mathrm{s}}$, resulting in the loop to be out of equilibrium. In order for the closed loop to return to equilibrium, several clock cycles are needed. The time, i.e.

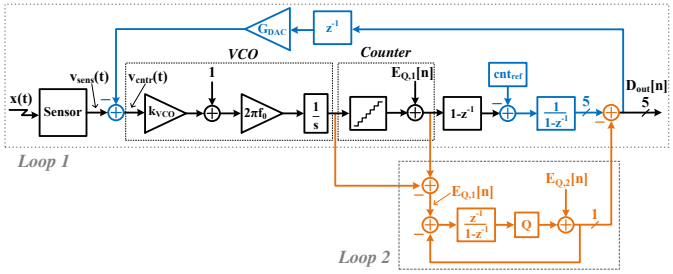

Fig. 5. Equivalent model of the sensor readout circuit in the z-domain.

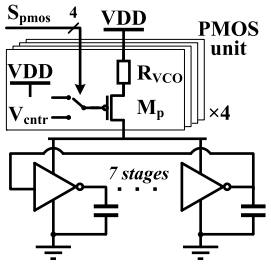

Fig. 6. Circuit schematic of the inverter-based VCO in *Loop 1*.

the number of clock cycles, needed to regain equilibrium is proportional to the difference in effective resistance between the two phases, and is inversely proportional to the VCO gain.

C. System Linearity and 2nd-Order Noise Shaping

The frequency-domain model of the proposed VCO-based sensor readout is shown in Fig. 5. The classical open-loop VCO-counter architecture [15] has been modified into a closed-loop structure by adding the blocks marked in blue, implementing the *Loop 1*. Considering *Loop 1* only, the signal transfer function STF_1 from the analog input v_{sens} to the digital output D_{out}, in the band of interest, can be approximated by a simple gain factor with a unit delay ($\mathrm{STF}_1 \propto z^{-1}$), while the noise transfer function NTF_1 from the quantization error $E_{\mathrm{Q},1}$ at the counter to the digital output D_{out}, in the band of interest, corresponds to a high-pass filter that first-order noise shapes the quantization error ($\mathrm{NTF}_1 \propto 1 - z^{-1}$). Therefore, the proposed closed-loop configuration (*Loop 1*) behaves similarly to [15], realizing a 1st-order $\Delta\Sigma$ modulator in the time domain thanks to the integrating property of the VCO, with the advantage of having a more robust input-output characteristic, as discussed in Section II-B above. Moreover, thanks to the closed-loop architecture (*Loop 1*), the VCO input voltage V_{cntr} is kept within a small range and is on average constant. Since this range is significantly smaller than the full VCO range, the nonlinearity of the VCO does not appear at the output, resulting in a highly linear conversion.

Loop 1, however, achieves only 1st-order noise shaping. In [13], [16], [17], [29] higher-order noise shaping is achieved by means of a single-loop modulator [16], [17] or a SMASH structure [13], [29]. The overall system linearity is, however, limited by the VCO nonlinearity, which is external to the closed loop and which experiences the full signal swing. In [30] 2nd-order noise shaping is achieved in a single loop using a PLL structure, overcoming the VCO nonlinearity limitation. However, two VCOs and an external clock reference are used. In this work, a single-VCO approach is used to further reduce the area and to intrinsically eliminate any VCO-mismatch-related issues. In order to achieve 2nd-order noise shaping while employing only one VCO and a sampling clock, a 1-1 SMASH [27] architecture is used. Differently from MASH architectures like in [31]–[33], the proposed SMASH system does not suffer from inter-stage mismatch. Finally, being a 1-1 SMASH modulator, the stability of this architecture is similar to that of a 1st-order system, and thus not a problem. In MASH and SMASH architectures, the quantization error of the first stage is fed as input to the second stage in a cascaded way. When the first stage is implemented using a VCO, the quantization error is intrinsically created in the time domain. This time-domain quantization error is processed by gated-ring oscillators [32], VCOs [33] or digitally-controlled oscillators (DCOs) [16], [17], requiring a multi-bit digital output for the second stage.

Therefore, the presented 1-1 SMASH solution features a second loop, *Loop 2*, which is added to the architecture, and which receives as input the time-domain quantization error $E_{\mathrm{Q},1}$ of *Loop 1*. As represented by the orange blocks in Fig. 5, *Loop 2* implements a simple and compact 1-bit $\Delta\Sigma$ modulator. Its signal transfer function STF_2 and noise transfer function NTF_2 are a simple delay factor (z^{-1}) and a differentiator, ($1 - z^{-1}$) respectively. The *Loop 2* 1-bit output is directly subtracted from the *Loop 1* 5-bit output to generate the overall 5-bit system output, which is fed back to the input through the DAC, thus realizing a SMASH architecture. The system output in the frequency domain can be expressed as [34]:

$$\begin{aligned} D_{\mathrm{out}} = {} & X \cdot \mathrm{STF}_1 + E_{Q,1} \cdot \mathrm{NTF}_1 \cdot (1 - \mathrm{STF}_2) + \\ & E_{Q,2} \cdot \mathrm{NTF}_1 \cdot \mathrm{NTF}_2 \\ \approx {} & X \cdot z^{-1} + E_{Q,1} \cdot (1 - z^{-1})^2 + E_{Q,2} \cdot (1 - z^{-1})^2 \end{aligned} \tag{5}$$

where X is the sensor input signal, STF_i, NTF_i and $E_{Q,i}$ denote the signal transfer function, the noise transfer function and the quantization error of the i-th loop, respectively. By considering the nature of the $\mathrm{STF}_i/\mathrm{NTF}_i$, as previously described, it is clear from (5) that 2nd-order noise shaping is realized for both quantization errors $E_{Q,1}$ and $E_{Q,2}$. Therefore, the proposed architecture achieves both 2nd-order noise shaping and high linearity in an area-compact solution.

III. Circuit Implementation

The main features and implementation details of the building blocks in the presented design are described in this section.

A. VCO

The schematic of the VCO in *Loop 1* is shown in Fig. 6. The transistor $\mathrm{M_p}$ converts the control voltage V_{cntr} into a current that drives a 7-stage current-controlled oscillator (CCO). A PMOS tail current is chosen over an NMOS to reduce flicker noise. This VCO topology has been selected mainly for two reasons: firstly, it realizes a highly-digital and easily-scalable

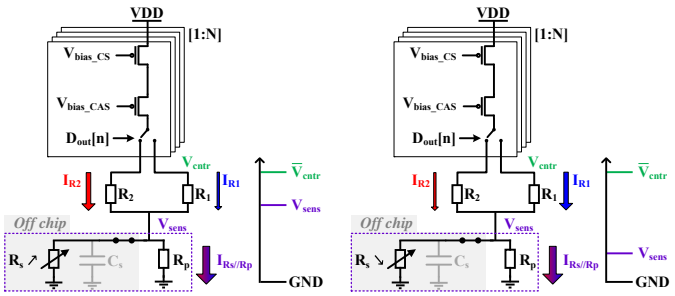

Fig. 8. Circuit schematic of the IDAC and the resistive bridge. Qualitative voltage levels and current magnitudes are shown for large (left) and small (right) resistive sensor values R_s.

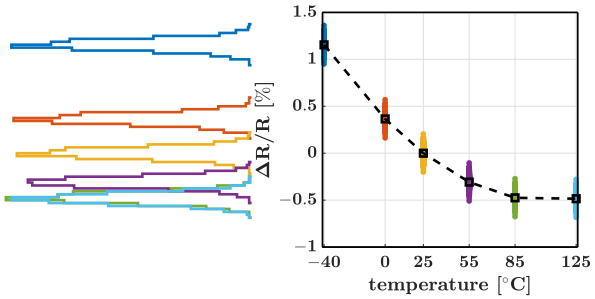

Fig. 9. Simulated variation of the resistance as a function of temperature (right), considering Monte-Carlo mismatch variation (left) for the bridge resistors R_p and R_1.

implementation, and secondly, its input-output characteristic is voltage-to-frequency (V-to-f) linear, thus satisfying the requirement for the VCO-counter architecture [35].

The VCO central frequency f_0 is made tunable by activating 1 to 4 identical PMOS units through the selection signal $\mathrm{S_{pmos}}$[1:4] (Fig. 6. The number of selected units is proportional to the VCO central frequency, since each PMOS unit is biased by the bridge output voltage V_cntr and contributes in the same manner to the total current driving the CCO. Therefore, increasing the number of active units allows to increase the sampling frequency of the whole system, thus reducing the conversion time at the expense of increasing the current consumption in both the VCO and the digital core. A tunable resistor R_VCO degenerates the PMOS transistor, improving the linearity and lowering the $1/f$ corner frequency of the VCO at the expense of some gain loss.

B. IDAC and Resistive Bridge

The overall feedback is realized by a 5-bit thermometer-coded current-steering DAC (IDAC), as shown in Fig. 8. The nominal LSB current is 700nA. This value has been chosen so that the bridge output voltage V_cntr (which is also the VCO input voltage) ensures the functionality of the oscillator, when the system is locked and in equilibrium. Since the IDAC provides both the feedback signal and the biasing of the external resistive sensor R_s, the loop is closed with no extra power, resulting in a high energy efficiency. In fact, the current through the parallel combination of the external resistive sensor and the internal resistor ($R_\mathrm{s} \parallel R_\mathrm{p}$) is always equal to $32 \cdot I_\mathrm{LSB}$, independently of the sensor resistance value, as shown in Fig. 8 by the purple arrow. The feedback, on the other hand, controls the amount of current flowing through the resistor R_1, shown as a blue arrow in Fig. 8, such that the resulting voltage V_cntr, which is fed as input of the VCO, remains on average constant and equal to V_0 (see Sec. II-B). The current through the resistor R_2 does not create any useful voltage, but it is essential to the architecture, since the currents flowing through both R_1 and R_2 are summed at the sensor node V_sens, creating the constant current through $R_\mathrm{s} \parallel R_\mathrm{p}$.

To limit the range of the voltage V_sens for a large resistive sensor range ($R_\mathrm{s} \in [100\Omega\text{–}1\mathrm{M}\Omega]$), the internal resistor R_p of approximately $20\mathrm{k}\Omega$ is placed in parallel to the external sensor R_s. In order to properly size the resistor R_1 such as

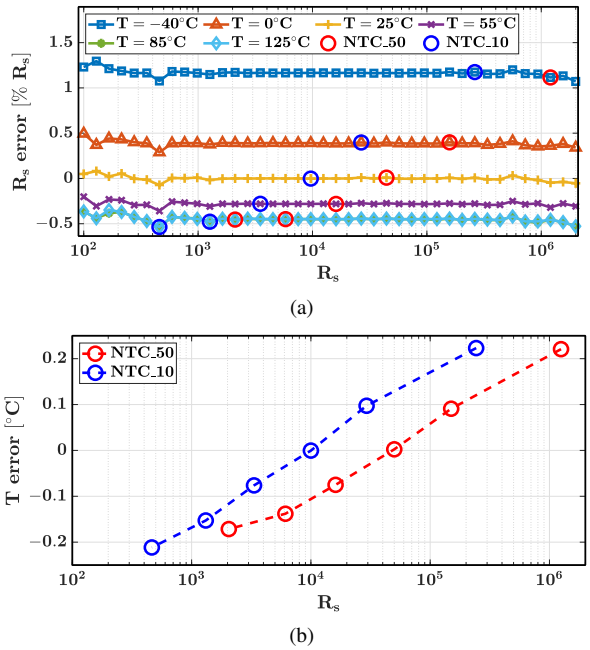

Fig. 10. (a) Simulated resistance error at different temperatures for different values of R_s using the offset and gain coefficients extracted at room temperature. The blue and red circles indicate the resistive value and the corresponding error for two different NTC thermistors, NTC50 [36] and NTC10 [37], respectively. (b) Calculated temperature error as a function of the value of R_s at different temperatures due to the error reported in (a) for both thermistors. In this case, the temperature of the chip and of the NTC thermistor are assumed to be the same.

to be able to convert the whole targeted resistive input range, the following considerations are made. Assuming a resistive sensor R_s varying between 100Ω and $1\mathrm{M}\Omega$, and a parallel internal resistor R_p of $20\mathrm{k}\Omega$, the equivalent $R_\mathrm{s} \parallel R_\mathrm{p}$ range is approximately between 100Ω and $20\mathrm{k}\Omega$. Since the modulator needs to properly operate across this range, the equations representing the bridge output voltage V_cntr in equilibrium for the extreme limit input range values can be expressed as follows:

$$\begin{aligned}\overline{V}_{\mathrm{cntr}(R_\mathrm{s}\parallel R_\mathrm{p})_\mathrm{max/min}} &= R_1 \cdot D'_{\mathrm{out,min/max}} \cdot I_\mathrm{LSB} \\ &+ (R_\mathrm{s} \parallel R_\mathrm{p})_\mathrm{max/min} \cdot 2^N \cdot I_\mathrm{LSB} \quad (6)\end{aligned}$$

where D'_out is the digital output, N is the IDAC number of bits, and I_LSB is the IDAC LSB current. A qualitative

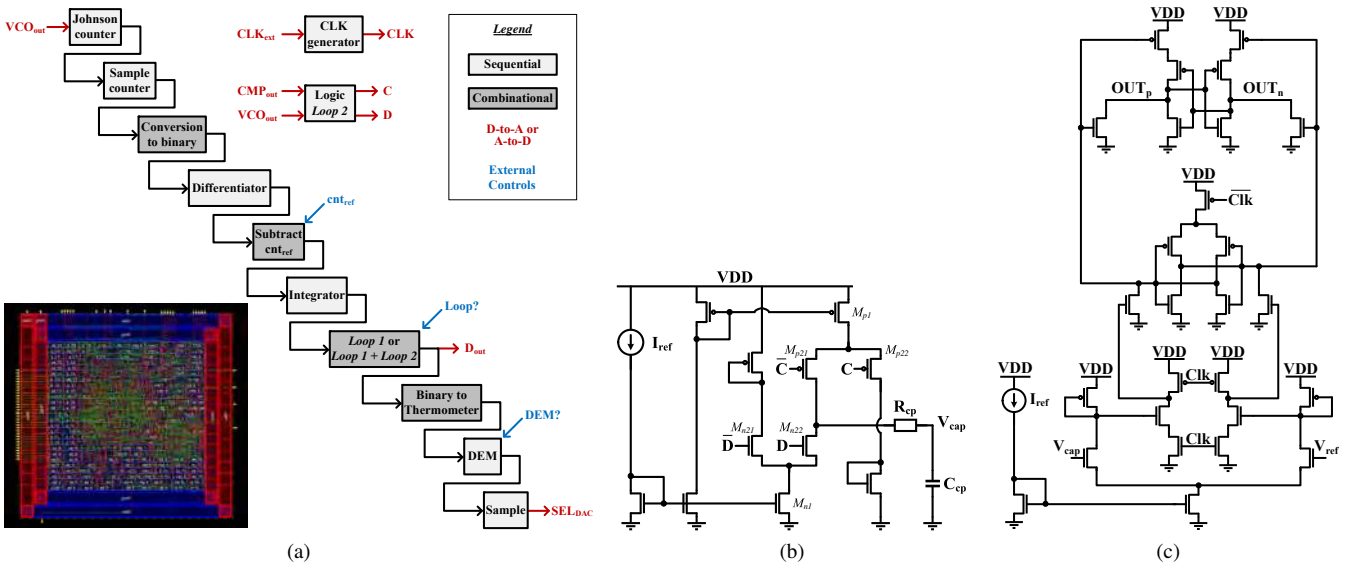

Fig. 7. Digital core (a). Circuit schematic of the charge pump (b) and of the comparator (c) in *Loop 2*.

representation of the relevant bridge voltages is shown in Fig. 8 for the two cases: large and small R_s, respectively.

Thanks to the closed loop, the voltage V_cntr is kept constant on average, independently of R_s. Therefore, (6) expressed for the two cases (max and min R_s) can be equated to calculate the minimum value for the bridge resistor R_1 as follows:

$$R_1 \geq \frac{(R_\mathrm{s} \parallel R_\mathrm{p})_\mathrm{max} - (R_\mathrm{s} \parallel R_\mathrm{p})_\mathrm{min}}{D'_\mathrm{out,max} - D'_\mathrm{out,min}} \cdot 2^N \tag{7}$$

where $D_\mathrm{out,max} - D_\mathrm{out,min} < 2^N$ for stability reasons. Therefore, R_1 has been chosen to be 25kΩ.

The bridge resistors R_1, R_2 and R_p have been implemented using non-salicided p-doped polysilicon to ensure good stability over temperature. Fig. 9 shows the variation in resistance as a function of temperature in combination with the Monte-Carlo mismatch variation. Using these data in a Verilog-AMS model, the estimated resistance error across the targeted external resistive sensor R_s range is calculated for different temperatures, as shown in Fig. 10(a). Using (3), all R_s values are calculated from the room-temperature values of R_p and R_1. The resistance error (in %) is constant across the wide input resistive range for each temperature value. This relative error value is equal to the resistance variation with temperature of the bridge resistors R_p and R_1 (Fig. 9). This result can be derived mathematically by explicitly indicating the temperature dependence of the bridge resistors R_p and R_1 in (4) as follows:

$$\begin{aligned} R_{\mathrm{s_T}} &= R_\mathrm{p} \cdot \left(1 + \frac{\Delta R(T)}{R}\right) \cdot \left[\frac{R_\mathrm{p} \cdot \left(1 + \frac{\Delta R(T)}{R}\right)}{R_1 \cdot \left(1 + \frac{\Delta R(T)}{R}\right)} \cdot \frac{2^N}{D_\mathrm{out}} - 1\right] \\ &= R_\mathrm{p} \cdot \left(1 + \frac{\Delta R(T)}{R}\right) \cdot \left(\frac{R_\mathrm{p}}{R_1} \cdot \frac{2^N}{D_\mathrm{out}} - 1\right) \end{aligned} \tag{8}$$

The difference between the sensor value $R_{\mathrm{s}_{1-\mathrm{p}}}$ calculated using the adopted 1-point trimming approach (4) and the sensor value $R_{\mathrm{s_T}}$ calculated considering the temperature variation of the bridge resistors (8) is equal to $R_\mathrm{s} \cdot \Delta R(T)/R$, where R_s is the resistive sensor value and $\Delta R(T)/R$ is the temperature-dependent variation of the bridge resistors in percentage, as reported in Fig. 9. This value indicates the error in the sensor value calculation due to the assumption of temperature-independent bridge resistors and the 1-point trimming calibration at room temperature. By using the data of commercially available NTC thermistors [36] and [37], it is possible to estimate a realistic temperature error due to the aforementioned assumption, as reported in Fig. 10(b). The maximum error remains below 0.25°C. Therefore, the 1-point trimming entails a single calibration point at room temperature, thus lowering the costs, at the expense of a small increase in temperature inaccuracy, which is still similar to the state of the art [22], [23].

C. Digital Core

All digital circuitry has been synthesized with standard cells and laid out with a commercial P&R tool. The sampling clock f_s is generated by a 2× clock divider from an off-chip master clock. Since the VCO and the clock are asynchronous, errors in the sampled counter value might occur due to the counter reset. In order to reduce the severity of these errors, a Johnson counter has been implemented, followed by a differentiator, which limits the worst-case count error to ±1. The variable $\mathrm{cnt_{ref}}$ is set externally. The digital output of the system D_out is a 5-bit digital word in binary representation. Since the IDAC is thermometer coded, a binary-to-thermometer (B-to-T) converter is added in the feedback loop. Moreover, a dynamic-element-matching (DEM) algorithm is implemented in the IDAC to reduce the nonlinear distortion caused by the mismatch among the LSB units. The main digital functional blocks together with the external control signals and the signal from/to the analog part are shown in Fig. 7(a).

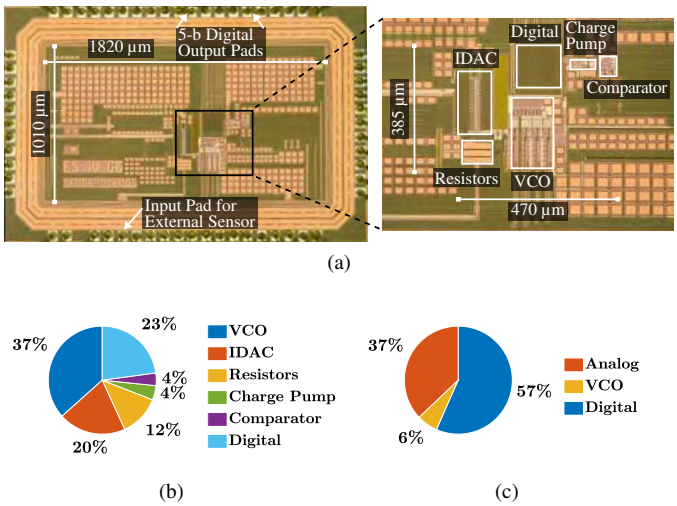

Fig. 11. Chip micrograph and zoom in of the core (a), core area breakdown (b), and typical core power breakdown (c).

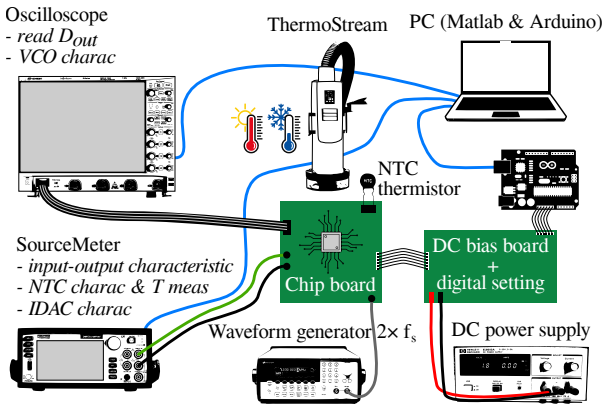

Fig. 12. Measurement setup for the resistive sensor interface.

D. Charge Pump and Comparator

The charge pump, shown in Fig. 7(b), has been designed to provide the same charge/discharge current using always-on current mirrors (transistors M_{n1} and M_{p1}). The constant current flow, independent of the charge C and discharge D signals, ensures more stable voltages, which, in turn, ensures a more accurate integration, at the expense of a slight increase in power consumption. The transistors M_{n21}, M_{n22}, M_{p21} and M_{p22} are minimum in size to minimize charge injection.

The 1-bit quantizer, shown in Fig. 7(c), has been implemented as a two-stage dynamic latch-based comparator preceded by an amplifier to minimize the kickback, which can jeopardize the integration signal V_{cap}. The first input stage provides additional gain and is followed by the second regenerative stage. Finally, the SR latch provides the rail-to-rail NRZ comparator output. Since both circuits operate in *Loop 2* of the Sturdy-MASH modulator, the noise requirements are greatly relaxed, allowing scalability.

IV. Experimental Results and Discussion

The prototype chip, shown in Fig. 11(a), has been fabricated in a standard 180nm CMOS process and occupies an active area of only 0.064mm^2. Fig. 11(b) and Fig. 11(c) show the area and power breakdown for typical operation conditions. The reported power consumption includes the sensor power, since the external resistive sensor is biased using the total IDAC current. However, since the resistive sensor is external to the chip, its area in not included. The characterization of the resistance-to-digital converter, the measurements results with an external NTC thermistor, the DPI measurement results, and the comparison with the state of the art are discussed in this section. Three random samples have been tested. The measurement setup used to characterize the sensor interface performance is shown in Fig. 12.

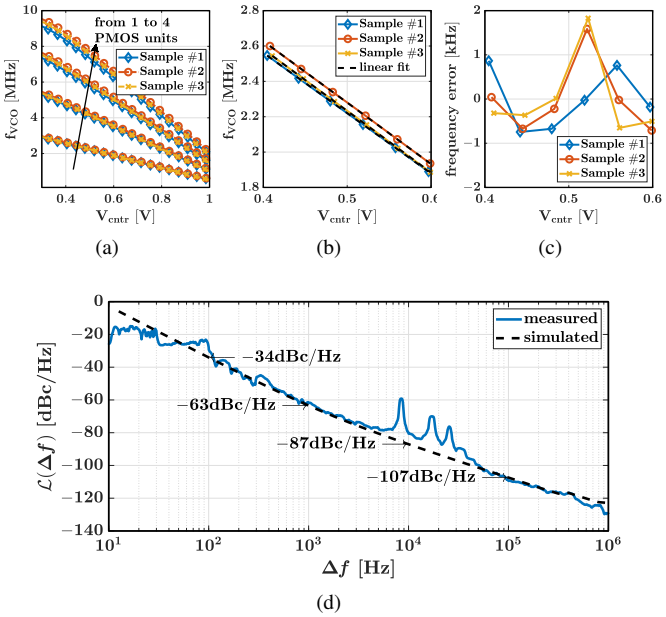

Fig. 13. (a) Measured VCO input-output characteristic for $R_{\text{VCO}} = 50\text{k}\Omega$ for multiple chip samples. (b) Measured VCO input-output characteristic for $R_{\text{VCO}} = 50\text{k}\Omega$ and 1 PMOS unit in the equilibrium operation region, and (c) the frequency error with respect to the linear fit. (d) Phase noise measurement for $R_{\text{VCO}} = 50\text{k}\Omega$ and with 1 PMOS unit.

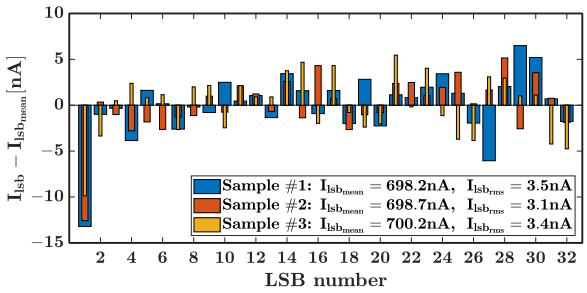

Fig. 14. Measured IDAC current values for three chip samples.

A. VCO and IDAC Characterization

In test mode, the characterizations of the standalone VCO as well as of the standalone IDAC are possible, which are the two most important blocks in the system.

1) VCO: The oscillator output is measured while externally sweeping the control input voltage. The measured VCO input-output characteristic from three samples with R_{VCO} set equal to 50kΩ is shown in Fig. 13(a). Depending on the number

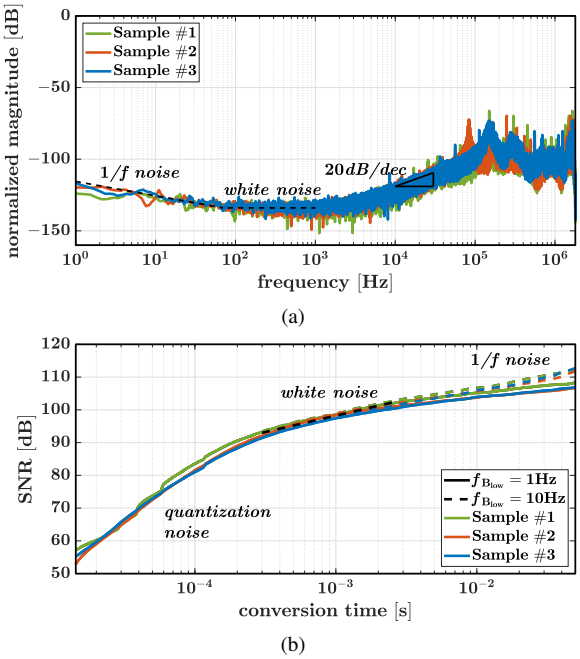

Fig. 15. Measured normalized PSD of the output bitstream (a), and plot of the SNR as a function of the conversion time (b) in the fast sampling mode: $f_s = 1.8$MHz, $\mathrm{cnt}_{\mathrm{ref}} = 2$ and all 4 VCO PMOS units activated. Three samples have been tested.

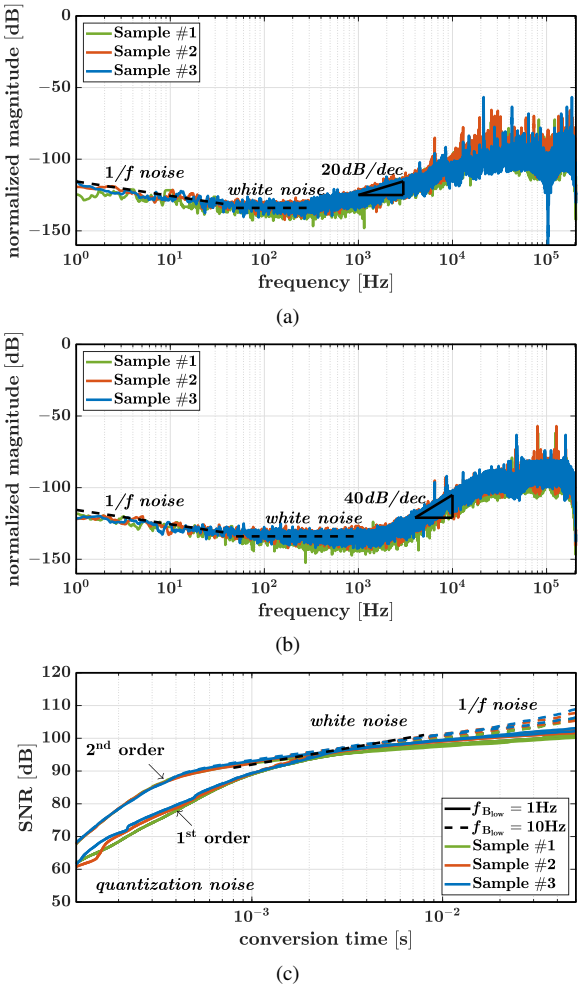

Fig. 16. Measured normalized PSD of the output bitstream (a) for 1st- and (b) 2nd-order configuration in the slow sampling mode: $f_s = 210$kHz, $\mathrm{cnt}_{\mathrm{ref}} = 8$ and 1 VCO PMOS unit activated. (c) Corresponding plot of the SNR as a function of the conversion time. Three samples have been tested.

of PMOS units activated, the central frequency can cover a wide range, allowing different operation modes. The curves are visually linear. Fig. 13(b) shows the curves for the case of one active PMOS unit for input voltage values corresponding to the equilibrium operation region. The deviation of the VCO input-output curve from a best linear fit (i.e. the nonlinearity error) is shown in Fig. 13(c). The worst-case nonlinearity is 0.28% over the considered tuning range. The average VCO free-running frequency with $V_{\mathrm{cntr}} = 0.5$V is 2.24MHz, while the average VCO gain is $-3.46\mathrm{MHz/V}$. The measured phase noise figure is -107dBc/Hz at 100kHz offset, as shown in Fig. 13(d). The $1/f$ noise corner frequency is around 2kHz. Those values are close to the simulated results. The peaks present in the measurement results around 10kHz offset are likely due to interference, but they do not affect the overall system performance. As shown in [38], the VCO gain and phase noise are key factors in determining the overall system performance in the spectrum region limited by the VCO phase noise.

2) IDAC: In Fig. 14, the measured values of the IDAC LSB currents are plotted for three chip samples. Thanks to the closed-loop architecture, the absolute value of the IDAC current is not crucial (see (3)), as long as the voltage V_{cntr} is within the VCO's functional range. The linearity of the IDAC is limited to 7-8 bits, as shown in Fig. 14 by the variation in the LSB currents. In order not to limit the overall linearity to that of the IDAC, a dynamic element matching (DEM) technique is implemented, allowing to achieve a larger input-output system linearity.

B. Sensor Readout Characterization

In sensor interface applications, the signal generally varies extremely slowly compared to the system sampling frequency, therefore it can be considered as a DC input signal for the system. Hence, the sensor readout interface is characterized for its static rather than its dynamic performance.

1) System Resolution: Depending on the number of PMOS units activated in the VCO and the externally set variable $\mathrm{cnt}_{\mathrm{ref}}$, the chip can operate in a slow and a fast sampling mode. The former operating mode features a slower sampling clock frequency and a larger average number of VCO periods per clock cycle than the latter. Being a sensor interface, the system input consists of a DC value, more specifically a resistor. As done in [26], the effective resolution of the overall sensor interface is obtained by calculating the integrated noise of the digital output bitstream PSD (Power Spectral Density) when applying a constant sensor input value. The PSD is normalized with respect to the full-scale digital output. The resolution on the resistance measurement can be calculated roughly as $\mathrm{R_p}/2^{\mathrm{ENOB}}$, as $\mathrm{R_p}$ is the full-scale resistive input value.

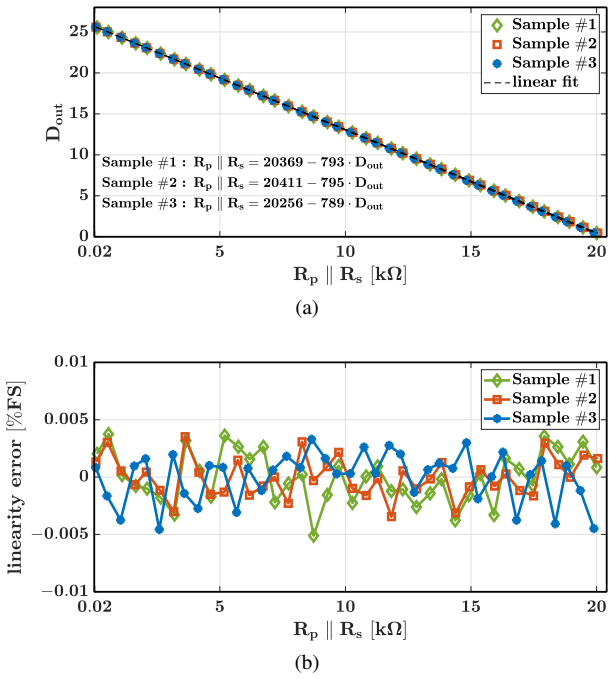

Fig. 17. Measured system input-output characteristic (a), and output error (b) as calculated using the fitted linear equation shown in (a). These measurements have been performed at room temperature.

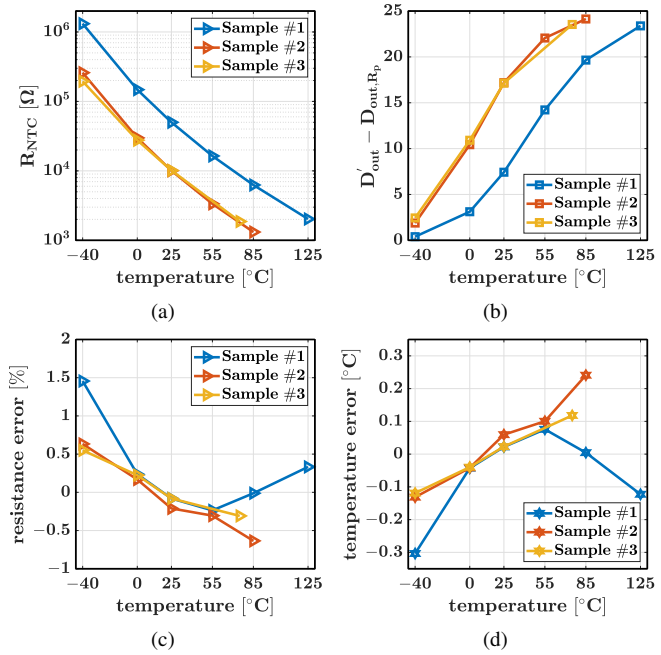

Fig. 18. Measured NTC characteristic as a function of temperature (a) and corresponding digital output (b), and relative resistor error with respect to the NTC characterization (c) and the corresponding temperature error (d).

Fig. 15(a) shows the measured output spectrum normalized to the full-scale digital output [26] of the sensor interface in the fast sampling mode, where $f_s = 1.8$MHz and all 4 VCO PMOS units activated. Since $\mathrm{cnt}_{\mathrm{ref}}$ is set to 2 in this mode, *Loop 2* cannot be activated[1], resulting in 1st-order noise

[1]*Loop 2* requires at least eight VCO periods in each sampling period to operate properly, leading to the requirement $\mathrm{cnt}_{\mathrm{ref}} \geq 8$ (see Fig. 2).

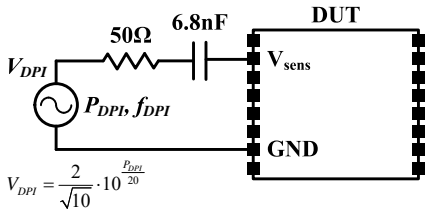

Fig. 19. DPI measurement test setup.

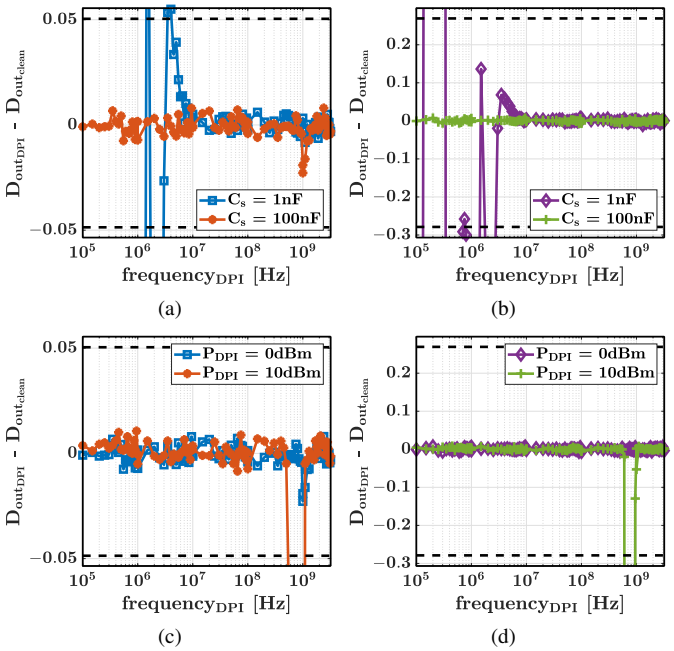

Fig. 20. DPI measurement results for $P_{\mathrm{DPI}} = 0$dBm with C_s equal to 1nF and 100nF for R_s equal to 1kΩ (a) and 100kΩ (b). DPI measurement results for P_{DPI} equal to 0dBm and +10dBm with $C_s = 100$nF for R_s equal to 1kΩ (c) and 100kΩ (d).

shaping only. A resolution of 16.1 bits is achieved in 1ms conversion time (Fig. 15(b)), while consuming 171µW. The 1/*f* noise from the VCO and the IDAC limit the performance for a long conversion time, as shown in Fig. 15(b). On the other hand, the normalized FFT plots of the measured bitstream output in slow sampling mode, $f_s = 210$kHz and only one VCO PMOS unit activated, are shown in Fig. 16(a) and 16(b). Since $\mathrm{cnt}_{\mathrm{ref}} = 8$, *Loop 2* can be activated: when only *Loop 1* is active, 1st-order noise shaping is achieved, while 2nd-order is obtained when also activating *Loop 2*. In the quantization-noise-limited region, the 2nd-order quantization noise shaping mode indeed achieves a higher resolution for the same conversion time compared to the 1st-order mode with the same settings, as shown in Fig. 16(c). The chip consumes 138µW and 145µW from a 1.8V supply in the two configurations (1st-order and 1-1 SMASH), respectively. The power spectral densities have been measured for three random chip samples, showing a very similar performance concerning their system noise floor.

2) Linearity and Calibration: In order to characterize and calibrate the prototypes, a SourceMeter (see Fig. 12) has been employed to sink current from the sensor node V_{sens} and at the same time measure the voltage. This method allows to

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH THE STATE OF THE ART.

	This work	JSSC13 [25]	JSSC13 [20]	ISSCC18 [22]	ISSCC17 [23]	JSSC19 [26]	VLSI19 [19]	ISSCC19 [21]	ISSCC18 [24]
Topology (-based)	**time (count)**	time (PLL)	time (count)	time (FLL)	time (FDC)	time (PLL)	time (PWM+GRO)	amplitude (CTSDM)	amplitude (SAR)
Sensor type	**external resistor**	external resistor	external resistor	internal p-resistor	internal VCO	external resistor	external resistor	internal p-resistor	external resistive bridge
Technology (nm)	**180**	130	180	65	180	180	110	180	180
Area$_{core}$ (mm^2)	**0.064**	0.2	0.18	0.007$^{\triangleright}$	0.22$^{\triangleright}$	0.26	0.02	0.12$^{\triangleright}$	1.7
Power$_{core}$ (µW)	**171**	125	13101	68	0.57	3410	152.3	79	2.65
t$_{conv}$ (ms)	**0.2** | **1**	0.05	100	1	8	0.014	5	10	1
ENOB	**14.5**† | **16.1**†	8.9†	18.5††	13.6††	8.3††	9.9†	15.67	18.3††	7.9†
Temp. range (°C)	**-40–125**	-20–80	-40–85	-40–85	-20–100	-40–175	- -	-55–125	- -
Inaccuracy (°C)	**0.3**$^{\star,\diamond}$	0.56$^{\star,\diamond}$	- -	±0.35$^{\star\star,\diamond\diamond}$	0.76$^{\star,\diamond\diamond}$	- -	- -	±0.14$^{\star\star,\diamond\diamond}$	- -
FOM$_W$* (pJ/c.s.)	**1.48** | **2.4**	13.03	3626	5.27	14.21	50	14.6	2.43	11.25
FOM$_S$$^+$ (dB)	**160.7** | **163.5**	134.4	138.7	152.6	132.3	131.5	154.2	170	131.9

$^{\triangleright}$sensing element on chip, †from integrated noise, †† $\mathrm{SNR} = 20\log\left(\frac{\mathrm{T_{range}}}{2\sqrt{2}\mathrm{T_{res}}}\right)$, *min or max, $^{\star\star}3\sigma$, $^{\diamond}$1-point trimming, $^{\diamond\diamond}$2-point trimming,

$^{*}\mathrm{FOM_W} = \frac{\mathrm{Power}\cdot\mathrm{t_{conv}}}{2^{\mathrm{ENOB}}}$, $^{+}\mathrm{FOM_S} = \mathrm{SNR} + 10\log\left(\frac{1}{2\cdot\mathrm{Power}\cdot\mathrm{t_{conv}}}\right)$

emulate the variation of a resistive sensor in an automated and controlled way. The input-output characteristics shown in Fig. 17(a) have been obtained from these measurements. Using the best linear fit, the linear input-output equation (also indicated in the graph) has been calculated for each prototype, as in (3). From the system equation in Fig. 17(a), it is possible to identify the value of $R_{\mathrm{p}} \approx 20\mathrm{k}\Omega$ as offset, and the value of $R_1 \approx 25\mathrm{k}\Omega$ as 32 times the gain. The prototypes have been characterized fully at room temperature (RT), resulting in a cheap and efficient single-point trimming calibration. The three chip samples shown in Fig. 17 present similar performance, achieving more than 14 bits of linearity (see Fig. 17(b)).

C. NTC Thermistor Measurements

Two different commercial NTC thermistors [36] and [37] have been used as external sensors to perform temperature measurements in a temperature-controlled environment by means of a ThermoStream, as shown in Fig. 12. Fig. 18(a) shows the measured sensor values over the temperature range. The first NTC thermistor [36] has a RT resistive value $\mathrm{R_{NTC,25}}$ equal to $50\mathrm{k}\Omega$, while the second NTC thermistor [37] is characterized by $\mathrm{R_{NTC,25}} = 10\mathrm{k}\Omega$. In Fig. 18(b) the digital output as a function of temperature is shown when these NTC thermistors are connected as input to the proposed sensor interface. The chip is functional across the entire automotive temperature range (from $-40°\mathrm{C}$ to $125°\mathrm{C}$). Using (3) and the coefficients of the room-temperature characterization from Section IV-B2, the sensor values R_{s} have been calculated for the three chip samples. The calculated sensor values are compared to the NTC thermistor characterization data shown in Fig. 18(a) The corresponding relative resistance error is plotted in Fig. 18(c). From the latter, the temperature error is calculated according to [36] and [37], which is both temperature- and sensor-dependent. The maximum measured temperature inaccuracy is only $\pm 0.3°\mathrm{C}$ across the entire temperature range (Fig. 18(d)), while the readout circuit is calibrated only at room temperature.

D. DPI Measurements

Since the automotive industry requires robust solutions, also when using external resistive sensors, high EMI (Electro-Magnetic Interference) immunity is an important requirement. Therefore, low-pass filtering needs to be added at the sensor readout input node. When using traditional interfaces (e.g. Wheatstone bridge [25]), the sensor element is inside the feedback path of the closed-loop VCO-based interface. This limits the amount of low-pass filtering that can be applied, while still ensuring the correct operation of the system. Thanks to the proposed architecture, the current flowing through the external resistive sensor R_{s} is constant, independently of the digital output D_{out} of the modulator, and equal to the overall IDAC current, as shown in Fig. 8. Since the proposed architecture decouples the sensor excitation mechanism from the feedback path, a larger low-pass filtering is allowed, increasing the EMI immunity without interfering with the operation of the system. This is achieved by adding extra capacitance C_{s} to the input node.

Fig. 20 shows the measurement results of the DPI (Direct Power Injection) test, which is one of the most applied EMC immunity tests for ICs. The DPI measurement setup is shown in Fig. 19. Fig. 20(a) and Fig. 20(b) show the measurement results for the same injected power level P_{DPI} for different capacitor values C_{s} and different values of R_{s}. The system

digital output is compromised by low-frequency interference for small capacitor values, while it is recovered for larger values, which is possible thanks to the proposed architecture. Fig. 20(c) and Fig. 20(d) show the measurement results with the large C_{s} of $100\mathrm{nF}$ for different injected power level P_{DPI} and for different values of R_{s}. The prototype chip operates correctly with an injected power level of $+10\mathrm{dBm}$, satisfying the requirements. The horizontal black dashed lines in the plots in Fig. 20 indicate the range of variation on the digital output corresponding to $\pm 1^{\circ}\mathrm{C}$ temperature error.

E. Comparison to the State of the Art

In Table I, the measured sensor interface performance is summarized and compared to the state of the art. The presented system compares favorably to other time-based solutions [22], [23], [25], [26], [20]: it achieves a high resolution up to 16.1 bits for a low conversion time in a small area footprint. Overall, it achieves the best FOM values (both $\mathrm{FOM_W}$ and $\mathrm{FOM_S}$) among all reported time-based solutions. This chip also achieves a better $\mathrm{FOM_W}$ value compared to recent state-of-the-art sensor readout circuits that use a conventional amplitude approach [21], [24] (right two columns in Table I), while offering a more digital, therefore smaller and process-scalable solution.

V. Conclusion

This paper has presented a novel VCO-based closed-loop resistive-sensor-to-digital interface that achieves an ultra-small energy-efficient time-based design with high resolution. Employing one oscillator, the architecture is suitable for the readout of single-ended highly-nonlinear resistive sensors, such as NTC thermistors. The 2^{nd}-order noise shaping property has been demonstrated in a 1-1 SMASH closed-loop time-based system. The highly-digital architecture allows to synthesize large portion of the design, resulting in a portable and technology-scalable solution. The design has been fabricated in a standard 180nm CMOS technology and occupies an active area of only $0.064\mathrm{mm}^2$. The chip consumes $171\mu\mathrm{W}$ from a 1.8V supply and achieves a resolution of 16.1 bits in 1ms conversion time, resulting in a 163.5dB $\mathrm{FOM_S}$. Trading resolution for bandwidth, the chip achieves 14.5 bits in 0.2ms conversion time, leading to a 1.48pJ/c.s. $\mathrm{FOM_W}$. These are excellent FOM values for a resistive sensor readout interface.

The prototype has been tested with commercial NTC thermistors in a temperature-controlled environment across the entire automotive temperature range $[-40^{\circ}\mathrm{C};125^{\circ}\mathrm{C}]$. It is capable of converting sensor values from $\mathrm{k}\Omega$ to $\mathrm{M}\Omega$ with a maximum inaccuracy of only $0.3^{\circ}\mathrm{C}$, while requiring only room-temperature characterization. Finally, DPI measurements have shown a high EMI immunity. Compared to the state of the art, the proposed architecture achieves excellent sensor readout FOM values with an ultra small, robust and highly-scalable implementation.

Acknowledgment

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