# A 16.6 μW 3.12 MHz RC relaxation oscillator with 160.3 dBc/Hz FOM

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# A 16.6 μW 3.12 MHz *RC* Relaxation Oscillator with 160.3 dBc/Hz FOM

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***Abstract*—This paper presents a new *RC* relaxation oscillator for biomedical sensor interface circuit. A novel switch-capacitor based *RC* charging/discharging circuit is proposed to effectively improve the oscillator phase noise and power performance. The inverter-based comparator with replica biasing is employed and optimized to enhance the phase noise performance and to lower output dependence on the supply voltage variation. The oscillator's temperature insensitivity is also improved by resistor temperature compensation. The prototype *RC* relaxation oscillator circuit is designed in a commercial 65nm CMOS process. The post-layout simulation results showed 3.12 MHz output frequency, −112dBc/Hz phase noise at 100 kHz offset, and 16.6 μW power consumption under 1 V supply voltage. The frequency variation is ±0.294%/V for supply within 1 V to 1.6 V, and 11.31 ppm/°C for temperature across −40°C to 100°C. The overall circuit performance is compared favorably to the state-of-art designs, with an outstanding Figure of Merit (FOM) of 160.03 dBc/Hz at 100 kHz.**

***Keywords—RC relaxation oscillator; low phase noise; high FOM; switch-capacitor; capacitor stacking***

## I. INTRODUCTION

The *RC* relaxation oscillator has become a topic of interest for System-On-Chip in recent years. While it can be implemented as an on-chip clock/timing signal generator [1] [2], it can also be used as the frontend of wearable biomedical sensor system [3]. The *RC* relaxation oscillator provides a direct conversion from sensor's resistance or capacitance value to frequency for easy digitization [3]. As the frontend of the readout circuit, the *RC* relaxation oscillator should achieve reliable conversion result, which translates to design challenges of low output phase noise, low power consumption, and low frequency sensitivity to the supply and temperature variation.

Many *RC* relaxation oscillators had been reported to meet these design challenges. To improve the oscillator output phase noise performance, a voltage swing boosting technique is proposed in [4] to achieve outstanding phase noise performance. An anti-jitter technique by subtracting a fixed charge packet to remove the comparator noise is designed in [5] to achieve excellent phase noise performance too. However, the trade-off for good phase noise is the additional power consumption, either from having high voltage swing or deploying low noise output comparator. Meanwhile, the supply variation alters circuit delay, so does the oscillation frequency. To compensate this, oscillators with voltage averaging feedback (VAF) circuit [6] [7] are proposed to adjust the comparator switching threshold based on the actual circuit delay to lock the overall circuit delay. This feedback method effectively reduces the frequency variation with supply but compromises the phase noise and power performance. In addition, temperature variation causes changes in parameters such as *RC* value, switches matrix, comparator offset and comparator delay [8], resulting in frequency variation with temperature. To compensate this, temperature insensitive MIM capacitor together with temperature compensated resistor are implemented in [4][9][10]. [8] further proposed an optimized switch matrix and comparator offset cancellation with constant bandwidth comparator to effectively remove the temperature dependent factors from output frequency.

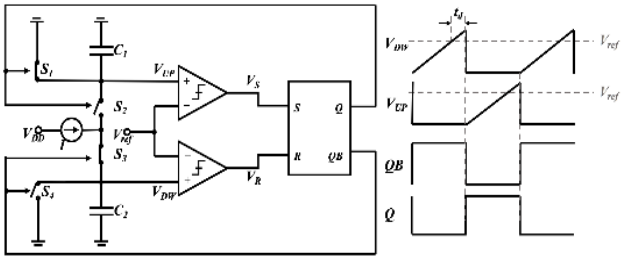


Figure 1: Classic RC relaxation oscillator with its timing diagram

In this work, a novel on-chip *RC* relaxation oscillator is proposed. Phase noise performance is ensured via the switch-capacitor-based voltage stacking method, while the frequency variation with supply and temperature is reduced by employing the inverter-based comparator with replica biasing and the resistor temperature compensation technique. The total power consumption is also reduced through the novel *RC* charging/discharging circuit and by eliminating comparator static power.

This paper is organized as follows. Section II presents the system architecture of the classic design and the proposed design while Section III provides details of the proposed design. Post-simulation results of the proposed design are presented in Section IV and this work is concluded in Section V.

## II. *RC* RELAXATION OSCILLATOR SYSTEM ARCHITECTURE

### *A. Architecture of the Classic Design*

The classic *RC* relaxation oscillator is illustrated in Fig. 1. The oscillation is achieved by charging/discharging timing capacitors $C_1$ and $C_2$ alternatively using the constant current

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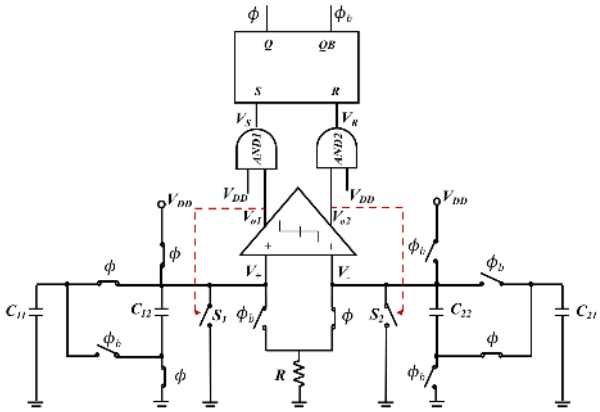


Figure 2: Proposed *RC* relaxation oscillator

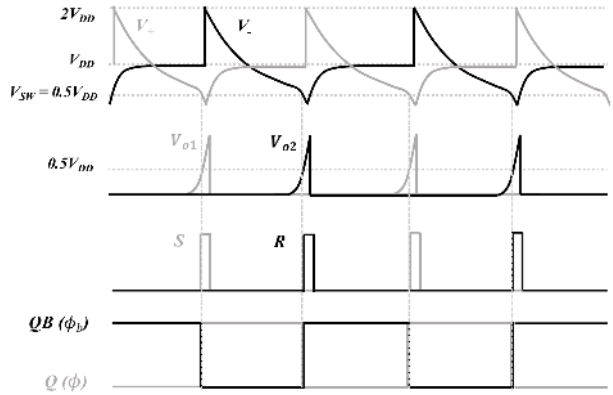


Figure 3: Timing diagram of proposed *RC* relaxation oscillator

source *I*. The slope of the timing waveform is fixed by this constant current source. [11] [12] show that the phase noise is inversely related to the slope and directly related to the noise source in series with timing capacitor. Therefore, for better phase noise performance, the classic design needs a large current source which increases the power consumption. On the other hand, the constant current source introduces additional noise source in series with timing capacitors, which is undesirable.

### *B. Architecture of the Proposed Design*

To improve the performance of the classic design, a new *RC* relaxation oscillator is proposed. The architecture of proposed *RC* relaxation oscillator and timing diagram are shown in Fig. 2 and Fig. 3, respectively. The proposed design consists of a novel *RC* charging/discharging circuit, an inverter-based comparator with replica biasing, a *SR* latch and some logic buffers.

The basic operation of the proposed design is described as follows. Setting the initial state of $V_-$ = $V_{DD}$ and $V_+$ = *GND*, the inverter-based comparator and logic gates give $V_S$ = $V_{DD}$ and $V_R$ = *GND*, which triggers the *SR* latch to output $Q$ = $V_{DD}$ and $QB$ = *GND*. These two complimentary signals set the switch matrix of the *RC* charging/discharging block to that shown in Fig. 2. With this switch configuration, capacitor $C_{11}$ and $C_{12}$ are connected in parallel for charging, pushing $V_+$ to $V_{DD}$, while capacitor $C_{21}$ and $C_{22}$ are stacked together in series, pushing $V_-$ to $2V_{DD}$ as $C_{21}$ and $C_{22}$ are both charged to $V_{DD}$ before stacking. The stacked $C_{21}$ and $C_{22}$ are then discharged immediately via resistor $R$ toward the ground, pulling $V_-$ down from $2V_{DD}$.

When $V_-$ drops to the comparator switching point $V_{SW}$, comparator output $V_{o2}$ starts to increase. The increasing $V_{o2}$ turns on switch $S_2$ when it is about to trigger the next logic toggling. This further steepens the discharging slope of $V_-$ by pulling $V_-$ to the ground directly and thus, enhances the oscillator overall phase noise performance. The faster decrease of $V_-$ also causes a faster increase of $V_{o2}$, which crosses the following logic gates with a steeper edge after a negligible time delay. Therefore, $V_R$ is set to $V_{DD}$ while $V_S$ is kept at GND as $V_+$ = $V_{DD}$. As a result, the *SR* latch toggles its outputs $Q$ and $QB$. The new states of $Q$ and $QB$ reconfigure the switch matrix in *RC* charging/discharging block, stacking $C_{11}$ and $C_{12}$ together while re-charging the paralleled $C_{21}$ and $C_{22}$ to $V_{DD}$. The whole process

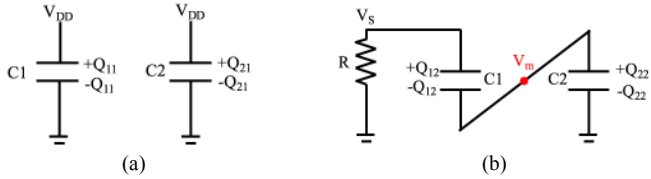


Figure 4: (a) *RC* network during charging phase (b) *RC* network during discharging phase

iterates, resulting in a 50%-duty-cycle square wave outputs at $Q$ and $QB$ with a theoretical frequency of

$$f_{osc} = \frac{1}{-2RC_{eq}\ln(0.5k)} \tag{1}$$

where $C_{eq}$ = $(C_{11}C_{12})/(C_{11}+C_{12})$ = $(C_{21}C_{22})/(C_{21}+C_{22})$ and $k$ = $V_{SW}/V_{DD}$. As the comparator is inverter-based, $V_{SW}$ is designed to be $0.5V_{DD}$ by selecting proper aspect ratio for input transistors. Therefore, $k$ is theoretically independent of $V_{DD}$. However, $f_{osc}$ will still vary with $V_{DD}$ due to the supply-dependent comparator delay and logic stage delay, with the comparator delay being the dominant factor based on simulation. To compensate this, suitably large input transistors are chosen for the comparator to minimize the delay effect on $f_{osc}$.

The proposed architecture has the following advantages. The stacked capacitors boost the voltage swing and increase the waveform slope at $V_+$ and $V_-$ for a better phase noise performance. The proper combination of capacitance in RC block cuts down the power consumption. On the other hand, the inverter-based comparator with replica biasing improves the phase noise performance by having a small input-referred noise and at the same time, enhances the frequency insensitivity to supply voltage changes. More details are provided in the following section.

## III. Main Circuit Blocks of the Proposed RC Relaxation Oscillator

### *A. The Switch-Cap based RC Charging/Discharging Circuit*

During the charging phase, the *RC* network is connected as that shown in Fig. 4(a). The total charging capacitance $C_p$ = $C1+C2$ and both capacitors are charged to $V_{DD}$. During the

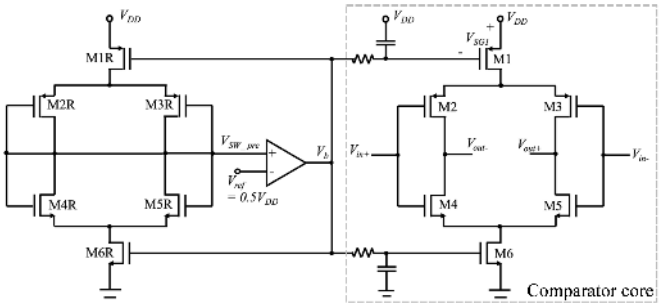

Figure 5: Inverter-based Comparator with replica biasing circuit

discharging phase, as shown in Fig. 4(b), the total discharging capacitance $C_S = (C1C2)/(C1+C2)$, and $V_S = 2V_{DD}$ initially. $C_S$ then discharges via resister $R$, and $V_S$ starts to drop until it crosses the comparator's switching threshold $V_{SW}$ to initiate another round of toggling.

The proposed $RC$ charging/discharging circuit replaces the constant charging/discharging current source by a passive resistor $R$. Although both current source and resistor add current noise directly to the discharging waveform, with the same amount of discharging current, it is shown that the passive resistor introduces less noise power as compare to the transistor current source[13], and therefore improves the circuit output phase noise performance.

On the other hand, the proposed $RC$ circuit optimizes the power consumption by making use of charge sharing between two capacitors. Referring to Fig. 4(b), comparator switches when $V_S = 0.5V_{DD}$, and at this point, since charges at $V_m$ conserved, $V_m$ is derived as

$$V_m = (1.5x - 0.5)V_{DD} \tag{2}$$

where $x = C2/(C1+C2)$. Without changing the value of $C_p$, the power consumption will then depend on how many chargers need to be re-pumped into $C1$ and $C2$ after discharging, or during the charging phase. This will essentially be decided by the values of $C1$ and $C2$. Using (2), the additional charges to be added to $C1$ and $C2$ after discharging phase can be estimated and suitable values of capacitors can be determined to reduce the power. The proposed circuit uses $C1 = 0.1(C1+C2)$ and $C2 = 0.9(C1+C2)$. It can be calculated that the total discharging capacitance for this 10%-90% case is 2.78× smaller than that in the 50%-50% case, which will result in a different output frequency. Therefore, for comparison purpose, the power to frequency ratio is computed. Based on the schematic simulation, the ratio for the 10%-90% case is 2.144 µW/MHz and for the 50%-50% case, it is 4.082 µW/MHz, ceteris paribus, which verifies that the capacitor combination can be optimized to improve the power efficiency.

Furthermore, to compensate the temperature dependency of the resistor, both HR poly and N+ diffusion resistors are used. Based on simulation, the resistance variation of HR poly resistor and N+ diffusion resistor is -0.037%/°C and 0.123%/°C, respectively, for temperature range of –45°C to 125°C. The resistive temperature compensation is achieved by combining them to minimize the 1st order temperature dependency of the frequency on resistor.

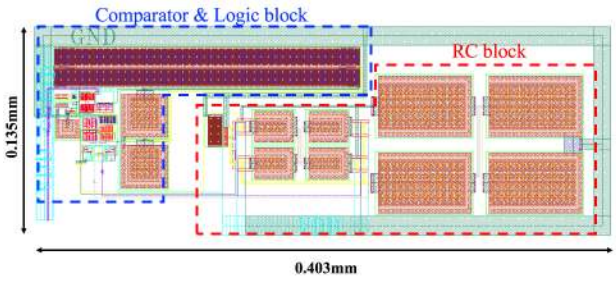

Figure 6: Layout of the proposed circuit

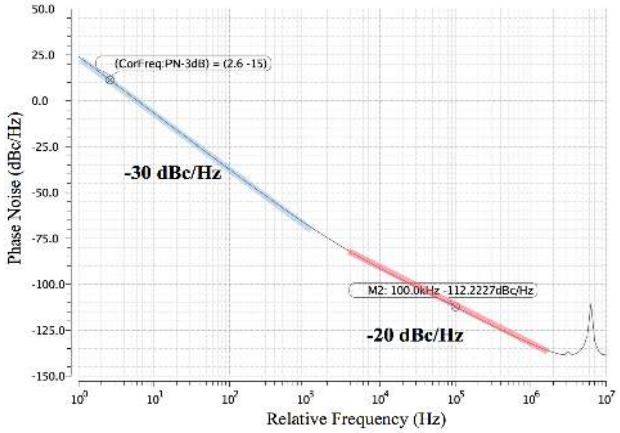

Figure 7: Phase noise plot of proposed circuit

### B. *The Inverter-based Comparator with Replica Biasing*

Instead of employing the conventional differential-pair comparator, an inverter-based comparator with replica biasing, similar to [4], is adopted in this design as shown in Fig. 5. It consists of a replica biasing circuitry and a comparator core.

As the comparator core is inverter-based, it only turns on when the input is near the comparator switching point. Therefore, the static power consumption is eliminated, and the input transistors can thus be scaled up for a smaller comparator delay without having too much penalty on the power consumption. Meanwhile, with larger transistor sizes, the transistor flicker noise, which is referred back to the comparator input, is reduced too. On the other hand, as the inverter-based input pair has a larger $g_m$ than that of the single transistor input pair, the comparator input-referred noise is reduced. Moreover, to further compensate the comparator delay variation with $V_{DD}$, the replica biasing circuit with feedback amplifier [14] is deployed to regulate the comparator current under different $V_{DD}$, thus reduces the output $f_{osc}$ dependence on $V_{DD}$.

## IV. Post-Layout Simulation Results

The proposed circuit has been designed and simulated in a standard commercial 65 nm CMOS process. The chip layout is shown in Fig. 6. Under typical condition of 1 V supply and 27°C, the entire circuit consumes an average power of 16.6 µW and the nominal output frequency is 3.12 MHz.

TABLE I. PERFORMANCE COMPARISON

| Year | 2008 [5] | 2009 [16] | 2010 [15] | 2013 [7] | 2016 [8] | 2016 [4] | **This work** |
|---|---|---|---|---|---|---|---|
| Technique | Switch-cap | Auto-zeroing | Feedback +chopped Amplifier | Feedback +chopping FLL | Offset cancellation | Swing-boosting | **Stacked capacitor** |
| Technology | 65nm | 0.13um | 65nm | 65nm | 65nm | 0.18um | **65nm** |
| Power (μW) | 91/~3600 | 38 | 100 | 98.4 | 0.13 | 219.8 | **16.6** |
| Chip area ($mm^2$) | 0.03 | 0.073 | 0.02 | 0.01 | 0.032 | 0.015 | **0.055** |
| Frequency (MHz) | 12.5 | 3.2 | 6 | 12.6 | 0.0185 | 10.5 | **3.12** |
| Supply (V) | 1.3 | 1.4 | 1.25 | 1.1 | 1 | 1.4 | **1** |
| Frequency Variation with $V_{DD}$ (%/V) | N.A. | ± 0.4 @1.4 - 1.6V | ± 0.26 @1.15 - 1.35V | ± 0.07 @ 1.1 - 1.5V | ± 0.2 to ± 2.5 @ 0.95 - 1.05V | ± 0.44 @ 1.4 - 2V | **± 0.294 @ 1 - 1.6V** |
| Temp. Range (°C) | N.A. | 20 to 60 | –40 to 125 | 0 to 80 | –40 to 90 | –40 to 125 | **–40 to 100** |
| Frequency Variation with Temp. (ppm/°C) | N.A. | 125 | 24 | 205 | 27.7 to 42.3[a] | 137 | **11.31** |
| FOM (dBc/Hz) | 162 @100kHz | 132 @10kHz | 137.6 @1kHz | 152.6 @100kHz | N.A. | 162.1 @100kHz | **160.03 @100kHz** |

[a] Calculated from original reported data of ± 0.18% to ± 0.55%

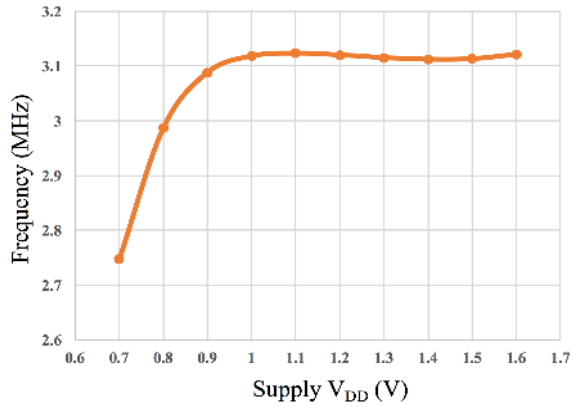

Figure 8: Frequency variation with supply voltage of proposed circuit

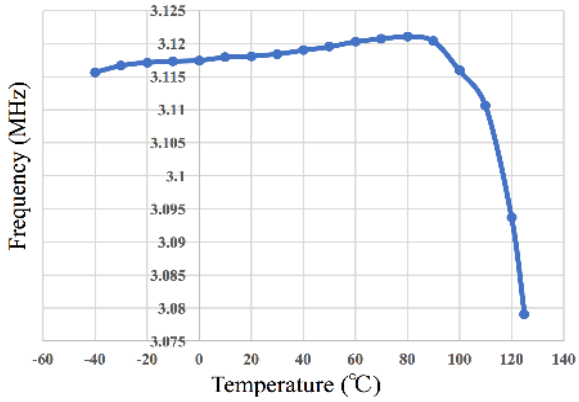

Figure 9: Frequency variation with temperature of proposed circuit

The phase noise performance of oscillator output is shown in Fig. 7. At 100 kHz offset frequency, the simulated phase noise value is 112.2 dBc/Hz. The oscillator output FOM is calculated as

$$FOM = 10\log\left[L(f_{-2})\cdot\left(\frac{f_{-2}}{f_{osc}}\right)^2\cdot\left(\frac{P_{total}}{1mW}\right)\right]. \quad (3)$$

Using (3), the FOM for the proposed circuit is 160.03 dBc/Hz, which is favorably comparable to the benchmark value of 162.1 dBc/Hz.

The output frequency variation with respect to supply voltage is shown in Fig. 8. For a range of 1 V to 1.6 V, the output frequency variation is calculated as ±0.294%/V, which is closed to the performance of [15]. The output frequency variation with temperature is shown in Fig. 9. The frequency variation for temperature range of –40°C to 100°C is 11.31 ppm/°C.

The performance of the proposed circuit and state-of-arts are summarized in Table 1. Compared to circuit in [4] with similar swing boosting idea, our circuit consumes 10× less power while oscillating at 4× smaller frequency. Furthermore, the frequency variation with supply and temperature is also closed to some conventional designs which trade off more phase noise performance and power consumption.

## V. CONCLUSION

In this work, an *RC* relaxation oscillator with novel *RC* charging/discharging circuit and inverter-based comparator with replica biasing is proposed for biomedical sensor readout application. It achieves an overall good performance in post-layout simulation with 160.03 dBc/Hz FOM, ± 0.294%/V frequency variation for supply between 1 V to 1.6 V, and 11.31 ppm/°C frequency variation for a temperature range of –40°C to 100°C.

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