A 16-bit Oversampling A-to-D Conversion Technology Using Triple-Integration Noise Shaping

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Abstract —**A highly stable triple-integration noise-shaping technology is discussed which permits greater accuracy for monolithic audio A-to-D converters. Based on this new technology, using 2-μm CMOS technology, a 16-bit 24-kHz bandwidth A-to-D converter LSI with digital filters was successfully developed. An SNR (S/(N+THD)) of 91 dB and a total harmonic distortion (THD) of 0.002 percent at full-scale input were attained.**

I. INTRODUCTION

IMPROVING the accuracy of monolithic A-to-D converters is a never-ending research goal because the A-to-D converter is a key component of electrical systems, such as high-quality audio and high-accuracy measurement systems.

Conventionally, either the successive approximation or dual-ramp conversion technique is used for high-resolution A-to-D converters. In successive approximation, a means of trimming the weighting network is indispensable to achieving a conversion accuracy of over 15 bits [1]–[3]. This is because the conversion accuracy depends on the device matching tolerance of the weighting networks and is limited to 14-bit accuracy when using nontrimming weighting networks [4], [5]. Using the dual-ramp technique, high speed and accuracy are required in the integrator, current sources, comparators, and sample-and-hold (S/H) circuits. To realize these circuits, high f_T bipolar process technologies must be used [6]. The development of an S/H circuit with over 16-bit accuracy is especially difficult, because the sampled charge in the sampling capacitor is leaked through the base impedance of the bipolar transistor.

Recently, oversampling has attracted considerable attention as a conversion technique for VLSI technology, which does not require trimming or a precise S/H circuit [7], [8]. The noise reduction concept of the noise-shaping oversampling technique is to distribute quantization noise outside the signal band by setting the sampling rate much higher than the signal bandwidth and the noise shaping by an integration. This technique thus has the advantage that the device tolerance is relaxed, and it is possible to use a two-value quantizer which theoretically produces no distortion. By using a higher frequency as the sampling clock pulse and higher order integration noise shaping characteristics, higher accuracy is achieved.

The conventional noise-shaping oversampling technique, however, is limited to an accuracy of 80 dB in the audio signal bandwidth with CMOS process technologies, which are useful for VLSI's [9], [10]. This limitation stems from the fact that higher order integration noise-shaping characteristics over double integration cannot be realized due to the oscillation of the feedback loop.

To overcome this problem, we have developed a multistage noise-shaping technique which permits higher order, more than double integration, noise-shaping characteristics by using a new multistage configuration based on a stable first-order Δ-Σ quantizer [11]. Hereafter, this technique will be referred to as MASH. To confirm the feasibility of the MASH technique, we fabricated the double-integration MASH A-to-D conversion LSI [12].

In this paper, the realization of higher order integration noise-shaping characteristics, which are the essential features of the MASH technique, and the usefulness of MASH as a high-accuracy, over 16-bit, A-to-D conversion technique, will be described. In Section II, the accuracy limitations of the oversampling technique are discussed. Also in Section II, the necessity of triple integration noise shaping characteristics to realize 16-bit accuracy (which is required for high-quality audio encoding) using CMOS process technology is shown. In Section III, the operating principle of the MASH technique is described, and it will be shown theoretically that high-order, more than triple

Manuscript received June 18, 1987; revised July 26, 1987.
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IEEE Log Number 8717214.

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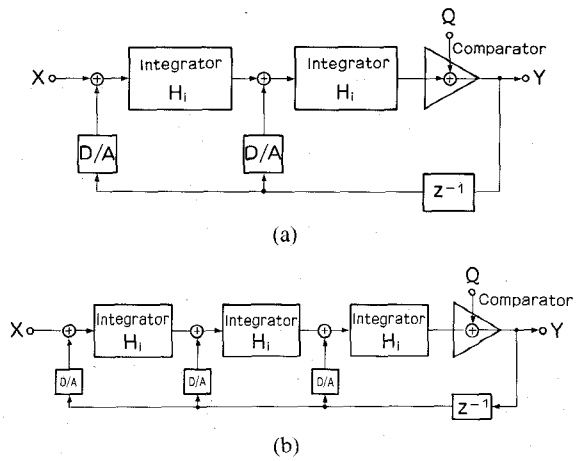

Fig. 1. (a) Conventional double-integration Δ-Σ quantizer signal flowchart. (b) Conventional triple-integration Δ-Σ quantizer signal flowchart.

integration, noise-shaping characteristics are easily realized. In Section IV, the practical accuracy limiting factors and the way these factors were optimized to realize the triple-integration MASH A-to-D converter are discussed. In Section V, the circuit configurations and operations of the developed 16-bit A-to-D conversion LSI with precise digital filters are described in detail. In Section VI, measurement results of the fabricated LSI with an SNR of 91 dB and a total harmonic distortion (THD) of 0.002 percent are presented. These results confirm the usefulness of MASH as a technique to enhance monolithic A-to-D converter accuracy.

II. The Theoretical Accuracy Limiting Factors of the Δ-Σ Oversampling Technique

In the Δ-Σ oversampling technique which uses noise shaping characteristics, theoretical accuracy limiting factors are 1) oversampling frequency, and 2) the order of the integration of noise-shaping characteristics.

Signal flowcharts of the double- and triple-integration Δ-Σ quantizer using cascade integrators are shown in Fig. 1 (a) and (b), respectively, where X is an analog input, Y is a digital output, and Q is a quantization noise [13]. The transfer function of an integrator H_i is defined by $1/(1-z^{-1})$. Therefore, the transfer functions of these signal flowchart are given by

$$Y = X + (1 - z^{-1})^2 Q \tag{1}$$

$$Y = X + (1 - z^{-1})^3 Q. \tag{2}$$

Fig. 2 shows the theoretical relationship between SNR and sampling frequency at the 24-kHz signal bandwidth. These are calculated using (1) and (2). To obtain better than 16-bit accuracy using double-integration noise-shaping characteristics, a sampling frequency of 6.6 MHz is required. If triple-integration noise-shaping characteristics are realized, the sampling frequency can be reduced to 2.0 MHz.

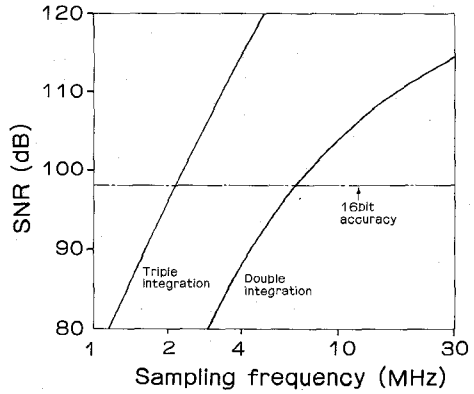

Fig. 2. Theoretical relationship between SNR and the sampling frequency.

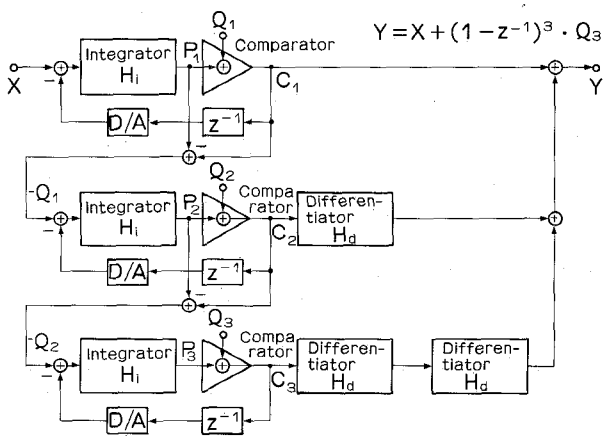

Fig. 3. Three-stage MASH signal flowchart.

Using a CMOS switched-capacitor integrator, the maximum sampling frequency for high-accuracy integration is about 4 MHz [14], [15].

Even with low sampling frequencies under 4 MHz, 16-bit accuracy can be attained using triple-integration noise-shaping characteristics, but not with double-integration noise-shaping characteristics.

III. Principle of the Three-Stage MASH Operation

To realize an over 16-bit accuracy CMOS oversampling A-to-D converter, a triple-integration noise-shaping technique is required. However, the loop of the conventional triple integration Δ-Σ quantizer, as shown in Fig. 1(b), which includes a three-stage cascade integrator, oscillates because of a 270° phase shift.

Therefore, to realize stable triple-integration noise-shaping characteristics without the oscillation problem, a three-stage MASH configuration using stable first-order Δ-Σ quantizers (DSQ) was proposed. Fig. 3 shows a signal flowchart of this three-stage MASH. The analog output of the first DSQ is given by $P_1 - C_1$, which is equal to the quantization noise $-Q_1$, and is quantized by the second DSQ. The analog output $P_2 - C_2$ of the second DSQ,

which is equal to the quantization noise $-Q_2$, is quantized by the third DSQ. When H_i is $1/(1-z^{-1})$, outputs of the first, second, and third DSQ's are given by (3)–(5):

$$C_1 = X + (1-z^{-1})Q_1 \tag{3}$$

$$C_2 = -Q_1 + (1-z^{-1})Q_2 \tag{4}$$

$$C_3 = -Q_2 + (1-z^{-1})Q_3. \tag{5}$$

Output Y of the three-stage MASH is synthesized C_1, C_2, and C_3. C_2 is differentiated one time, C_3 is differentiated two times, and these are added to C_1. Thus, when $H_d = (1-z^{-1})$:

$$\begin{aligned} Y &= C_1 + (1-z^{-1})C_2 + (1-z^{-1})^2 C_3 \\ &= X + (1-z^{-1})Q_1 - (1-z^{-1})Q_1 + (1-z^{-1})^2 Q_2 \\ &\quad - (1-z^{-1})^2 Q_2 + (1-z^{-1})^3 Q_3 \\ &= X + (1-z^{-1})^3 Q_3 \end{aligned} \tag{6}$$

Since quantization noise Q_1 can be suppressed by C_2 and Q_2 can be suppressed by C_3, (6) is equivalent to (2). The important point is that triple-integration noise-shaping characteristics can be obtained using three first-order Δ-Σ quantizers. This ensures stable operation.

The analog quantization noise Q_1 and Q_2 of $P-C$ for the next stage is generated easily without the analog subtractor. This operation is discussed in Section V.

IV. Practical Accuracy Limiting Factors

Practical factors limiting conversion accuracy are the integrator gain, the settling speed, the capacitance tolerence, and the noise from the digital circuits.

A. The Integrator Gain and Settling Speed

In Section II it was shown that 16-bit accuracy can be obtained by triple-integration noise-shaping characteristics and CMOS process technology at a sampling frequency of 2.0–4.0 MHz. Based on this range, we selected a sampling frequency f_s of 3 MHz, which can easily generate the 48-kHz data output rate by $f_s/64$ for the 24-kHz signal bandwidth.

The integration gain accuracy G_e, which is defined as V_o/V_{oi} (V_o: actual integrator output value; V_{oi}: ideal integrator output value), results from the finite amplifier gain of the integrator. This is because the virtual *GND* voltage, which is the negative input at the amplifier of the integrator, is varied depending on the integrator output voltage. When the amplifier gain is defined as $G_i (G_i = V_o/V_g$; V_o: amplifier output voltage; V_g: virtual *GND* voltage), G_e is given by

$$G_e = 1 - \frac{1}{G_i + 1}. \tag{7}$$

To define the settling accuracy of the integrator as G_s, the output of the integrator P is given by

$$P = G_e \cdot G_s (X + Pz^{-1}). \tag{8}$$

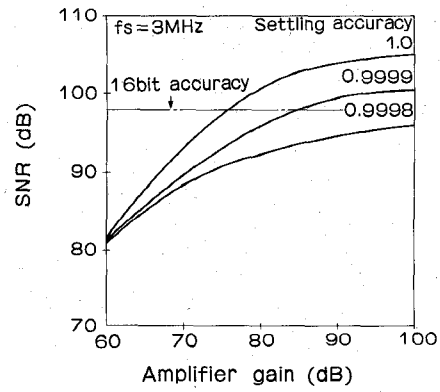

Fig. 4. SNR dependence on amplifier gain.

For the MASH configuration, the analog input and the feedback D/A output must be integrated individually. Therefore, the integrator is operated twice in each conversion operation. When the feedback D/A output is defined as D_a, the transfer function of the integrator considering integrating operations of two times is given by

$$P = G_e \cdot G_s \left(D_a + G_e \cdot G_s (X + Pz^{-1}) \right)$$

$$P = \frac{G_e \cdot G_s \cdot D_a}{1 - (G_e \cdot G_s)^2 z^{-1}} + \frac{(G_e \cdot G_s)^2 X}{1 - (G_e \cdot G_s)^2 z^{-1}} \tag{9}$$

Fig. 4 shows the SNR dependence on the amplifier gain at a settling accuracy of 1.0, 0.9999, and 0.9998 calculated by the three-stage MASH signal flowchart and (9). To obtain 16-bit accuracy at a 3-MHz sampling frequency, a gain of more than 85 dB and a settling accuracy of more than 0.9999 is required.

Focusing on the speed, the high-speed and low-distortion amplifier for the integrator is designed as shown in Fig. 5(a). It consists of two stages: a differential stage and a push–pull output stage. The measured characteristics of the amplifier are summarized in Table I. Where V_{dd} is 5 V, the input signal swing is 2 V_{pp}, the input signal frequency is 1 kHz, the bandwidth for SNR measurement is 24 kHz, and the output swing for settling time measurement is 0.5 V. These characteristics are all satisfactory except for the gain, which was only 82 dB. To boost the gain, it was necessary to improve the integrator.

Usually, a switched-capacitor integrator is used for the Δ-Σ quantizer, as shown in Fig. 5(b), because its accuracy depends on only capacitance-matching tolerance. The integration gain accuracy G_e of the switched-capacitor integrator is defined as $Q_i/(Q_i + Q_s)$ (Q_i: charge integrated in C_i; Q_s: charge remaining in C_s). $Q_i/(Q_i + Q_s)$ is given by

$$\frac{Q_i}{Q_i + Q_s} = \frac{C_i (V_o - V_g)}{C_i (V_o - V_g) + C_s \cdot V_g} \approx 1 - \frac{1}{\frac{C_i}{C_s} G_i + 1}. \tag{10}$$

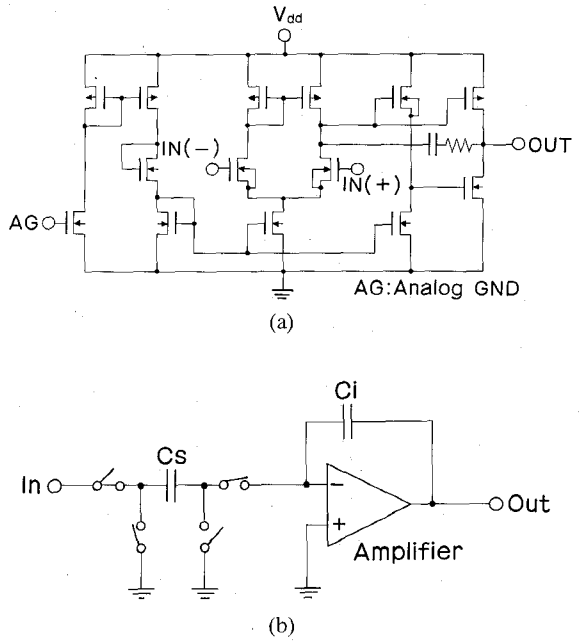

Fig. 5. (a) Configuration of the amplifier circuit. (b) Configuration of the integrator.

TABLE I
AMPLIFIER CHARACTERISTICS

Gain	82 dB
OdB bandwidth	47 MHz
THD	0.0003 %
S/N	105 dB
Settling time (0.01%)	100 ns
Power Dissipation	8.5 mW

Setting the capacitance ratio between the integrator capacitance C_i and the sampling capacitance C_s to 2:1, the amplifier gain considering C_i and C_s $(G_i \cdot C_i/C_s)$ is improved to 88 dB. Using this design, a gain of 88 dB and an SNR of 99 dB were attained—values that are high enough to achieve 16-bit accuracy.

B. Capacitance-Matching Tolerance

A gain mismatching of each DSQ causes the degradation of SNR. The gain of each DSQ is defined as digital output of the comparator/analog input. C_1, C_2, and C_3, shown in Fig. 3, are the ideal digital output at the DSQ gain of 1. αC_1, βC_2, and γC_3 are defined as the digital outputs at the DSQ when the DSQ gain is not equal to 1. Inserting αC_1, βC_2, and γC_3 into (6), we have the following equation:

$$\begin{aligned} Y &= \alpha C_1 + \beta(1-z^{-1})C_2 + \gamma(1-z^{-1})^2 C_3 \\ &= \alpha X + (\alpha-\beta)(1-z^{-1})Q_1 + (\beta-\gamma)(1-z^{-1})^2 Q_2 \\ &\quad + \gamma(1-z^{-1})^3 Q_3. \end{aligned} \tag{11}$$

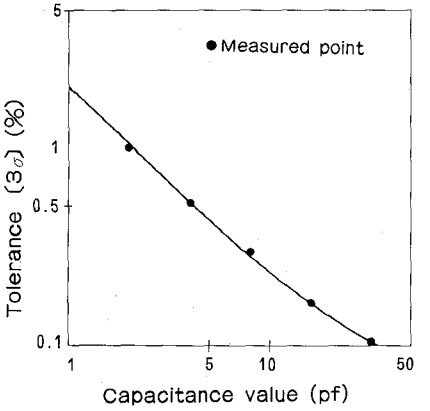

Fig. 6. Relationship between tolerance and capacitor value.

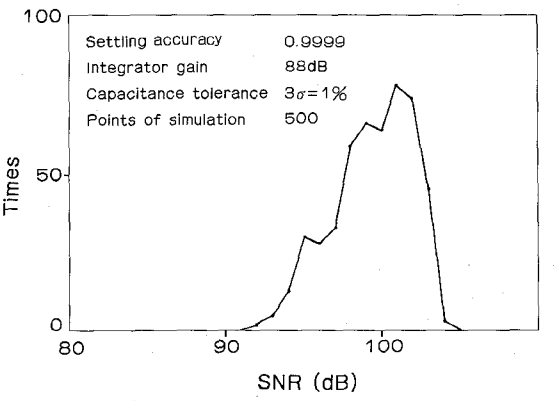

Fig. 7. Monte-Carlo simulated SNR results.

As can be seen from this equation, quantization noises Q_1 and Q_2 are not suppressed by the gain mismatching of each DSQ. This gain mismatching is caused by the capacitance ratio mismatching of C_i to C_s.

The measured tolerance (3σ) dependence on the capacitance value [5] is shown in Fig. 6. Considering the parasitic capacitor, the circuit noise, and the integrator settling speed, a capacitance value of 2 pF is suitable. At this value, the capacitance tolerance is about 1 percent at 3σ.

The SNR Monte-Carlo simulation results of the three-stage MASH A-to-D converter at a capacitance mismatching of 1 percent (3σ) among C_s, C_i, C_{d1}, and C_{d2} of each DSQ, an amplifier gain of 88 dB, and a settling accuracy of 0.9999 are shown in Fig. 7. From these results, an SNR of 99 dB occupies 67 percent and an SNR of 92 dB occupies 99.7 percent.

C. Reducing Noise from the Digital Circuits

The noise of the first-stage input is not noise shaped and must therefore be kept low. The main noise sources are the induced noise from the digital circuits and the $1/f$ noise of the integration amplifier. Using a wide gate area transistor of 2700 μm^2 as the amplifier input, an amplifier SNR of 105 dB is achieved. To reduce noise from the digital circuits, a differential configuration is adopted at the first DSQ, which can suppress the common-mode noise.

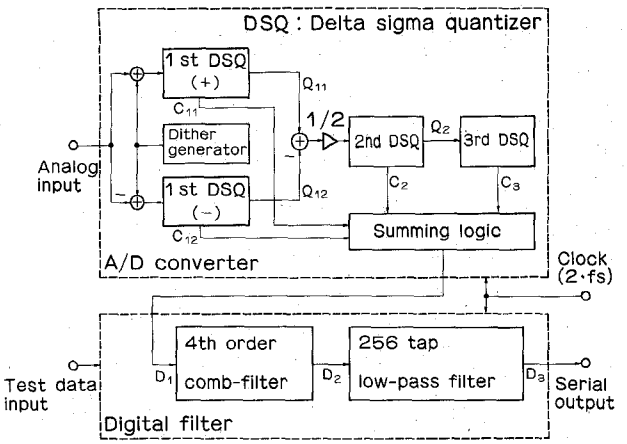

Fig. 8. Block diagram of the A-to-D conversion LSI.

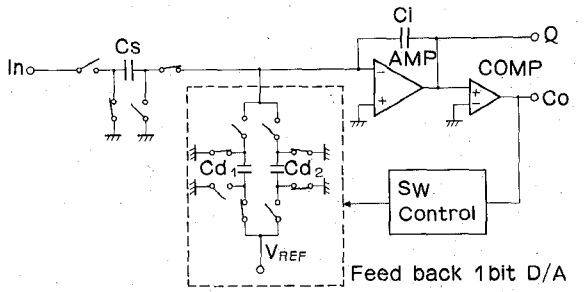

Fig. 9. DSQ configuration.

V. Circuit Configuration

By incorporating the various optimizations discussed above in Section IV, we designed a three-stage MASH A-to-D conversion LSI with digital filters. In this section, we will describe the LSI configuration and circuit operations in some detail.

A. Block Diagram

A block diagram of the A-to-D conversion LSI is shown in Fig. 8. It consists of an A-to-D converter using three-stage MASH, a fourth-order digital comb filter (FIR1), and a 256-tap low-pass digital filter with a dual-loop shift register (FIR2). In this figure, the DSQ's are first-order Δ-Σ quantizers. The digital-filter test data input function is added for chip selection and testing.

A first-order Δ-Σ quantizer generates discrete spectral lines and thus reduces the SNR for low input levels without dithering. Therefore, 64-kHz 0.5-V_{pp} square waves are generated by the switched-capacitor circuits as a dither, and put in the differential stages as common mode. This dither vanishes by adding the first-stage differential outputs.

B. Analog Circuit Configuration and Operation

Each DSQ can be constructed of the same simple switched-capacitor circuit, as shown in Fig. 9, consisting of an input switched-capacitor circuit, a feedback 1-bit D-to-A conversion circuit (DAC), an integrator, and a comparator.

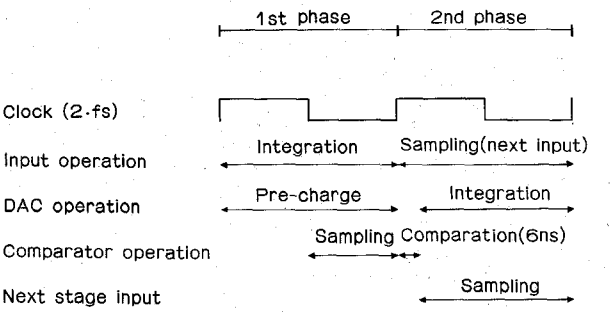

Fig. 10. DSQ operation timing.

In the Δ-Σ quantizer, the harmonic distortion of the DAC is one of the factors causing SNR degradation. The feedback 1-bit DAC consists of two switched-capacitor circuits. In these circuits, C_{d1} outputs the positive full scale and C_{d2} outputs the negative full scale. Theoretically, this DAC does not generate any harmonic distortions, because it outputs only two values. These modifications make it possible to fabricate a high-accuracy quantizer for the three-stage MASH configuration.

In the operation of this quantizer, the input voltage is first integrated by the input capacitor C_s. Simultaneously, feedback capacitors C_{d1} and C_{d2} are precharged to positive and negative full-scale charges, respectively. Ending the integration of the charge in C_i, the comparator compares the integrator output value and the *GND* level. Next, if the comparator output is positive, the negative full-scale charge, which is the output of the feedback D-to-A converter, is integrated. In the opposite case, the positive full-scale charge is integrated. The circuit operation timing of DSQ is shown in Fig. 10. The timing is divided into two phases: the input signal integration and DAC precharge phase, and the DAC output integration and next stage input switched-capacitor circuit sampling phase. The comparator acts at the end of the first phase for 6 ns. The SNR of the Δ-Σ quantizer is not degraded, even if the comparator has a conversion error and offset of more than ± 15 mV, because the noise which is generated by the conversion error is also shaped. Therefore, for high-speed operation, the comparator consists of a simple positive feedback flip-flop without the preamplifier.

By using this operation timing, the integrator outputs the quantization noise Q for the next stage input without any additional circuits. This can be shown as follows.

P, defined as the integrator output value at the end of the first phase, can be expressed as

$$P_1 = P_1 z^{-1} + X - C_1 z^{-1} \tag{12}$$

where X is the analog input value, and C_1 is the comparator output value of the first DSQ. The relationship between X and C_1 was expressed by (3). The amplifier output value at the end of the second phase is given as $P_1 - C_1$ by transforming (12) to produce

$$P_1 - C_1 = \frac{X - C_1}{1 - z^{-1}}. \tag{13}$$

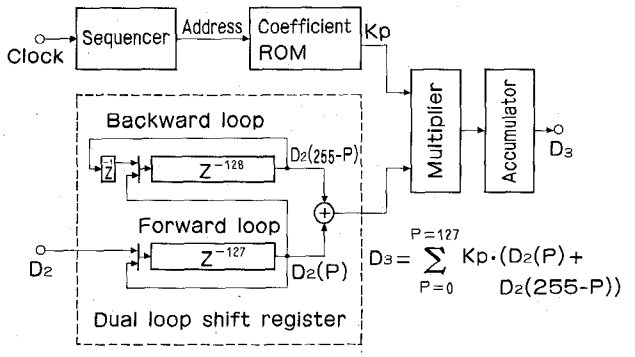

Fig. 11. Block diagram of the 256-tap low-pass transversal filter.

Therefore, $P_1 - C_1$ is given by (3) and (13):

$$P_1 - C_1 = -Q_1. \tag{14}$$

It is clear from (14) that the integrator output $P_1 - C_1$, which is the end of the second phase, equals the quantization noise Q_1. The configurations of the second and third stages are the same as that of the first stage. By this operation timing, the simple switched-capacitor quantizer without an analog subtractor for the three-stage MASH can be realized.

C. Digital Filter Configuration and Operation

The digital filter consists of a 1/16 decimation fourth-order comb filter and a 1/4 decimation 256-tap low-pass transversal filter using a dual-loop shift-register technique, as shown in Fig. 8.

A block diagram of the 256-tap low-pass transversal filter is shown in Fig. 11. It consists of a dual-loop shift register with 127 stages and 129 stages, a multiplier, an accumulator, a coefficient ROM, and a sequencer.

With symmetrical coefficients, the number of multiplications can be cut by summing data before multiplication [16]. Also, by dividing the shift register into a forward and a backward loop, two symmetrical data can be output at the same time.

Fig. 12 shows how the dual-loop shift register operates using a 16-tap filter. The 16-tap filter consists of a seven-stage shift register as a forward loop and a nine-stage shift register as a backward loop. Z_n is defined to be $D_2 z^{-n}$.

Fig. 12(a) is the initial condition of the data in the registers. The loop output data are Z_9 and Z_8. Z_1 is input into the forward loop, and Z_8 is input into the backward loop. Z_{17} is thrown away. Next, the forward and backward loops are actually made into loops and shifted once, which is shown in Fig. 12(b). At this point, loop outputs are Z_{10} and Z_7. Fig. 12(c) shows the results of shifting the forward and backward loops seven times. At that point, loop outputs are Z_{16} and Z_1, and all pairs of symmetrical data from Z_1 to Z_{16} are output by these shift operations. Then, when the forward and backward loops are shifted again, the results shown in Fig. 12(d) are produced. It is apparent that this is the same as the first condition plus one delay. This is the initial condition of the next operation.

The chief merits of this configuration are simplicity and controllability. Only, the shift registers are shifted, and the selectors are switched only once in each operation.

The use of a dynamic shift register reduces the area occupied by a one bit cell to that of a one bit RAM cell. The shift-register loops do not require a wiring area or any control logic. A precise on-chip digital filter is thus made possible.

VI. Measurement Characteristics

The actual chip photomicrograph fabricated using 2-μm CMOS process technology is shown in Fig. 13. The capacitors are placed in the center of the A-to-D converter block in order to reduce mismatching. The two quantizers of the first differential stage are laid out symmetrically with the digital blocks, because cross-talk noise from within the digital blocks is canceled as common-mode noise by this layout.

The chip size of the converter is 2.7×2.7 mm, and the size of the whole chip is 9.0×5.4 mm. The digital blocks contain 16.6K gates and the number of analog elements is 1.6K.

A block diagram of the measurement system is shown in Fig. 14. In this system, the SNR at the bandpass filter output is more than 100 dB at 1 kHz. The analysis accuracy of the FFT analyzer with minimum window is more than 103 dB at nonsynchronization for the analog signal and there are 2K FFT points at 48 ksps. The clock pulse of the A-to-D conversion LSI is 3 MHz and the digital data output rate is 48 ksps.

The measured spectrum is shown in Fig. 15. The digital filter cutoff frequency is 24 kHz. The second- and third-order harmonic distortions are about −102 dB, and higher order harmonic distortions are below the noise floor. The THD from the second to tenth order is 0.002 percent.

The SNR including THD versus input level characteristics are shown in Fig. 16, where the input signal frequency is 1 kHz and the signal bandwidth is 24 kHz. The SNR is 91 dB at a full-scale input level and 93 dB at a small-signal input level. These characteristics are good enough for high-quality audio encoding.

The digital filter frequency response is shown in Fig. 17. This is measured from the input of the comb filter to the digital output, as shown in Fig. 8. The passband is 24 kHz and the sampling frequency is 3 MHz. We obtained a passband ripple of 0.001 dB and a stopband attenuation of 105 dB.

The performance of the LSI is summarized in Table II. The SNR+THD is 91 dB at full-scale input. The power dissipation of the whole LSI is 110 mW at 3 MHz and that of the analog block is 35 mW.

Fig. 18 compares the use configuration of our developed LSI with the conventional A-to-D converter. In conventional A-to-D converters, both an S/H circuit and a high-order antialiasing analog filter are required, both of which are difficult to make with current VLSI technology.

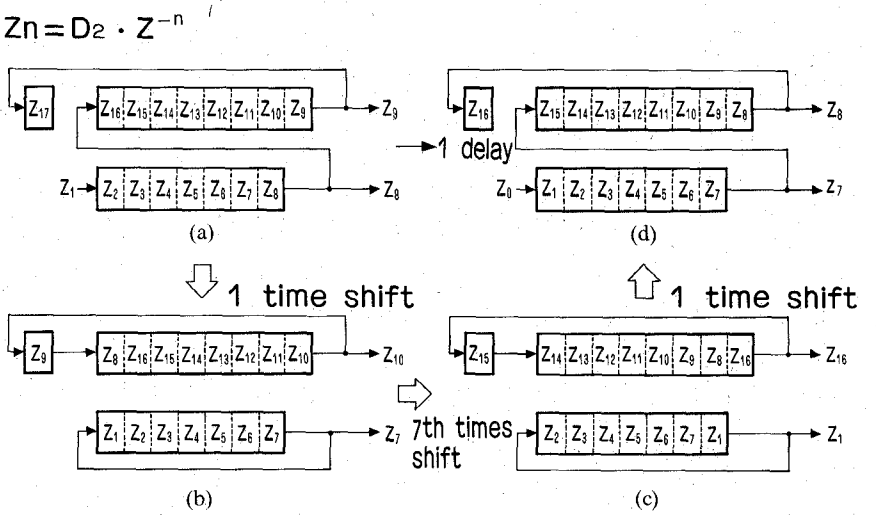

Fig. 12. Operations of the dual-loop shift register. (a) First condition. (b) Second condition. (c) Eighth condition. (d) First condition (next operation).

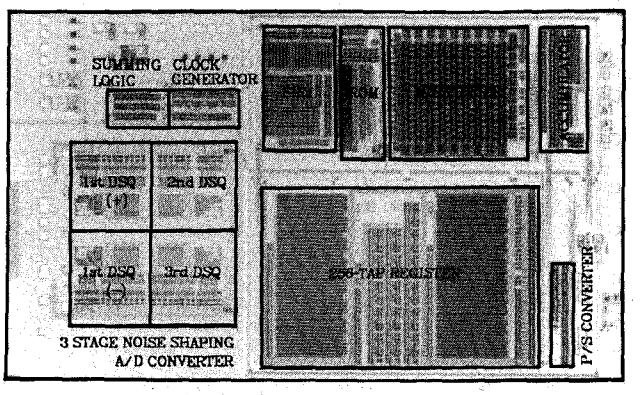

Fig. 13. Chip photomicrograph.

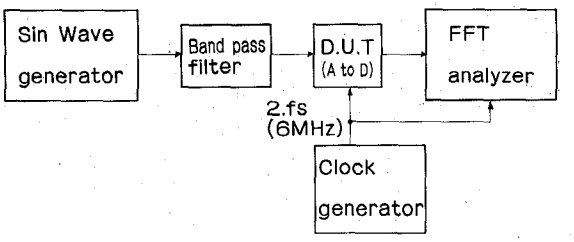

Fig. 14. Block diagram of the measurement system.

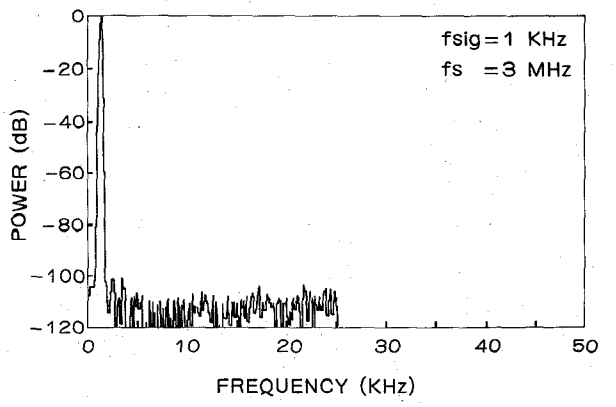

Fig. 15. Measured spectrum.

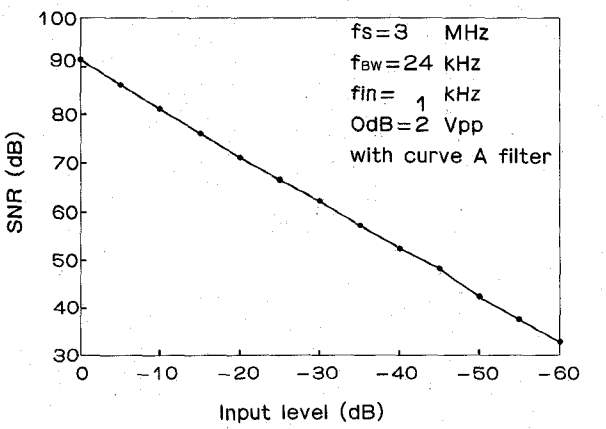

Fig. 16. SNR characteristics.

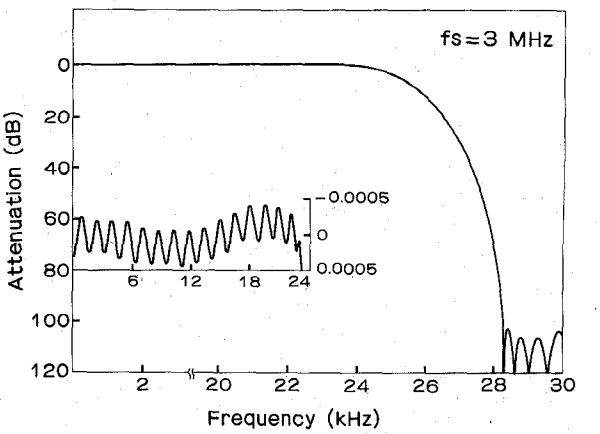

Fig. 17. Digital filter frequency response.

Our new LSI, however, does not require an S/H circuit, because the comparator acts only one time in each conversion operation. Also, a low-order *RC* filter can be used as an analog prefilter, because the sampling frequency is very high in comparison to the bandwidth (24 kHz).

TABLE II
LSI PERFORMANCE

Resolution	16 bit
Sampling frequency(fs)	⩽ 3 MHz
Signal bandwidth	fs/128
Signal/(Noise+THD)	91 dB
THD	0.002 %
Supply voltage	5 V
Power Dissipation	110 mW

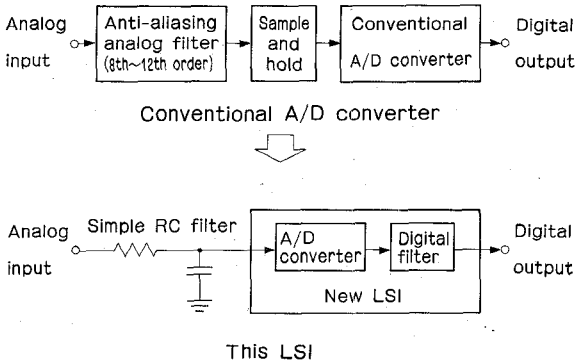

Fig. 18. Use configuration of this LSI.

VII. CONCLUSIONS

A triple-integration noise-shaping A-to-D conversion technology based on a multistage configuration of a delta-sigma quantizer has been developed. Applying this technology, a 16-bit 24-kHz bandwidth A-to-D converter with digital filters was integrated on a single chip utilizing a 2-μm CMOS process technology. An SNR of 91 dB and a THD of 0.002 percent at the full-scale input were successfully attained.

ACKNOWLEDGMENT

The authors would like to thank T. Sudo, E. Arai, Y. Akazawa, T. Kimura, and T. Kaneko, for their helpful suggestions and encouragement.

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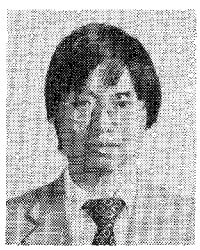

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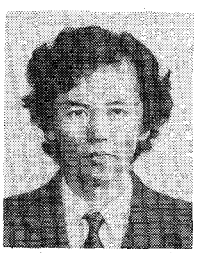

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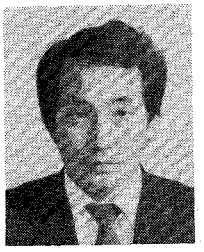

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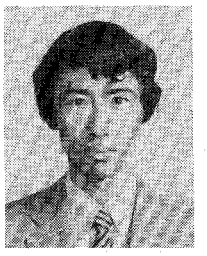

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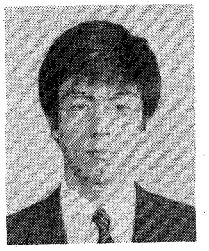

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