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2006

Chong, K. S., Gwee, B. H., & Chang, J. S. (2006). A 16-channel low-power non-uniform spaced filter bank core for digital hearing aids. IEEE Transactions on Circuits and Systems-II: Express Briefs, 53(9), 853-857.

https://hdl.handle.net/10356/90562

https://doi.org/10.1109/TCSII.2006.881821

A 16-Channel Low-Power Nonuniform Spaced Filter Bank Core for Digital Hearing Aids

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***Abstract*—We describe a 16-channel critical-like spaced, high stopband attenuation ($\geqslant$60 dB, 109th $\times$ 16-order), micropower (247.5 μW@1.1 V, 0.96 MHz), small integrated circuit (IC) area (1.62 mm^2@0.35-μm CMOS) finite impulse response filter bank core for power-critical hearing aids. We achieve the low-power and small IC area attributes by our proposed common pre-computational unit to generate a set of pre-calculated intermediate values that is shared by all 16 channels. We also take advantage of the consecutive zeros in the coefficients of the filter channels, allowing the multiplexers therein to be simplified. We show that our design is very competitive compared to reported designs, and with the advantages of higher stopband attenuation and linear phase frequency response. Compared to a design using the usual approach, our design features 47% lower power dissipation and 37% smaller IC area.**

***Index Terms*—Filter bank, finite-impulse response (FIR) digital filters, hearing aids, low power, nonuniform bandwidth.**

I. Introduction

HEARING aids (hearing instruments) are well accepted in the medical community as high-efficacy assistive portable biomedical devices to improve the speech intelligibility of hearing impaired users. The primary challenges of these devices include noise reduction (higher signal-to-noise ratio signals in noisy environments) [1], higher acoustical gain before the onset of acoustic feedback [2], low-distortion high-efficiency output amplifiers (Class-D) [3], small integrated circuit (IC) area, and low-power dissipation [4]. In the case of the latter two, for aesthetic and portability reasons, these hearing aids are powered remotely from a low-energy capacity ($\sim$100 mA $\cdot$ h) low voltage (1.1–1.4 V) miniature-size battery. Consequently, much of these challenges pertain to the development of more intelligent algorithms and to the degree of sophistication of these algorithms that can be realized without excessive power dissipation and IC area overhead.

One commonality between virtually all current-art hearing aids is the embodiment of a dedicated filter bank core—the filter bank decomposes the input signals into multiple sub-band signals (channels). The primary function of the filter bank is to obtain an adjustable/programmable magnitude frequency response of the hearing aid to compensate for elevated hearing thresholds of the hearing impaired user (fitted according to some prescription formula, typically the NAL-NL), and for the realization of noise reduction and multi-channel compression. The specifications of the filter bank typically include the stopband attenuation (e.g., 40–50 dB), number of channels (e.g., 16), and the passband spacing (typically Bark scale or critical band [5] that matches human frequency limens). The sophistication of these parameters is largely limited by the power budget allowed and IC area.

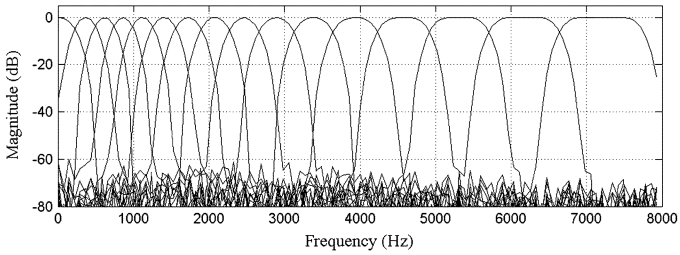

Fig. 1. Magnitude response of the 16-channel filter bank.

For a future advanced hearing aid, we specify the need for a linear phase (constant group delay) filter bank as opposed to the prevalent nonlinear phase infinite-impulse response (IIR) filter bank in current-art hearing aids. We deem the linear phase response necessary for an improved acoustic noise cancellation algorithm [2] and for the potential of better preserving the phase cues for binaural (as opposed to bilateral) hearing when a pair of hearing aids are simultaneously worn. The major drawback in a linear phase realization is the need for the order of the filter bank to be higher (hence increased overheads) over a filter bank without a linear phase for the same magnitude response. A further attribute that we impose is higher stopband attenuation ($\geqslant$60 dB) for the filter channels than current-art hearing aids (typically 50 dB). A higher stopband has potential for increased gain before the onset of acoustic feedback and greater magnitude response programmability.

To reduce the power dissipation of the filter bank for hearing aids, low computational complexity interpolated finite-impulse response (IFIR) filter banks [6], [7] have been proposed. However, the bandwidths of these filter banks are usually fixed (spaced uniformly), hence limiting the magnitude response programmability for hearing aids and poor frequency selectivity, particularly at low frequencies. Another approach to reduce the power is to reduce the power due to multiplications as multiplications are the main arithmetic operations in the filter bank. This reported approach includes multipliers with reduced spurious switching [8], multiplier-less and/or reduced hardware complexity techniques including canonical-signed-digit [9], powers-of-two [10], [11], common sub-expression elimination [12], etc. Although the latter techniques [9]–[12] are appeared

Manuscript received September 29, 2005. The work of K.-S. Chong was supported by the Singapore Millennium Foundation. This paper was recommended by Associate Editor S. L. Netto.

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Digital Object Identifier 10.1109/TCSII.2006.881821

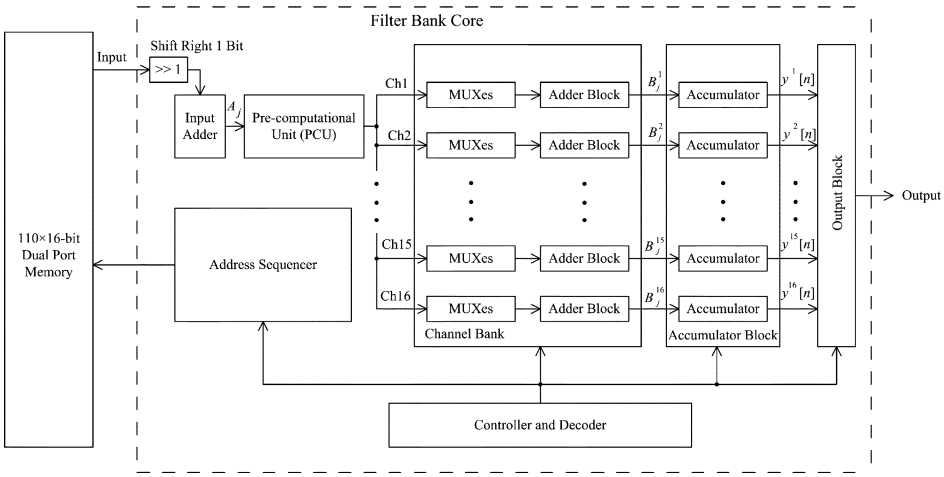

Fig. 2. Block diagram of the proposed 16-channel filter bank.

to be power efficient, this is true only for fixed coefficients that are optimized to particular bit patterns. The consequent shortcomings are the limited programmability and flexibility.

In this brief, we propose a critical-like spaced 16-channel linear-phase FIR filter bank core that features micropower [247.5 μW (excluding the memory)@1.1 V, 0.96 MHz using a 0.35-μm CMOS process] operation, high stopband attenuation ($\geqslant$60 dB per channel), and small IC area (1.62 mm^2). We achieve the low-power attributes by the design of a proposed simple pre-computational unit [(PCU), see Fig. 3, shown later] that can be shared by all channels and output of the PCU is multiplexed and added in a predetermined sequence to obtain the multiplication outputs. The multiplication operations are hence not realized by the usual dedicated power-hungry multipliers, and hence power reduction. In addition to the proposed architecture, we further reduce the power dissipation of the filter bank by adopting the technique of reducing the effective wordlength of the coefficients of the filter channels (where there are consecutive zeros) without compromising performance. We show that our design is very competitive against reported designs, yet obtaining the added desirable linear phase and high stopband attributes not featured in current-art devices. When compared to a conventional filter bank core (16 separate FIR filters with usual array multipliers [13]) of the same filter order, our filter bank is estimated to dissipate 47% lower power dissipation and to feature 37% smaller IC area.

II. FIR Filter Bank Specifications and Design

Fig. 1 depicts the magnitude response of 16 channels of the filter bank; each channel is a 109th-order (110 taps) FIR filter sampled at 16 kHz. We adopt the linear-phase-structured FIR (LPFIR) filter and use its symmetrical property [14] to reduce the number of multiplications by half (replaced by simple additions) compared to usual structures such as the transposed or transversal direct form structures. The expression for 109th-order LPFIR filter is

$$y^i[n] = \sum_{j=0}^{54} h^i[j] \cdot \{x[n-j] + x[n-109+j]\} \qquad (1)$$

where $h^i[j]$ is the coefficient for $j = 0$ to 54 in channel i, $y^i[n]$ is the output of channel i at time n, and $x[n-j]$ is the input at time n-j.

From (1), we observe that the inputs and their sequence to all channels ($i = 1$ to 16) are identical (before performing the respective multiplications). We exploit this observation by proposing to pre-calculate a set of intermediate signals by means of a PCU, and thereafter reuse these intermediate signals for all channels to generate the multiplication outputs (see Fig. 2). It is interesting to note that a recent reported computation sharing programmable FIR filter [15] also employed a somewhat similar PCU. However, this reported approach is for a high speed transposed direct form FIR filter with a low filter order and is hardware inefficient for realizing filters with a high stopband attenuation—its hardware (shift units and adders) increases proportionally with the order of the filter. Furthermore, the reported PCU was also not designed to be shared by the different channels of a filter bank. Our proposed design, on the other hand, does not suffer from these drawbacks—our design easily accommodates high-order filters and the PCU is shared by all channels and is independent of the order of the filters. These desirable attributes ultimately lead to a low-power dissipation and small IC area design.

Fig. 2 depicts the architecture of our proposed filter bank. The filter bank consists of a 110×16-bit dual port RAM and the filter bank core comprising an input adder, a PCU, an address sequencer, a controller and decoder, a channel bank, an accumulator block, and an output block. The PCU effectively provides scaled values (by means of hardwire shifts and adders/subtractors) of intermediate nodes, A_j, shown at output of the input adder in Fig. 2. The outputs of the PCU are multiplexed, shifted, and added (by means of multiplexers, hardwire shifts, and adders) in the channel bank and finally accumulated to obtain the outputs of the filter bank. In this proposed architecture, multiplication operations by the usual power-hungry multipliers are completely avoided to reduce power dissipation.

Prior to delineating the filter bank depicted in Fig. 2, we will first describe the PCU and subsequently the operation of Channel $i = 1$. In Fig. 3, we depict the proposed PCU that generates the eight possible multiplication products of

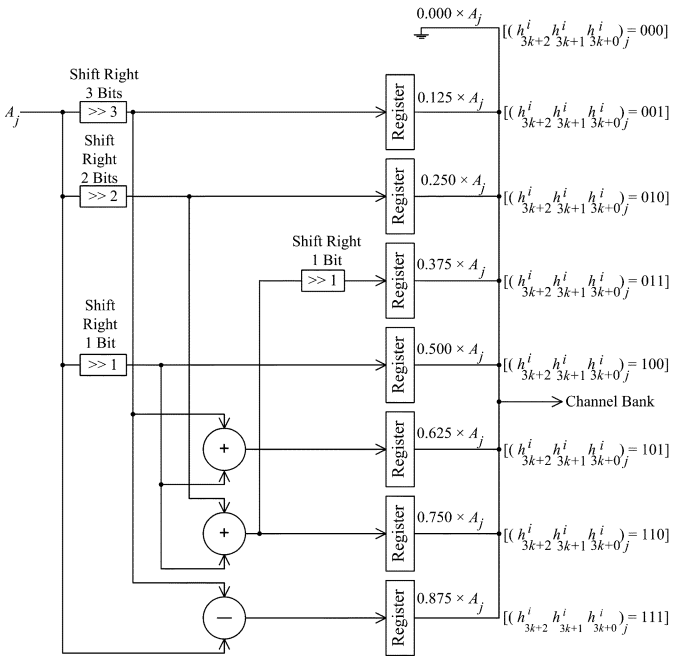

Fig. 3. PCU.

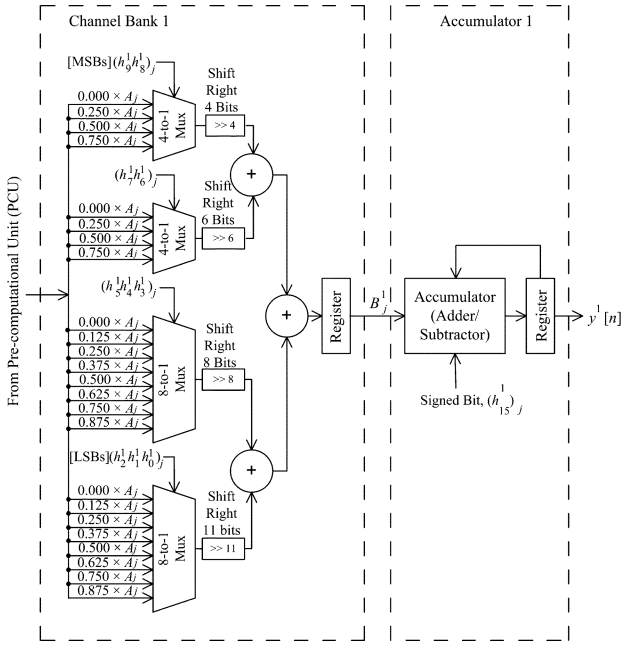

Fig. 4. Channel bank and accumulator for channel 1.

$(h^i_{3k+2}h^i_{3k+1}h^i_{3k+0})_j \times A_j$. In this specific case, we group the magnitude bits of the coefficients into a group of 3-bit patterns, and we denote them as "Group 3-bit." In Section III, we investigate the effect of the variations of different size groupings on the overall power dissipation of the filter bank. Of specific interest, note that no specific multiplier circuit is required to realize the PCU—only two 16-bit adders, one 16-bit subtractor, and seven 16-bit registers are required—and shifting is done by a simple hardwire shift. From an algorithmic view point, this is somewhat akin to a booth radix-4 multiplication [13]. However, the hardware realization of B^i_j (as multiplication outputs in Fig. 2) in our design is different from a booth radix-4 multiplier (and dedicated multipliers are not required).

Fig. 4 depicts the detailed block diagram of the channel bank and the accumulator block for Channel $i = 1$. In Fig. 4, the output of the PCU is weighted according to the coefficient by means of multiplexers. The outputs of the multiplexers are then shifted according to the coefficient. For example, for a 3-bit least significant bit (LSB) $(h^1_2 h^1_1 h^1_0)_j$, the output of the multiplexer is shifted right 11 bits; the actual shifts should have been 12 bits but to accommodate the overflow (the input signals have been scaled by half before passing to the input adder, see Fig. 2), only 11 bits need to be shifted. The shifted outputs of the multiplexers are then summed and B^1_j is obtained in the 24-bit register.

The output $y^1[n]$ is simply a summation of B^1_j for $j = 0$ to 54, taking the sign into account—the filter bank uses 16-bit fixed point data representation, the coefficients $(h^i[j])$ are in signed magnitude representation, and the inputs and data at nodes A_j are in 2's complement representation. The summation is accomplished in the Accumulator Block in Fig. 4, that is the positive or negative B^1_j are accumulated by a 24-bit accumulator to obtain the output of Channel 1, $y^1[n]$, in 2's complement data representation.

TABLE I
EFFECTIVE WORDLENGTH (EXCLUDING THE SIGNED BIT) OF COEFFICIENTS FOR DIFFERENT CHANNELS

Channel	1,2,3,4	5,6,7,8,9,10,12	11,13,14,15,16
Effective Wordlength (bits)	10	11	12

The computation for the remaining channels, Channel 2 to Channel 16, is similar to that described for Channel 1 except for the effective wordlength of the coefficients and the value of the coefficients therein. We note that the input adder to obtain A_j and the PCU (refer Fig. 2) are identical for all channels. We share these functional blocks between all channels, thereby substantially reducing the hardware complexity of the filter bank. We will quantify the advantages of this proposed approach in Section IV later.

The filter bank requires 60 clock cycles to compute each input sample: 55 clock cycles are used for processing 55 pairs of input data (110 taps) and the remaining 5 clock cycles are used to initialize and reset the filter bank. For 16-kHz sampling frequency, the system clock of our filter bank is low (0.96 MHz, this low clock rate is slightly lower than most current-art hearing aids).

In our filter bank, we take advantage where there are consecutive zeros in the 16-bit coefficients of a particular channel. For example, consider the magnitude bits of the coefficients of Channel 1, 000-00xx-xxxx-xxxx$_2$, where x is either 1 or 0. The first five MSBs are removed because the resultant product from a multiplication with consecutive zeros is always 0.

Table I tabulates the effective wordlength (excluding the signed bit) of the coefficients of the different channels in our filter bank. Arising from this simple technique, the average wordlength of the coefficients in the filter bank is reduced by $\sim$4 bits, that is the average effective wordlength is $\sim$11 bits. In hardware terms, this translates to $\sim$20% fewer multiplexers and $\sim$25% fewer adders in the channel bank.

TABLE II
POWER AND IC AREA OF THE FILTER BANK CORES BASED ON DIFFERENT PCUS AND MULTIPLEXERS@1.1 V, 0.96 MHZ

Design	PCU/Multiplexers	Power (μW)	Area (mm^2)
1	Group 2-bit/4-to-1	317.6	1.81
2	Group 3-bit/8-to-1	263.2	1.63
3	Group 4-bit/16-to-1	327.5	1.94
4	Group 3-bit/16-to-1 & 8-to-1	247.5	1.62

III. EFFECTS OF DESIGN VARIATIONS

We earlier delineated that different size groupings in the PCU and the channel bank affect the overall hardware complexity and power dissipation of the filter bank. In this section, we will describe the effect of these variations, for example Group 2-bit, Group 4-bit, etc.; in Fig. 3 for the PCU, a Group 3-bit was selected. The different bit-length combinations require different multiplexer designs (for example, 4-to-1, 8-to-1, 16-to-1, and various multiplexer combinations), different number of multiplexers and adders (to sum the data in the channel bank). In these combinations, the interconnection complexity of the filter bank will also be affected.

In general, we remark that the smaller the group number (e.g., 2-bit per group) for the PCU, the larger the number of multiplexers and adders required in the channel bank, and the converse (e.g., 4-bit per group) is true. As it is not obvious which specific combination would yield the design with the lowest power dissipation and the smallest IC area, we investigate the different combinations and designs.

We tabulate in Table II, the power dissipation and IC area of the filter bank core (without the memory) based on different group bit designs; the demands on the memory is independent of the size of the group bit. The different designs for the PCU and channel bank include Group 2-bit with 4-to-1 multiplexers (Design 1), Group 3-bit with 8-to-1 multiplexers (Design 2), Group 4-bit with 16-to-1 multiplexers (Design 3), and Group 3-bit with 4-to-1 and 8-to-1 multiplexers (Design 4).

From Table II, we note that Design 1 and Design 3 dissipate high power and occupy large IC area. This is largely because the former requires a larger number of multiplexers and adders in the channel bank while the latter results in more complex interconnections between the PCU and the multiplexers (for all channels) in the channel bank. Design 2 and Design 4 (embodying Group 3-bit for the PCU) feature low-power dissipation and comparable small IC area. This is largely because of a good tradeoff between the number of multiplexers and adders, and the complexity of the interconnections between the PCU and the channel bank. Of the two Group 3-bit designs, Design 4 features lower power dissipation (6% lower) and smaller IC area. This is because some multiplexers can be simplified (4-to-1 instead of 8-to-1) in the channel bank to take advantage of the consecutive zeros in the coefficients in the different channels—we earlier depicted this design combination in Fig. 4 for Channel 1.

In summary, on the basis of our investigation, we select Design 4.

IV. SIMULATION RESULTS

We depict the layout of our filter bank in Fig. 5 and our simulations are based on the extracted parameters from this layout. The design is based a commercial 0.35-μm-dual-poly-four-metal CMOS process and standard digital library cells were employed.

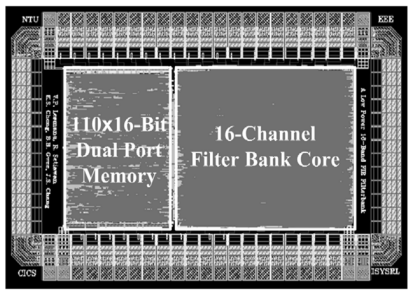

Fig. 5 Layout of the 16-channel filter bank.

TABLE III
BREAKDOWN OF NUMBER OF TRANSISTORS, IC AREA, AND POWER DISSIPATION OF THE DIFFERENT BLOCKS@1.1 V, 0.96 MHZ

Sub-Modules	Transistors	Area (mm^2)	Power (μW)
Channel Bank	58528	1.008	87.3
Accumulator Block	33692	0.389	70.7
PCU	4220	0.048	66.9
Controller & Decoder	10636	0.110	14.5
Address Sequencer	2244	0.028	2.1
Other	2516	0.037	6.0
Total	111836	1.620	247.5

We tabulate in Table III the breakdown of the number of transistors, area, and power dissipation of the various blocks of the filter bank core. As expected, the blocks that do most of the computations, namely the channel bank, accumulator block, and PCU, dissipate most of the power and occupy the largest IC area. Of specific interest, the single PCU that is shared by all 16 channels dissipates $\sim$27% of the total power but occupies only $\sim$3% of the total area (or $\sim$4% of the total number of transistors). We attribute its relatively large power dissipation to the large capacitive load due to the large fan-out.

To appreciate the significance of sharing the PCU, we design the same filter bank core without sharing the PCU. Should 16 PCUs be physically realized instead of one being shared, the area of the filter bank core would be 2.3 mm^2, an increase of 30%. This filter bank core also dissipates 435.5 μW, a 43% increase in power. Put simply, the advantages gained by sharing the same PCU for all channels are significant.

For completeness, the area and power dissipation for the dual-port RAM are respectively $\sim$0.6 mm^2 and 94 μW@1.1 V, 0.96 MHz. The power dissipation for this memory is relatively high because it is synthesized using flip-flops. The power dissipation of the memory based on the standard 8-transistor dual-port RAM cells would be considerably smaller.

At this juncture, it is instructive to compare our design against reported low-power filter bank designs for hearing aid applications. At this outset, we remark that a comparison of this nature will be somewhat contentious because of the very varied parameters.

We tabulate in Table IV a comparison and make the following comments. First, IFIR filter banks [6] (the passband bandwidths for each channel are constrained by the prototype filters due to its wavelet-based structure and its bandwidth is $\sim$1000 Hz)

TABLE IV
COMPARISON OF REPORTED FIR FILTER BANKS AND OUR PROPOSED FIR FILTER BANK

	Attenuation/ Order	Channels	V_{DD} (V)	Power (μW)	Area (mm^2)
Asynchronous IFIR [6]	40dB	7 (CB*)	1.55	117.0	19.36
Synchronous IFIR [6]	40dB	7 (CB*)	1.55	471.0	9.72
MDLNS filter bank [16]	60dB/75-order	8 (NB#)	1.60	316.0	0.05
LPFIR filters with multipliers	60dB/109-order	16 (NB#)	1.10	466.2	2.56
Proposed Design	60dB/109-order	16 (NB#)	1.10	247.5	1.62

* CB – Constrained Bandwidth, # NB – Non-constrained Bandwidth

dissipate low power. However, should the passband bandwidth be reduced to ~250 Hz and the stopband increased to 60 dB, the hardware would be considerably more complex and dissipate higher power. Second, the multidimensional logarithmic number system (MDLNS) filter bank [16] is a design where eight channels (bandwidth is ~1000 Hz) are independently designed but with some optimization to reduce the wordlength of the adders. Despite the small number of channels and relatively low-order filter, the power dissipation is relatively high. Third, using the usual approach involves realizing all channels of the 16-channel filter bank (16 LPFIR filters with multipliers) and the multiplication operations are obtained from the usual carry-saved array multipliers [13]. This design serves as a direct comparison against our proposed approach. By comparison, our design results in 47% lower power and 37% smaller IC area.

In summary, we show that our proposed design is very competitive in view of reported designs. When compared to nonlinear phase IIR filter banks embodied in current-art commercial hearing aids, our design is also competitive in terms of power dissipation and IC area, and with the added advantages of higher stopband attenuation and linear phase response; these advantages are otherwise expensive in hardware terms.

V. CONCLUSION

We have proposed a 16-channel critical band-like spaced micropower (247.5 μW@1.1 V, 0.96 MHz) small IC area (1.62 mm^2@0.35-μm CMOS) FIR filter bank core for hearing aid applications. We obtained the micropower and small IC area attributes by sharing the proposed PCU between all 16 channels and we take advantage of consecutive zeros in the coefficients of the filter channels. We have verified our filter bank on the basis of computer simulations from an actual layout. We have shown that our design is very competitive against reported designs, and with the added features of higher stopband attenuation and linear phase frequency response. When compared to a standard design of the same specifications, our design dissipates 47% lower power and features 37% smaller IC area.

ACKNOWLEDGMENT

The authors would like to thank V. Putra Lesmana and R. Setiawan for their assistance.

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