A 17-bit Oversampling D-to-A Conversion Technology Using Multistage Noise Shaping

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Abstract—**This paper discusses a highly stable, triple-integration noise-shaping technique and a precise differential pulse-width modulation (PWM) output method, which permits greater accuracy in monolithic audio D-to-A converters (DAC's), without trimming. Based on these new techniques, using 1.5-μm CMOS technology, a 17-bit 20-kHz bandwidth DAC LSI with digital filters was successfully developed. An SNR (S/(N+THD)) of 101 dB and a THD of 0.0007 percent at full-scale input were obtained.**

I. INTRODUCTION

WITH PROGRESS in the digital audio and telecommunications fields, a high-accuracy and high-resolution D-to-A conversion technology has become one of the key analog circuit technologies. Conventionally, either the weighted network circuit technique with trimming or the multislope integration circuit technique have been used for high-resolution D-to-A converters (DAC's). In the weighted network, which uses an R-$2R$ ladder or current summation, to achieve a conversion accuracy over 15 bits, some trimming of the weighted network using a laser, dynamic element matching, or digital method using ROM, was needed [1]–[3]. This is because the conversion accuracy, which depends on the device matching tolerance of the weighted network, is limited to 14-bit accuracy when nontrimming weighted networks are used [4], [5].

Using the multislope integration circuit, high speed and high accuracy are required in the integrator, sample-hold (S/H) circuit, and current sources. To make these circuits, high f_T bipolar process technologies must be used [6]. The development of an S/H circuit with more than 16-bit accuracy is especially difficult because the sampled charge in the sampling capacitor leaks through the base impedance of the bipolar transistor.

Recently, oversampling noise-shaping techniques have attracted considerable attention as conversion techniques suitable for VLSI technology, as they do not require trimming, a precise S/H, and weighted network [7], [8]. The noise reduction concept of an oversampling noise-shaping technique has two features. One is to distribute quantization noise outside the signal band by setting the sampling rate much higher than the signal bandwidth, and the other is the noise shaping resulting from integration. Thus, this technique has the advantage that the device tolerance is relaxed, and it is possible to use a two-value output circuit that requires no complicated analog circuits and in theory produces no distortion. By using a higher frequency than the sampling clock pulse and higher-order integration noise-shaping characteristics, higher accuracy is achieved.

Due to the instability of the integrator, a conventional oversampling noise-shaping technique, however, is limited to second-order noise-shaping characteristics [9]. [10]. To overcome this problem, we have developed a multistage noise-shaping technique, which permits higher-order noise-shaping characteristics (more than the double-integration level) by using a new multistage configuration based on a stable single-integration Σ-Δ quantizer [11], [12]. Hereafter, this technique will be referred to as multistage noise shaping (MASH). Recently, we successfully applied three-stage MASH technology to a 16-bit A-to-D converter LSI and confirmed the feasibility of MASH in concrete audio applications [13].

In this paper, we will discuss a D-to-A conversion technology, utilizing a two-stage MASH technique with triple-integration noise-shaping characteristics, and a differential pulse-width modulation (PWM) analog output generation technique with low noise and distortion. In Section II, the theoretical accuracy of the noise-shaping D-to-A conversion technique is discussed. In Section III, the operating principle of the MASH technique and the new loop-stabilizing technique are described, and it will be shown that high-order noise-shaping characteristics (more than triple-integration level) are easily obtainable. In Section IV, the configuration of the analog output circuit using the PWM method is shown, and distortion in the differential PWM method is discussed. In Section V, the circuit configuration and operation of the developed 17-bit D-to-A conversion LSI with precise digital filters is described in detail [14]. In Section VI, measurement results

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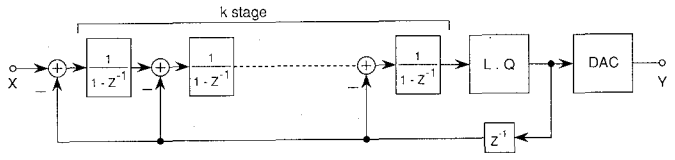


Fig. 1. Fundamental configuration of noise-shaping DAC.

of the fabricated D-to-A conversion LSI are presented. These results confirm the usefulness of MASH as a technique to enhance monolithic DAC accuracy.

II. Theoretical Accuracy of the Noise-Shaping Technique

In the conventional noise-shaping DAC, shown in Fig. 1, the theoretical accuracy-limiting factors are 1) oversampling frequency and 2) the integration order of noise-shaping characteristics. Generally, the transfer function of D-to-A converters using the noise-shaping techniques is given by

$$Y = X + (1 - z^{-1})^k Q. \tag{1}$$

Here, Y is the output of the DAC, X is the input, Q is the quantization noise of the local quantizer, and k is the order of integration. When m is the oversampling ratio, q is the voltage of 1 LSB, f_s is the oversampling frequency, and n is the number of local quantizer output levels. The power of signal X_p, the power of quantization noise Q_p, and $(1 - z^{-1})$ are given by

$$X_p = (n-1)^2 q^2/8 \tag{2}$$

$$Q_p = q^2/12. \tag{3}$$

The synthesis of quantization noise Q_i in signal bandwidth is given by

$$Q_i = \int_0^{f_s/2m} (1 - z^{-1})^{2k} Q_p df. \tag{4}$$

The approximation of (4) is given by (5) as $m > 4$:

$$Q_i = (q^2 \pi^{2k}) / (12(2k+1) m^{2k+1}). \tag{5}$$

Therefore, the SNR of the noise-shaping DAC is given by

$$\begin{aligned} \mathrm{SNR} &= 10 \log_{10} (X_p / Q_i) \\ &= (6k+3) \log_2 m - (9.94k - 1.76 - 10 \log_{10} (2k+1)) \\ &\quad + 20 \log_{10} (n-1) \\ &\approx (6k+3) \log_2 m - (8k-4) + 20 \log_{10} (n-1). \end{aligned} \tag{6}$$

The relationship between SNR and k, m is shown in Fig. 2, and the improvement of SNR in relation to the number of quantized outputs n is shown in Table I. To obtain an SNR of over 100 dB, an oversampling ratio of 177 is necessary for second-order noise-shaping characteristics, 57 is necessary for third-order, and 27 for fourth-order. Using noise-shaping technology, a wide variety of designs

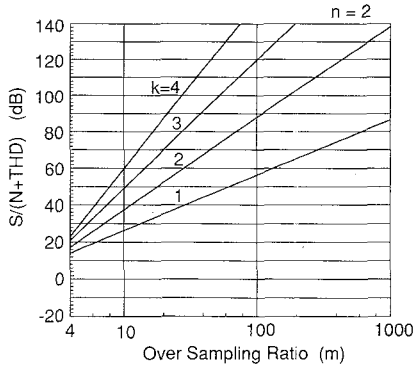


Fig. 2. Relationship between SNR and k, m.

TABLE I
Improvement of SNR in Relation to the Number of Quantized Output Levels

n	$20 \log_{10}(n-1)$
2	0 dB
4	9.5 dB
8	16.9 dB
16	23.5 dB
32	29.8 dB
64	36.0 dB
128	42.0 dB

is possible given the choice of m, k, and n. However, the integration order of noise-shaping k based on conventional Σ-Δ noise-shaping techniques, as shown in Fig. 1, is limited to only the second order in the case of $n < 32$, which is 5-bit resolution. The reason is that higher-order integration noise-shaping characteristics above the second order cannot be obtained due to instability caused by overloading of the integrator in the loop. The weighted network is required for realizing the local DAC with more than 5-bit resolution. Therefore, realizing an accuracy of more than 16 bits is very difficult due to the mismatch of the weighted network. To overcome this problem, we have developed the MASH technique, which realizes stable multiorder noise-shaping characteristics independent of the local DAC resolution n, and confirmed its feasibility with an experimental D-to-A conversion LSI using the MASH configuration with triple-integration noise-shaping characteristics and 3-bit local PWM DAC.

III. Principles of the Triple-Integration MASH

A. Basic MASH Technology

Signal flowcharts of a conventional double- and triple-integration Σ-Δ quantizer are shown in Fig. 3(a) and (b), respectively. The transfer functions of these signal flowcharts are given by

$$Y = X + (1 - z^{-1})^2 Q \tag{7}$$

$$Y = X + (1 - z^{-1})^3 Q. \tag{8}$$

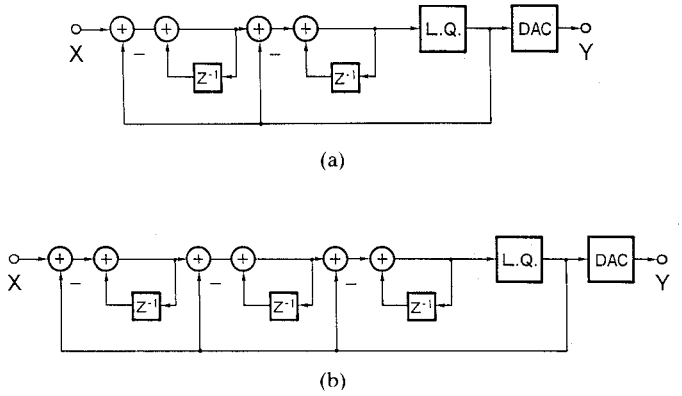


Fig. 3. Conventional Δ-Σ quantizer configuration: (a) double-integration Δ-Σ quantizer; (b) triple-integration Δ-Σ quantizer.

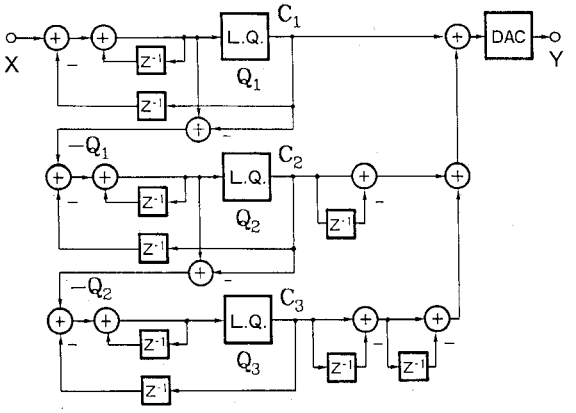


Fig. 4. Basic three-stage MASH configuration.

However, the loop of the conventional triple-integration Σ-Δ quantizer, as shown in Fig. 3(b), which includes tree integrators, oscillates because of a 270° phase shift. Therefore, for stable triple-integration noise-shaping characteristics, a MASH configuration, using stable single-integration Σ-Δ quantizers (DSQ's), was previously proposed [11], [13]. Fig. 4 shows a signal flowchart of the three-stage MASH. Outputs of the first, second, and third DSQ's are given by

$$C_1 = X + (1 - z^{-1})Q_1 \tag{9}$$

$$C_2 = -Q_1 + (1 - z^{-1})Q_2 \tag{10}$$

$$C_3 = -Q_2 + (1 - z^{-1})Q_3. \tag{11}$$

Y, which is the three-stage MASH output, is obtained by a summation of C_1, the first-order differentiation of C_2, and the second-order differentiation of C_3:

$$\begin{aligned} Y &= C_1 + (1 - z^{-1})C_2 + (1 - z^{-1})^2 C_3 \\ &= X + (1 - z^{-1})^3 Q_3. \end{aligned} \tag{12}$$

Equation (12) is the same equation as (8), evaluated from the basic Σ-Δ configuration of Fig. 3(b). Therefore, the configuration of Fig. 4 is equivalent to Fig. 3(b). The important point is that triple-integration noise-shaping characteristics can be obtained using a cascade connection and pipelined operation of three first-order Σ-Δ quantizers.

In a basic configuration with three-stage MASH technology, shown in Fig. 4, a problem is created because the SNR is limited by output voltage attenuation. This is because of the decrease in the transfer gain Y/X. The transfer gain is given by the ratio of the quantized-level number of the first local quantizer $L1$ to that of the overall three-stage quantizer L_t. For example, if quantizer levels of C_1, C_2, and C_3 are -1, 0, and 1, the final quantized level of 15 is $-7, -6, \cdots, 7$. Therefore, the ratio L_1/L_t is 1/7 and the output voltage is multiplied by about 0.143.

B. Enhancement of the Output Voltage Swing

In order to suppress this output level loss, the final quantized level L_t must be reduced by decreasing the number of the stage and increasing the first quantizer level L_1. Fig. 5 shows a new MASH configuration that solves this problem. It consists of a two-stage configuration of single- and double-integration Σ-Δ quantizers and has the same triple-integration noise-shaping characteristics as the Fig. 4 configuration. In Fig. 5, with C_1 and C_2 being defined as outputs of the local quantizers, the following equations are obtained:

$$C_1 = X + (1 - z^{-1})Q_1 \tag{13}$$

$$C_2 = -Q_1 + (1 - z^{-1})^2 Q_2. \tag{14}$$

Since output Y can be synthesized from C_1 and C_2, (15) is obtained:

$$Y = C_1 + (1 - z^{-1})C_2 = X + (1 - z^{-1})^3 Q_2. \tag{15}$$

This equation clearly shows that Y has third-order noise-shaping characteristics. For example, if quantizer levels of $C_1(L_1)$ are set at five levels $(-2, -1, 0, 1, 2)$ in order to increase the number of the first quantizer level and C_2 is set at two levels $(-0.5, 0.5)$, the number of final quantized levels L_t becomes seven $(-3, -2, -1, 0, 1, 2, 3)$, which is almost half the number of the basic three-stage MASH. These seven levels contain the five levels of the first-stage quantizer L_1. Therefore, a ratio of 4/6 can be obtained. This is about five times that of the basic MASH configuration shown in Fig. 4. In other words, an SNR improvement of 13.4 dB can be attained.

C. Improvement of Stability

Another problem, however, appears in the design of a double-integration Σ-Δ quantizer for the second quantizer of the new configuration, as shown in Fig. 5. Generally, when a large input voltage close to the full-scale level is applied, the double-integration Σ-Δ quantizer cannot track the input signal because the first integrator is overloaded. Fig. 6 shows the two-stage triple-integration MASH configuration for the D-to-A conversion with the loop-stabiliz-

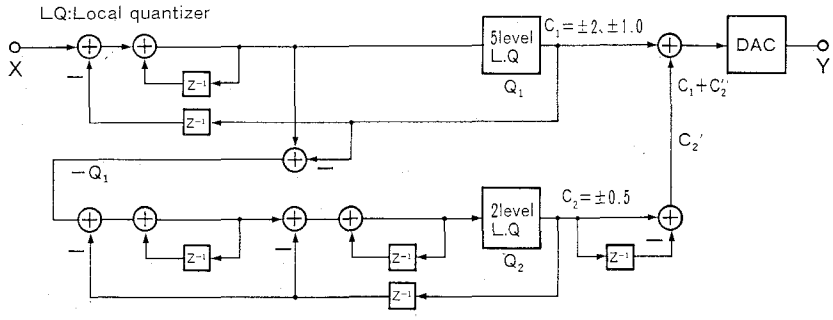


Fig. 5. Two-stage MASH configuration with single- and double-integration quantizer.

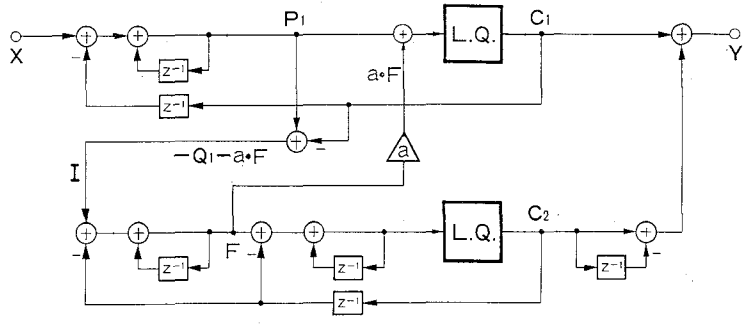


Fig. 6. Two-stage MASH configuration with local feedback pass for loop stabilization.

ing circuit. By feeding back the first integrator output of the second stage to the first stage local quantizer input, the input of the second stage is controlled so that the first integrator output in the second stage is never overloaded. The feedback signal is included in the first-stage output C_1 and second-stage input I. If F is the first integrator output of the second stage, and a $(0 < a < 1)$ is a coefficient for F, C_1, I, and C_2 are given by

$$C_1 = X + (1 - z^{-1})(aF + Q_1) \tag{16}$$

$$I = -Q_1 - aF \tag{17}$$

$$C_2 = I + (1 - z^{-1})^2 Q_2. \tag{18}$$

Therefore, DAC output Y is given by

$$Y = C_1 + (1 - z^{-1})C_2 = X + (1 - z^{-1})^3 Q_2. \tag{19}$$

Equation (19) is the same as (15), which means that the feedback signal in the first-stage output is canceled by the second-stage output C_2. This ensures a stable second-stage MASH operation and results in triple-integration noise-shaping characteristics.

IV. Differential PWM Output Method

A. Configuration of Differential PWM Circuit

Generally, the output DAC for the noise-shaping D-to-A converter uses a switched-capacitor circuit [11], [12], [15]. For high-accuracy D-to-A conversion, however, it is not suitable because the switched-capacitor circuit suffers accuracy degradation from clock feedthrough noise and settling error noise. Therefore, a multibit resolution DAC,

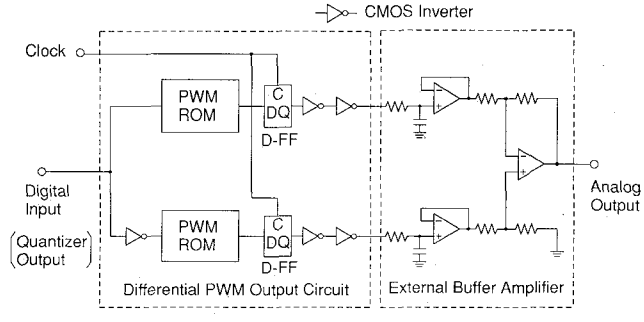


Fig. 7. Differential PWM output circuit configuration.

which is required in the final output DAC in this MASH configuration, was realized using a PWM method. This uses a parallel-to-serial converter, a retiming circuit, and a 1-bit DAC, none of which requires precision analog components. Furthermore, the 1-bit DAC can easily be designed using a CMOS inverter, taking care to decrease the noise from the digital circuits and to resolve the mismatching between high-to-low and low-to-high transition characteristics. The differential PWM output circuit is shown in Fig. 7. The PWM waveform is generated in ROM and resampled by the retiming circuit of the D-flip-flop (D-FF) to suppress the jitter. Buffer amplifiers, with differential-to-single conversion, and RC filters are formed using off-chip standard operational amplifiers.

B. Suppression of the Second-Order Harmonic Distortion

In this PWM output circuit, on-resistance mismatching of p- and n-channel MOS devices in the final-stage CMOS inverter causes second-order harmonic distortion. An equivalent circuit of the CMOS inverter is shown in Fig. 8.

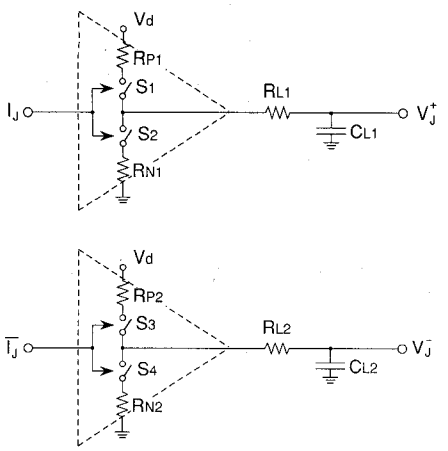


Fig. 8. Equivalent circuit of CMOS inverter.

The input I_J is a time-domain modulated PWM signal when time is J. Assuming the switch S_1 is ON for period T_a, and S_2 is ON for period T_b, and input signal is $\sin\theta$, T_a and T_b are shown as

$$T_a = T_m(1+\sin\theta) \tag{20}$$

$$T_b = T_m(1-\sin\theta) \tag{21}$$

where

$$T_m = 1/(2f_s).$$

Considering the time constant of R_{L1} and C_{L1}, the positive output voltage when time is J, is given by

$$\begin{aligned} V_J^+ &= \frac{T_a}{C_{L1}(R_{L1}+R_{P1})}(V_d - V_{J-1}) \\ &\quad - \frac{T_b}{C_{L1}(R_{L1}+R_{N1})}V_{J-1} \\ &= \alpha V_d(1+\sin\theta) - V_{J-1}[(\alpha+\beta)-(\alpha-\beta)\sin\theta] \end{aligned} \tag{22}$$

where

$$\alpha = \frac{T_m}{C_{L1}(R_{L1}+R_{P1})}$$

$$\beta = \frac{T_m}{C_{L1}(R_{L1}+R_{N1})}.$$

To solve (22) as recurrence formula, V_J^+ is approximately given by

$$\begin{aligned} V_J^+ &= \alpha V_d(1+\sin\theta) - \alpha V_d(1+\sin\theta) \\ &\quad \cdot[(\alpha+\beta)-(\alpha-\beta)\sin\theta] \\ &= \alpha V_d + \alpha V_d\sin\theta + \alpha V_d(\alpha-\beta)\sin^2\theta. \end{aligned} \tag{23}$$

The first term of (23) is a dc component, the second term is the signal, and the third term is the second-order harmonic distortion. Equation (23) shows that second-order harmonic distortion depends on $\alpha-\beta$. If a differential output circuit is adopted, negative phase output V_J^- is obtained by substitution of $-\sin\theta$ for $\sin\theta$ in (23), and the single-ended output is given by

$$V_J^+ - V_J^- = 2\alpha V_d\sin\theta. \tag{24}$$

From this equation, it is clear that the dc component and second-order harmonic distortion are canceled by a differential configuration. Furthermore, power supply noise and crosstalk are removed from the large-scale logic circuit by the common mode rejection characteristics of the differential configuration.

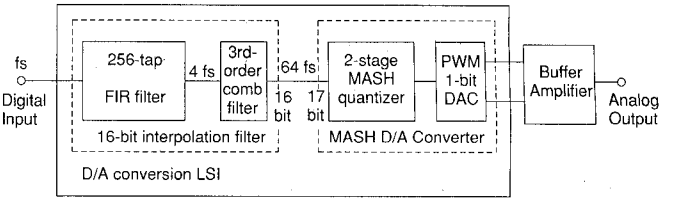


Fig. 9. Block diagram of the LSI.

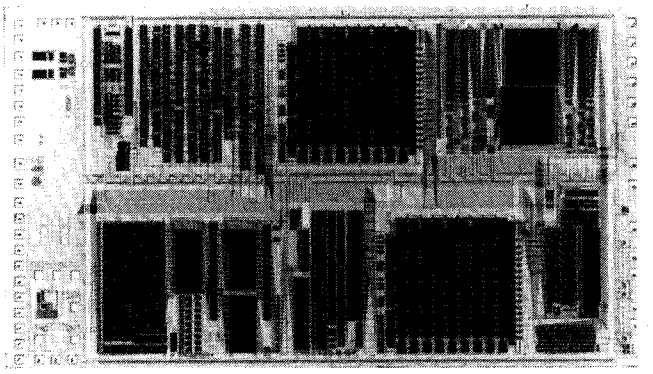


Fig. 10. Chip photomicrograph.

V. LSI Configuration and Fabrication

A block diagram of the LSI is shown in Fig. 9. It consists of an interpolation digital filter with a passband ripple of ± 0.0005 dB and a stopband attenuation of 105 dB, the MASH quantizer, and the differential PWM output circuit. The main features of the MASH quantizer are as follows: the oversampling ratio is 64, there are seven output levels (five at the first stage and two at the second stage), and the theoretical SNR is 120 dB. The digital filter consists of a linear phase 256-tap FIR filter, which interpolates the sampling rate to 4 f_s, and a third-order comb filter, which interpolates the sampling rate to 64 f_s. The FIR filter was designed with a dual-loop shift register architecture [12].

An experimental chip was fabricated using 1.5-μm CMOS process technology. A photomicrograph of this chip is shown in Fig. 10. The size of the whole chip is 7.4×4.0 mm, and the number of gates is 11K. The chip layout was automatically designed using a chip floor plan program and a routing program. Analog circuits, whose performance is sensitive to layout, and regular logic circuits were prepared as macrocells. Random logic resulted from the use of standard cells.

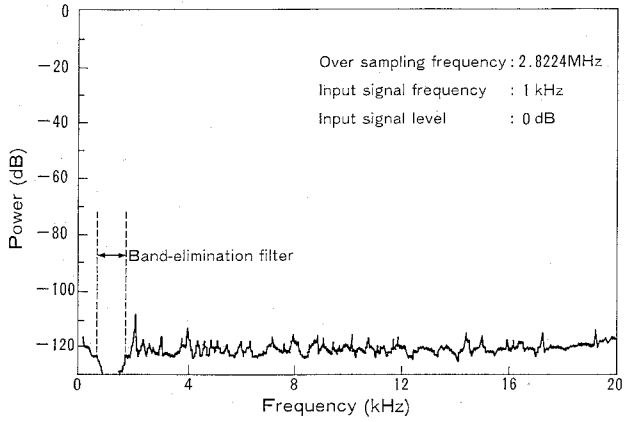


Fig. 11. Measured spectrum characteristics.

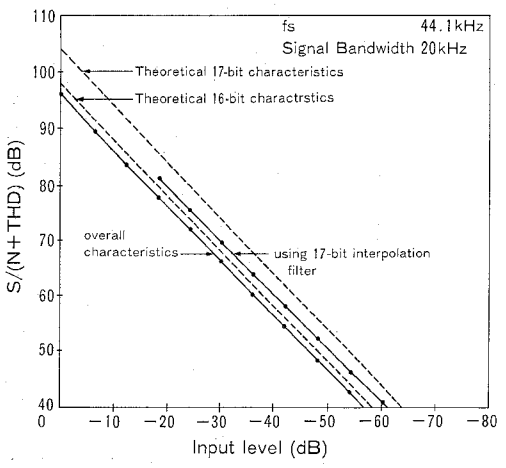
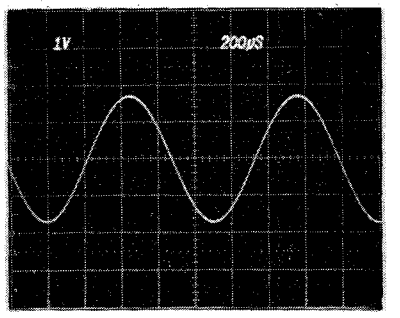


Fig. 12. Measured SNR characteristics including THD.

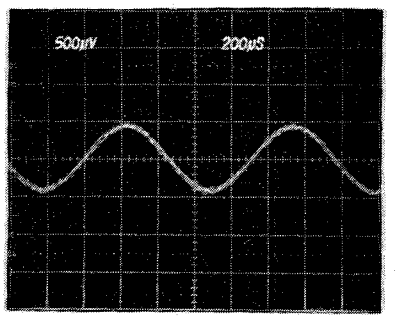
VI. Performance of the D-to-A Conversion LSI

The performance of this D-to-A conversion LSI is discussed below. The measured power spectrum at the full-scale input level is shown in Fig. 11. The second harmonic distortion is about −108 dB, and higher harmonic distortions are below −110 dB. The THD from second to tenth is 0.0007 percent, and the SNR is 96.0 dB. The SNR, including THD, versus input level characteristics is shown in Fig. 12. The dynamic range of this system is 96.5 dB from which the dynamic range of the developed LSI is estimated to be 97.2 dB, after eliminating the external component noise. These characteristics, which come close to 16-bit accuracy, are limited by the quantization noise of the 16-bit digital filter. The word length of the interpolation digital filter is basically 16 bits. To confirm the real accuracy of this D-to-A conversion technology, a 17th bit was added using the bit-length expansion function. This was produced by a bit shift circuit, so full input dynamic range could not be obtained. The measured characteristics are also plotted in Fig. 12, from which it can be seen that this D-to-A converter has a 101-dB dynamic range, which is equivalent to 17-bit accuracy.

The output waveforms at the full-scale and −72-dB sine-wave input are shown in Fig. 13. Conventional D-to-A converters with a weighted network circuit have zero-cross distortion, generated by the mismatch of the analog components. However, this LSI never generates such distortion and reconstructs a pure sine wave at even the very small input level of −72 dB.



Input Level 0 dB



Input Level -72 dB

Fig. 13. Output waveforms.

TABLE II
LSI Performance

Item	Whole LSI	D to A Converter
Resolution	16 bit	17 bit
Sampling frequency	48 KHz	
Over sampling ratio	64	
S/(N+THD) [fullscale input]	96.0 dB	
S/(N+THD) [-60dB input]	36.5 dB	41 dB
THD [2nd-10th]	0.0007 %	0.0007%
Idle channel noise	109 dB	
Supply voltage	5 V	
Power dissipation	160 mW	30 mW

The performance of the LSI is summarized in Table II. The maximum sampling frequency is 48 kHz, and the oversampling ratio is 64. The supply voltage is 5 V, and the power dissipation is 160 mW at a sampling frequency of 44.1 kHz. These characteristics are good enough for high-quality digital audio decoding and are applicable to CD players and digital audio tape recorders.

VII. Conclusions

A new noise-shaping D-to-A conversion technology of over 16-bit accuracy, based on a new multistage noise-shaping configuration and a differential PWM circuit, was developed. Applying these technologies, a 16-bit 20-kHz

bandwidth D-to-A conversion LSI with digital filters was integrated on a single chip utilizing a 1.5-μm CMOS process technology. A dynamic range of 101 dB and a THD of 0.0007 percent were obtained. This D-to-A conversion technology is suitable for the design of ASIC's because of its compatibility with digital VLSI process technology and digital signal processing technology.

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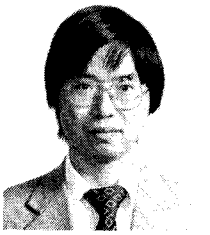

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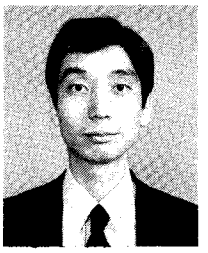

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