

A 183 GHz Metamorphic HEMT Low-Noise Amplifier with 3.5 dB Noise Figure

Giuseppe Moschetti, Arnulf Leuther, Herman Maßler, Beatriz Aja, Markus Rösch, Michael Schlechtweg, Oliver Ambacher, Ville Kangas, and Marie Geneviève-Perichaud

Abstract—This paper presents a 183 GHz low-noise amplifier (LNA), designed primarily for water vapor detection in atmosphere. The LNA requirements were defined by MetOp Second Generation (MetOp-SG) Microwave Sounder, Microwave Imager and Ice Cloud Imager instruments. MetOp-SG is the European contribution to operational meteorological observations from polar orbit. This LNA advances the current state-of-the-art for the InGaAs metamorphic high electron mobility transistor (mHEMT) technology. The five-stage common-source MMIC amplifier utilizes transistors with a gate length of 50 nm. On-wafer measurements show a noise figure of 3.5 dB at the operative frequency, about 1 dB lower than previously reported mHEMT LNAs, and a gain of 24 ± 2 dB over the bandwidth 160-200 GHz. The input and output matching are -11 dB and -10 dB, respectively. Moreover, the DC power dissipation at the optimal bias for noise is as low as 24 mW.

Index Terms—G-band, low-noise amplifiers (LNAs), metamorphic high electron mobility transistor (mHEMT), monolithic microwave integrated circuit (MMIC).

I. INTRODUCTION

THE 183 GHz frequency range is used in radiometers for humidity soundings due to the water vapor resonance, which allows humidity profiling of the atmosphere. Microwave sounding instruments have a long heritage in operational meteorology and are the core instruments for numerical weather prediction. Humidity soundings are also used for climate monitoring applications. The sensitivity (NEAT) of a radiometer is a key performance parameter, which is dominated by the receiver noise figure. Improving the NEAT improves directly the weather forecast skill. A large amount of work with the aim of developing ultra-low noise amplifiers operating at 183 GHz have been reported [1]-[8]. In [4], a minimum noise figure of 3.4 dB was demonstrated in a packaged amplifier based on 35 nm InP HEMTs. MMIC

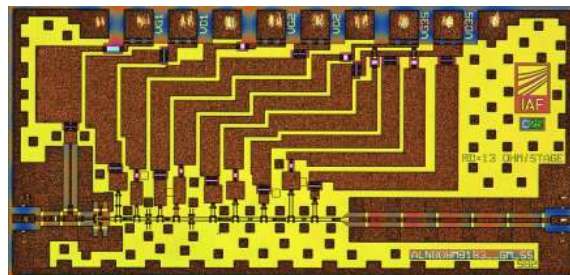


Fig. 1. Chip photograph of the five-stage 183 GHz MMIC amplifier. The chip size is 1×2 mm².

LNAs based on the mHEMT technology have demonstrated so far a lowest on-wafer noise figure of 4.4 dB at 165 GHz [8] and around 4.8 dB in the frequency range 180-200 GHz [7].

In this letter, we present the design and characterization of a 183 GHz MMIC LNA based on the 50 nm mHEMT technology which is designed to be used in the MetOp-SG meteorology satellites. At the operation frequency, the LNA demonstrates on-wafer noise figure of 3.5 dB and gain of 24.5 dB, as well as a low dc power consumption of 24 mW. To our knowledge, this result represents the state-of-the-art for the mHEMT technology, reducing the gap with the InP HEMT technology.

II. TECHNOLOGY

The LNAs were fabricated using the in-house 50 nm $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{In}_{0.8}\text{Ga}_{0.2}\text{As}/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ metamorphic HEMT heterostructure grown using molecular beam epitaxy (MBE) on 4-inch semi-insulating GaAs substrates. Details on the epitaxial growth and fabrication process are reported in [7]. This technology features peak transconductance g_m of about 2100 mS/mm and typical extrinsic values of f_T and f_{max} of about 370 GHz and 670 GHz, respectively, for a 2×15 μm device. The passive components of the MMICs include 50 Ω/sq thin film resistors in NiCr, 225 pF/mm² SiN based metal-insulator-metal (MIM) capacitors and two metal layers for interconnection with 2.7 μm thick Au plated air bridge technology. The technology features also backside processing with the substrate thinned down to 50 μm and a back plane metal layer for suppression of the substrate modes.

III. AMPLIFIER DESIGN

The single-ended MMIC LNA is a five-stage design with GCWG layout and a total chip area of 1×2 mm². A

G. Moschetti is with the Fraunhofer Institute for Applied Solid State Physics IAF, Freiburg 79108, Germany (e-mail: giuseppe.moschetti@iaf.fraunhofer.de).

A. Leuther, H. Maßler, M. Rösch, M. Schlechtweg, and O. Ambacher are with the Fraunhofer Institute for Applied Solid State Physics IAF, Freiburg 79108, Germany.

B. Aja is with the Fraunhofer Institute for Applied Solid State Physics IAF, Freiburg 79108, Germany and also with the University of Cantabria Santander, 39005, Spain.

V. Kangas and M. Geneviève-Perichaud are with the European Space Agency (ESTEC), NL-2200 AG, Noordwijk, The Netherlands.

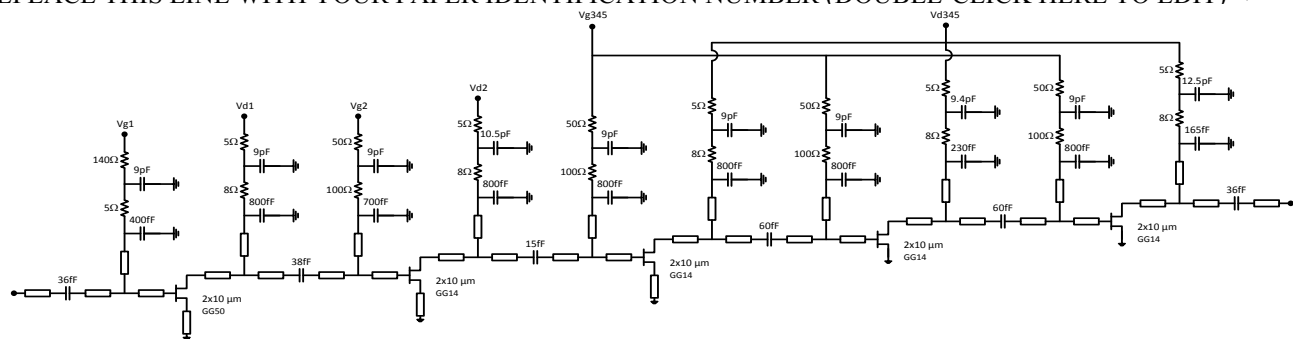


Fig. 2. Schematic diagram of the five-stage common-source single-ended amplifier circuit. The first stage is in 50 μm GCWG, whereas the subsequent stages are in 14 μm GCWG layout.

micrograph of the amplifier is shown in Fig. 1. The IAF transistor model includes small-signal and noise properties, the latter extracted with the Pospieszalski method [9]. This method consists in tuning the drain equivalent temperature associated to R_{ds} in order to fit the 50 Ω noise measurements. Transistors in common-source topology with a gate width in each stage of $2 \times 10 \mu\text{m}$ are chosen in order to achieve a good balance between gain, input matching and noise. The goal of the design is to achieve a noise figure below 5 dB on a packaged amplifier, a gain higher than 20 dB and input/output return loss better than 20 dB in the bandwidth 175-192 GHz. According to the small-signal performance of the transistor, five stages are necessary in order to accomplish the gain requirement at this frequency. Input, output and inter-stage matching networks are realized using series transmission lines with discrete impedances values of 50 Ω and 70 Ω . The design kit includes transmission lines in 50 μm ground-to-ground (GG50) layout as well as in 14 μm (GG14) layout. The GG50 layout has a 3 μm thick metal stack whereas the GG14 layout has a lower thickness of 0.3 μm . In order to minimize losses, and hence to improve noise performance, a GG50 layout is used for the input network. Interstage matching networks are designed with the more compact GG14 layout since the losses in the subsequent stages have a lower influence on the total noise figure of the amplifier. Interstage networks are optimized for achieving flat gain and to ensure stability inside and outside the frequency band. Inductive source feedback is used in the HEMTs of the first three stages to further improve stability. The drain bias networks are formed by a low value resistor and shunt MIM capacitors, whereas the gate bias networks have a large resistor. The gate resistor in the first stage affects the noise figure; consequently a low value of 5 Ω is used. A 50 Ω line of 650 μm length in GG50 layout is added after the output matching network in order to have a total chip length of 2 mm. The schematic diagram of the LNA is shown in Fig. 2.

IV. MEASUREMENT RESULTS

The amplifier performance is measured on-wafer. S-parameter measurements are performed using an Agilent PNA-X 4-port system, two VDI WR-4.3 T/R frequency extension modules, and two Cascade Infinity 260 microwave probes with back-to-back probes insertion loss of 3.8 dB at 183 GHz. A Cascade calibration substrate is used for an LRM-type calibration at the probe tip. For the noise measurements,

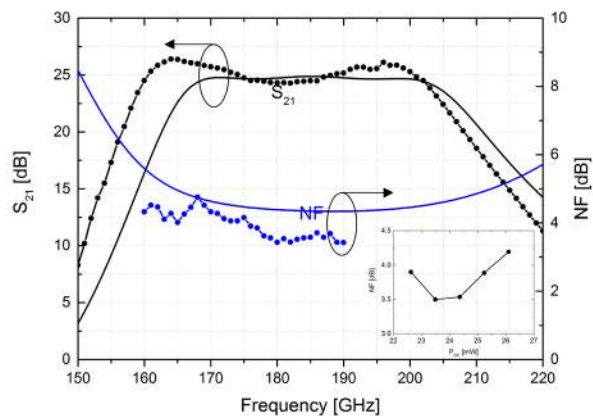


Fig. 3. Simulated (solid line) and on-wafer measured (circles) gain and noise figure of the amplifier. Inset figure shows NF vs P_{DC} at 183 GHz.

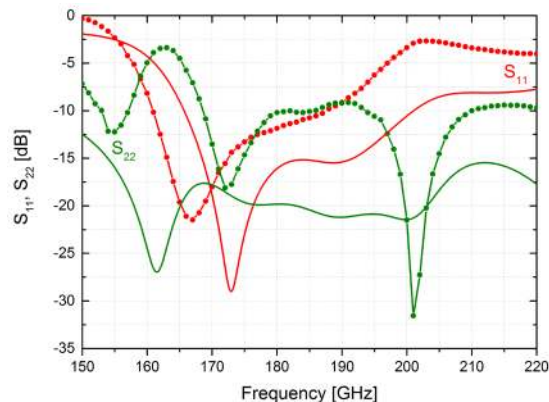


Fig. 4. Simulated (solid line) and on-wafer measured (circles) input and output reflection coefficients.

an ELVA noise source with an ENR around 10 dB is used. The receiver is built by a VDI sub-harmonic mixer, driven by a W-band source. Two Picoprobe Model 220 microwave probes are used. The output probe is matched to the mixer by an isolator. The scalar noise figure measurements are calibrated using an on-wafer line.

Fig. 3 shows measurements and simulation of gain (S_{21}) and noise figure (NF). The transistors are biased at 0.8 V and 300 mA/mm (6 mA), with exception of the first stage which is biased at a lower current density of 150 mA/mm (3 mA). At this bias, the DC power consumption (P_{DC}) of the whole amplifier is about 24 mW. The LNA exhibits a gain of 24.5 dB at 183 GHz with a variation of about ± 2 dB over the frequency band 160-200 GHz. The average value of the measured noise figure between 160 GHz and 190 GHz is 4 dB. Moreover, this average value decreases to 3.5 dB in the

TABLE I
COMPARISON OF REPORTED G-BAND MMIC LNAs

Ref.	Frequency Band (GHz)	NF (dB)	Gain (dB)	Gain/Stage (dB)	Gain/Power (dB/mW)	Number of Stages	P_{DC} (mW)	Device type	On-wafer/Packaged
[2]	200 – 225	5.3	12	6	0.67	2	18	InP HEMT	Packaged
[3]	170 - 205	4.9	18-23	6-7.7	-	3	-	35 nm InP HEMT	Packaged
[4]	170 - 185	3.4	17	5.7	-	3	-	35 nm InP HEMT	Packaged
[5]	160 - 170	3.7	12-16	4-5.3	0.55-0.73	3	22	35 nm InP HEMT	Packaged
[6]	150 - 220	-	18-26	6-8.7	-	3	-	50 nm InP HEMT	On-wafer
[7]	180 - 200	4.8	16	4	0.62	4	26	50 nm mHEMT	On-wafer
[8]	175 – 192	6.7	17-22	3.4-4.4	0.41-0.54	5	41	50 nm mHEMT	On-wafer
[10]	230 - 280	10	16-24	3.2-4.8	0.28-0.41	5	58	250 nm InP DHBT	On-wafer
[11]	200-220	11	10-18	1.4-2.6	0.22-0.4	7	44.5	32 nm CMOS	On-wafer
This work	178 – 185	3.5	24.5	4.9	1.02	5	24	50 nm mHEMT	On-wafer

frequency band 178-185 GHz. The removed back-end contribution is only 0.1 dB thanks to the high gain of the amplifier. In addition, on-wafer mapping showed an excellent uniformity with a spread of about 0.6 dB within 30 reticle cells. The noise figure of the LNA is expected to increase up to 4.5-5 dB in a packaged module, considering the insertion loss of a waveguide transition and wire-bond. The noise model used during the design tends to slightly overestimate the actual noise figure of the measured LNA. This might be due to the fact that the noise model at this frequency is an extrapolation of the model extracted up to 110 GHz. Inset of Fig. 3 shows NF at 183 GHz as a function of P_{DC} when sweeping the current density of the first stage from 100 mA/mm up to 300 mA/mm in steps of 50 mA/mm and with drain bias fixed at 0.8 V. From this plot it is clear that the optimal first stage bias current for noise performance ranges between 150 and 200 mA/mm. Simulation and measurements of input (S_{11}) and output (S_{22}) reflection coefficients are shown in Fig. 4. The amplifier is well matched since the measured S_{11} and S_{22} are -11 dB and -10 dB, respectively, at 183 GHz. Moreover, they are both better than -9 dB up to 190 GHz. The deviation from simulated values can be related to process variations as well as to parasitic modes propagating through the substrate and on the MMIC surface. Table I summarizes the performance of the presented LNA against previously reported G-band designs. This comparison shows excellent performance in terms of gain/stage and DC power consumption, combined with the lowest noise figure reported to date for a mHEMT based MMIC LNA operating at 183 GHz.

V. CONCLUSION

The design and characterization of a 183 GHz LNA, optimized for the MetOp-SG Microwave Sounder, Microwave Imager and Ice Cloud Imager instruments are presented. The five-stage amplifier is fabricated using the 50 nm mHEMT technology process. On-wafer measurement results have shown an average noise figure of 3.5 dB in the frequency band 178-185 GHz. These noise results are the lowest reported so far for a 50 nm mHEMT MMIC operating at 183 GHz. Moreover, the LNA exhibited a gain of 24.5 dB and a dc power consumption of only 24 mW. This study improves the current state-of-the-art for the mHEMT technology, pushing it even closer to the best results reported for 35 nm InP MMIC LNAs. Further enhancements of noise and gain performance are expected with the development of the 35 nm mHEMT technology node.

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