26.3 A 19GHz 0.5mW 0.35μm CMOS Frequency Divider with Shunt-Peaking Locking-Range Enhancement[1]

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A frequency divider is an essential building block and one of the major sources of power dissipation in widely-used frequency synthesizers. As the output frequency of the synthesizer increases, the trade-off between the speed and power dissipation of dividers becomes more critical. Existing frequency-division techniques can be categorized into two groups: wide-band flip-flop-based and narrow-band resonator-based. The former suffer from higher power dissipation due to the complete charging and discharging of capacitances during each cycle, which results in unnecessary energy loss. Although dynamic loading [1] can be used to alleviate this problem to some extent, the fundamental problem of energy loss still remains. On the contrary, narrow-band injection-locked frequency dividers (ILFD) [2] dissipate a fraction of the energy stored in the tank, which is determined by the quality factor, Q, of the resonator, in every cycle. Therefore, they have fundamentally lower power dissipation than wide-band dividers. Due to their narrow-band nature, ILFDs work in a limited frequency range (locking range). To achieve a larger locking range, an ILFD can use varactors to track the free-running frequency of the previous-stage voltage controlled oscillator (VCO) [2]. In this paper, shunt-peaking is used as an alternative approach to further increase the locking range and lower the power dissipation at higher frequencies.

In Reference 2, the locking range found to be proportional to the injected-signal voltage amplitude using Adler's model [3]. However, the injected signal is not always mixed with the intrinsic signal in the voltage domain, so it is not clear how this model can be directly applied to many high-frequency circuit implementations. In this case, it is preferable to use power instead of voltage to describe the injection phenomenon. Also, it is important to distinguish between the internal and external injection power. The internal injection power, i.e., the power injected into the oscillator core, determines the locking range of the ILFD. Therefore, the locking range can be enhanced by maximizing the internal injection power using the same external injection power, i.e., maximizing the power gain from the external injection point to the internal injection point. In this context, the external injection power is still referred to as injection power for simplicity since this is power provided by the previous stage and is what can be measured more easily.

The differential LC oscillator of Figure 26.3.1 is a good candidate for ILFDs because the tail node (the drain of the tail transistor, M_{tail}) offers natural frequency doubling. In practice, the signal is injected into the gate of M_{tail}, while the internal injection point is at the tail node, which has a large parasitic capacitance, C_{tail}, consisting of C_{gd} and C_{db} of M_{tail} as well as C_{sb} of M_1 and M_2, as shown in Figure 26.3.2. Unfortunately, C_{tail} significantly lowers the effective internal injection power which otherwise can be used for injection locking. To remedy the power loss on C_{tail}, a shunt inductor, L_{shunt}, is introduced to resonate with C_{tail} at the injection frequency, f_i, as shown in Figure 26.3.2. Consequently, the impedance at the tail node increases at f_i and so does the internal injection power. Another way to look at this effect is that M_{tail}, C_{tail}, and L_{shunt} form a tuned amplifier with output power peaking at f_i. Therefore, this technique is referred to as shunt-peaking locking-range enhancement. A capacitor, C_{shunt}, in series with L_{shunt} serves as a dc block.

Two ILFDs with input frequencies of 9GHz and 19GHz, using this shunt-peaking locking-range enhancement technique with 0.35μm CMOS transistors, each occupies 0.6x0.5mm^2, including the pads. Inductors L_1 and L_2 in Figure 26.3.1 are 8.5nH and L_{shunt} is 2nH in the 9GHz ILFD. Inductor L_1 and L_2 are 3nH and L_{shunt} is 1nH in the 19GHz ILFD.

The measurement setup is shown in Figure 26.3.3. To measure injection power correctly, a directional coupler must be inserted between the signal generator and the injection port, with a power meter at the coupling port to measure the injection power. Two one-port s-parameter measurements are necessary to measure the loss from the cables, adaptors and probe between the output of the directional coupler and the ILFD input as well as to measure the reflection coefficient at the input. The measured injection power can be adjusted accordingly to obtain the actual injection power using this calibration process.

To verify the effectiveness of shunt-peaking locking-range enhancement, each ILFD is measured twice before and after disconnecting the shunt-peaking circuitry using a laser, and the results from both measurements are compared in Figure 26.3.4 and Figure 26.3.5 for the 9GHz and 19GHz ILFDs, respectively. The tail current increases with injection power. The power supply voltage is 1.2V. The 9GHz ILFD achieves a locking range of 1490MHz (8.38-9.87GHz, 17%), with the injection power of +2dBm and tail current of 1.1mA, compared to 840MHz (8.37-9.21GHz, 9%), 2.4dBm and 1.5mA without shunt-peaking. This corresponds to 77% improvement in locking range. The 19GHz ILFD achieves a locking range of 1350MHz (18.01-19.36GHz, 7%) with the injection power of +5dBm and tail current of 1mA. It can also operate at 0.37mA with an injection power of -10dBm to achieve a locking range of 760MHz (18.50-19.26GHz). The relative locking-range improvement is smaller than that of the 9GHz ILFD due to an inadvertent mismatch in the center frequency of the shunt-peaking network. Figure 26.3.6 shows the phase noise performance of the free-running 19GHz ILFD, as well as the phase noise of the signal source and the locked output. The locked output is not affected by the poor phase noise of the free-running oscillator and follows the phase noise of the injected signal with a 6dB offset. This is because any phase error in the ILFD oscillation is re-adjusted by the injected signal twice every cycle when the ILFD is locked, and thus does not contribute to the phase noise at the divider output.

The chip micrographs of the two shunt-peaking dividers are shown in Figure 26.3.7.

References:

[1] H. Wang, et al., "A 1.8V 3mW 16.8GHz Frequency Divider in 0.25μm CMOS," ISSCC Digest of Technical Papers, pp. 196-197, Feb. 2000.

[2] H. R. Rategh, et al., "A CMOS Frequency Synthesizer with an Injection-Locked Frequency Divider for a 5-GHz Wireless LAN Receiver," IEEE J. Solid-State Circuits, vol. 35, pp. 780-787, May 2000.

[3] R. Adler, "A Study of Locking Phenomena in Oscillators," Proc. IRE, vol. 34, pp. 351-357, June 1946.

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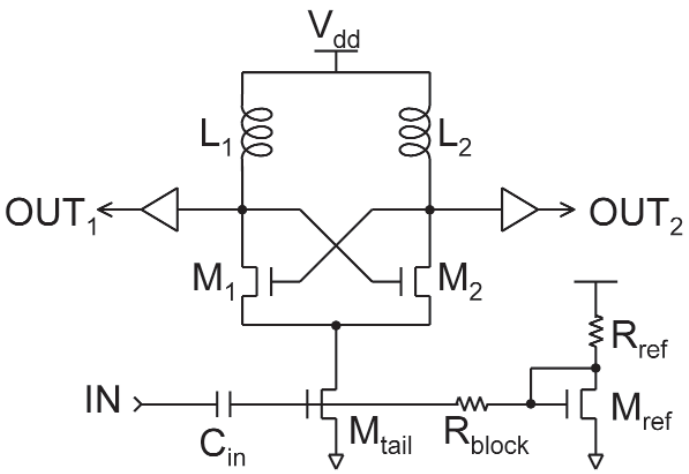

Figure 26.3.1: Standard ILFD.

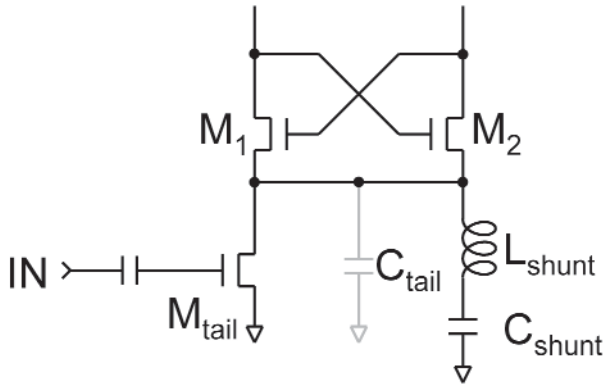

Figure 26.3.2: Enhanced ILFD with shunt-peaking.

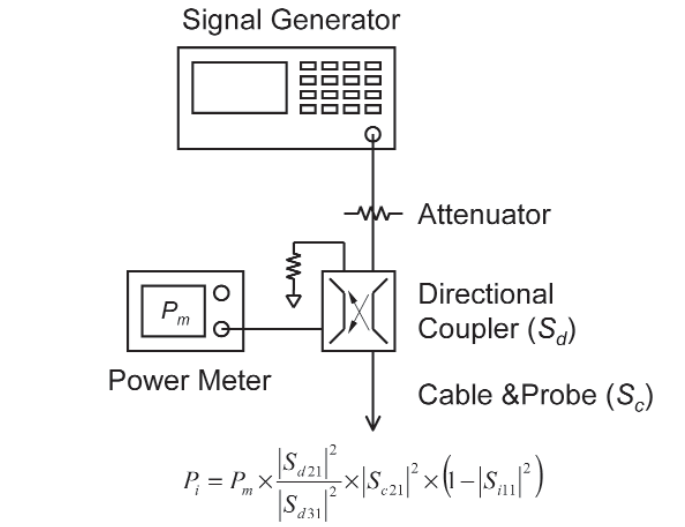

Figure 26.3.3: Measurement setup.

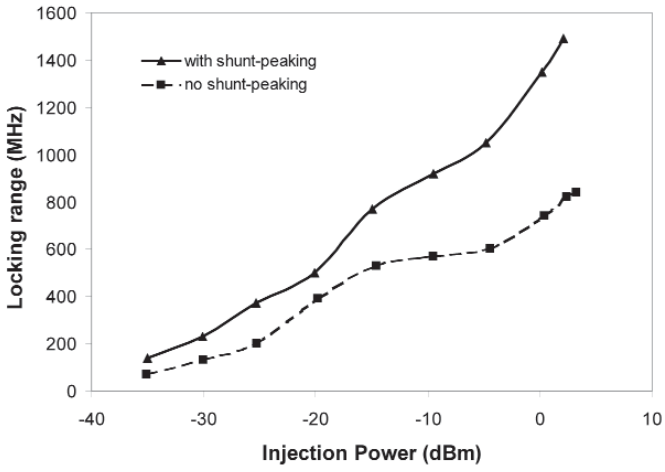

Figure 26.3.4: Locking range vs. injection power for 9GHz ILFD.

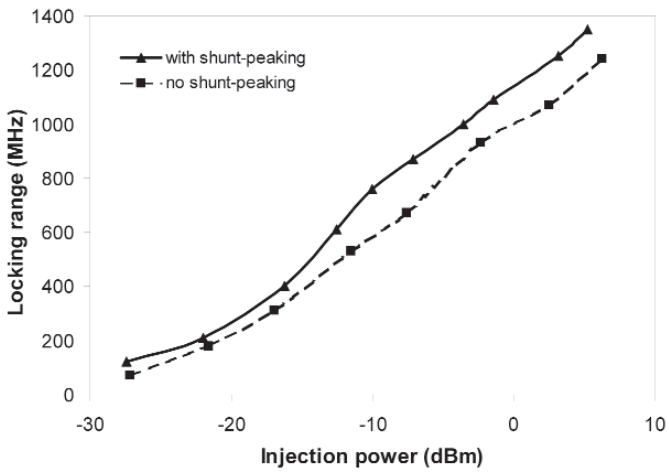

Figure 26.3.5: Locking range vs. injection power for 19GHz ILFD.

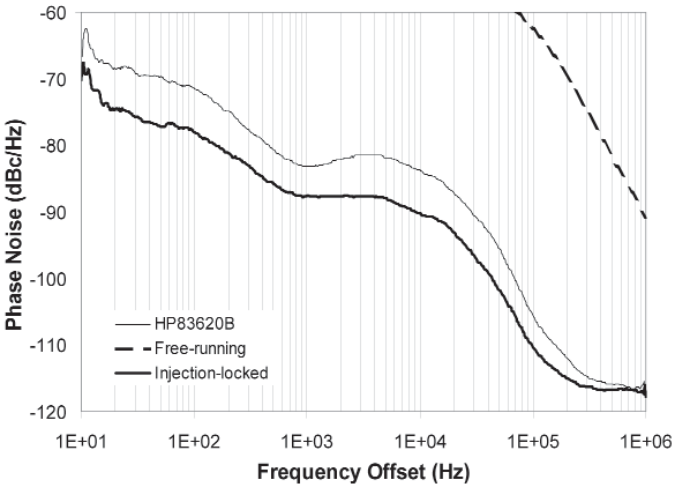

Figure 26.3.6: Phase noise performance.

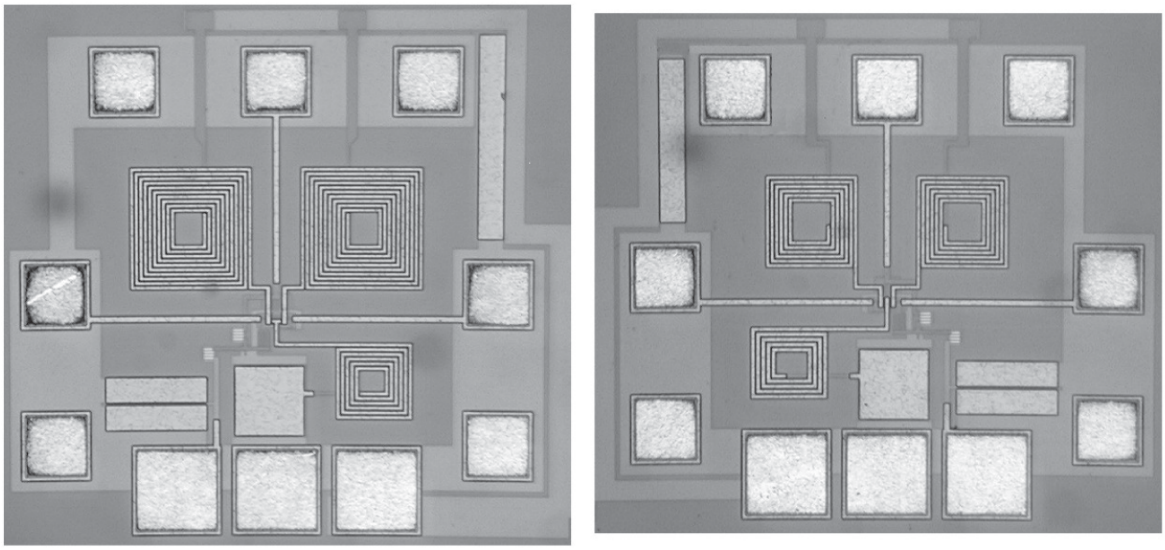

Figure 26.3.7: Chip micrographs.

