# A 1V 11fJ/Conversion-Step 10bit 10MS/s Asynchronous SAR ADC in $0.18 \mu \mathrm{~m}$ CMOS 

Chun-Cheng Liu ${ }^{1+}$, Soon-Jyh Chang ${ }^{1}$, Guan-Ying Huang ${ }^{1}$, Ying-Zu Lin ${ }^{1}$, Chung-Ming Huang ${ }^{2}$<br>${ }^{1}$ Department of EE, National Cheng Kung University, Tainan, Taiwan (Email ${ }^{+}$: jasonkingleo@sscas.ee.ncku.edu.tw)<br>${ }^{2}$ Himax Technologies, Inc., Tainan, Taiwan


#### Abstract

This paper presents a 10 -bit SAR ADC using a variable window function to reduce the unnecessary switching in DAC network. At $10-\mathrm{MS} / \mathrm{s}$ and $1-\mathrm{V}$ supply, the ADC consumes only $98 \mu \mathrm{~W}$ and achieves an SNDR of 60.97 dB , resulting in an FOM of $11 \mathrm{fJ} /$ Conversion-step. The prototype is fabricated in a $0.18 \mu \mathrm{~m}$ CMOS technology.


## Introduction

The DAC switching network in [1] saves $81 \%$ switching energy and $50 \%$ total capacitance as compared to the conventional one. However, the signal-dependent comparator offset caused by the input common-mode voltage variation degrades the ADC performance. Hence, this paper presents a splitting monotonic switching procedure to maintain the common-mode voltage during bit cycling.

Besides, the conventional SAR ADCs apply a binary search algorithm to approach the closest digital code to match the input signal. In a typical conversion, the reference DAC is added or subtracted a binary-weighted voltage according to the comparator output in each bit cycles. In the last cycle, the difference between input signal and reference is less than one LSB. However, during the conversion, the difference increases when adds a large voltage to a small difference, that results in unnecessary energy wasted. Fig. 1 shows the concept of our idea. When the difference is small, this ADC does not add or subtract any voltages until the remaining bit cycling operations could not reduce the difference to less one LSB. A variable window function is presented to ensure the difference does not increase during the conversion. The multi-comparator SAR ADCs [2-3] are able to reduce the risk of metastability and power consumption in comparators. This work uses the multi-comparator concept to perform the variable window function to reduce the unnecessary switching in DAC network. The method saves the power consumption in comparators, capacitor networks and switch buffers at the expense of little hardware overhead.

## Circuit Description

Fig. 2 shows the schematic of the proposed SAR ADC. Similar to the split capacitor array [4], the first 4 MSB capacitors in the capacitor array are all split into two equal sub-capacitors to perform the splitting monotonic switching method. At the sampling phase, the top plates of all capacitors capture the input signal via the bootstrapped switches. At the


Fig. 1: The approximations of conventional and proposed methods.


Fig. 2: The proposed SAR ADC.
same time, the bottom plates of capacitors $C_{1 \mathrm{a}} \sim C_{4 \mathrm{a}}$ are reset to ground, and the others ( $C_{1 \mathrm{~b}} \sim C_{4 \mathrm{~b}}$ and $C_{5} \sim C_{9}$ ) are reset to $V_{\text {ref }}$. Next, the comparators do the first comparison. The capacitor $C_{1 \mathrm{~b}}$ on the higher voltage potential side is pulled down to ground. On the lower voltage potential side, the capacitor $C_{1 \mathrm{a}}$ is pulled up to $V_{\text {ref }}$. Therefore, the common-mode voltage does not change. To avoid complicated control logic and layout routing, the splitting monotonic switching method is only applied to the first 4 MSB capacitors. The remaining operations still use the switching method in [1]. The common-mode voltage variation is diminished to only $1 / 16$ of that in [1]. The comparator dynamic offset problem becomes negligible in this 10 -bit case.
Fig. 3 shows how to reduce the unnecessary switching in DAC network. Take the Phase 1 as an example. When the voltage difference of input signal and reference is located in the "No Switching" region, even no capacitors switched in this cycle, the remaining bit cycling operations could reduce the difference to less than one LSB. Hence, this ADC does not switch any capacitors in this bit cycle. On the contrary, when the voltage difference is located in the "Switching" region, this ADC switches the relative capacitors according to the comparison. Otherwise the remaining bit cycling operations could not reduce the difference to less than one LSB.
Two coarse comparators and a sub-DAC are added to perform the function as shown in Fig. 3. In order to achieve a variable window function in different bit cycles, the reference voltage $V_{\mathrm{r}}$ must be variable. Fig. 4 shows the variable window


Fig. 3: The graph of proposed switching procedure.
function and $V_{\mathrm{r}}$. A 6-bit sub-DAC generates the variable $V_{\mathrm{r}}$. The real $V_{\mathrm{r}}$ in this ADC is large than the ideal value about 8 LSB, the real window size is a little smaller than the ideal one. Therefore, this ADC has about 8-LSB margin to tolerance the sub-DAC and coarse comparator offset errors. For best efficiency, the mechanism only used in first 4 MSB capacitors. Even includes the overhead of the 6-bit sub-DAC, this method saves $40 \sim 45 \%$ power dissipation in the capacitor network and switch buffers compared to [1]. Fig. 5 shows the digital error correction logic, which consists of only 4 full-adders.

This ADC uses a dynamic comparator with a p-type input pair. The dynamic comparator does not consume static current and hence is suitable for an energy efficient design. Internal control logic triggered by the global clock and comparator output asynchronously generates internal control clocks, which avoids a high frequency clock generator and makes the sampling rate equal to the clock rate. This ADC uses metal-oxide-metal (MOM) capacitors to construct the capacitor array. The unit capacitor is about 5 fF , composed of 5 metal layers in a $4 \times 4.8 \mu \mathrm{~m}^{2}$ area. The total input capacitance is 2.5 pF each terminal. According to simulation result, this ADC saves about $17.6 \%$ power consumption than the architecture in [1]. Besides, with less capacitors switched, the DNL and INL performance was improved especially around the middle of output codes. Hence, the linearity of ADC is enhanced.

## Experimental Result

The prototype is fabricated in a $0.18-\mu \mathrm{m}$ CMOS technology. The micrograph is shown in Fig. 6. The active core area is only $330 \times 260 \mu \mathrm{~m}^{2}$. At $10-\mathrm{MS} / \mathrm{s}, 1-\mathrm{V}$ supply and $1-\mathrm{MHz}$ input stimulus, the measured static performances are plotted in Fig. 7. The peak DNL and INL are $+0.28 /-0.34$ LSB and $+0.23 /-0.38$ LSB, respectively. The measured SNDR and SFDR are 60.97 and 79.4 dB , respectively. The resultant ENOB is 9.83 bit. Fig. 8 plots the measured SFDR and SNDR versus input frequency and FFT spectrum with input frequency closes to Nyquist frequency. The analog circuit, including the $\mathrm{S} / \mathrm{H}$ circuit and comparators, consumes $32 \mu \mathrm{~W}$, and the digital control circuit draws $50 \mu \mathrm{~W}$. The capacitor networks and Sub-DAC consume $16 \mu \mathrm{~W}$. The total power consumption of the ADC is $98 \mu \mathrm{~W}$. The prototype achieves an FOM of only $11 \mathrm{fJ} /$ conversion-step. Table I summarizes the comparison to state-of-the-art ADCs.

## Acknowledgement

The authors would like to thank the Chip Implementation Center, Taiwan, for supporting the chip implementation and measurements.

## References

[1] C. C. Liu, S. J. Chang, G. Y. Huang and Y. Z. Lin, "A 0.92 mW 10-bit $50-\mathrm{MS} / \mathrm{s}$ SAR ADC in $0.13 \mu \mathrm{~m}$ CMOS process," IEEE Symposium on VLSI Circuits, Jun. 2009, pp. 236-237.
[2] J. J. Kang and M. P. Flynn, "A 12b $11 \mathrm{MS} / \mathrm{s}$ successive approximation ADC with two comparators in $0.13 \mu \mathrm{~m}$ CMOS," IEEE Symposium on VLSI Circuits, Jun. 2009, pp. 240-241.
[3] W. Y. Pang, C. S. Wang, Y. K. Chang, N. K. Chou and C. K. Wang, "A 10-bit 500-KS/s Low Power SAR ADC with Splitting Comparator for Bio-Medical Applications," IEEE Asian Solid-State Circuits Conference, pp. 149-152, Nov. 2009.
[4] B. P. Ginsburg and A. P. Chandrakasan, " $500-\mathrm{MS} / \mathrm{s} 5-\mathrm{bit}$ ADC in $65-\mathrm{nm}$ CMOS with split capacitor array DAC," IEEE J. Solid-State Circuits, vol. 42, no. 4, pp. 739-747, Apr. 2007.


Fig. 4: Variable window function.


Fig. 5: Digital error correction logic.


Fig. 6: Chip micrograph.


Fig. 7: Measured DNL and INL.


Fig. 8: Measured dynamic performance
Table I. Comparison to state-of-the-art works

| Specification (Unit) | $[1]$ | $[2]$ | $[3]$ | This work |
| :---: | :---: | :---: | :---: | :---: |
| Technology | $0.13 \mu \mathrm{~m}$ | $0.13 \mu \mathrm{~m}$ | $0.18 \mu \mathrm{~m}$ | $\mathbf{0 . 1 8} \mu \mathrm{~m}$ |
| Supply Voltage (V) | 1.2 | 1 | 1 | $\mathbf{1}$ |
| Resolution (bit) | 10 | 12 | 10 | $\mathbf{1 0}$ |
| Sampling rate (MHz) | 50 | 11 | 0.5 | $\mathbf{1 0}$ |
| ENOB (bit) | 8.48 | 10.1 | 9.4 | $\mathbf{9 . 8 3}$ |
| Power ( $\mu \mathrm{W}$ ) | 920 | 3570 | 42 | $\mathbf{9 8}$ |
| FOM (fJ/Conv.-Step) | 52 | 311 | 124 | $\mathbf{1 1}$ |
| Active area (mm ${ }^{2}$ ) | 0.075 | 0.7 | 0.24 | $\mathbf{0 . 0 8 6}$ |

