A 2.18pJ/conversion, 1656um2 Temperature Sensor with a 0.61pJ K2 FoM and 52-pW Stand-By Power

A 2.18-pJ/conversion, 1656-μm^2 Temperature Sensor With a 0.61-pJ·K^2 FoM and 52-pW Stand-By Power

Kevin Pelzers, Haoming Xin, *Fellow, IEEE*, Eugenio Cantatore, *Fellow, IEEE*, and Pieter Harpe, *Senior Member, IEEE*

***Abstract*—This letter describes a miniature, ultra low power, all-dynamic temperature sensor based on a duty-cycled resistive transducer bridge and a 9-bit asynchronous SAR ADC in 65-nm CMOS. It features a novel floating bridge technique and automatic power gating to achieve the lowest reported power consumption. It consumes 2.18 pJ per conversion and has an RMS resolution of 0.53 K, leading to an FoM of 0.61 pJ·K^2. A standby power of 52 pW allows a high power-efficiency, even at low sample rates. It occupies 36×46 μm of chip area and has a sensing range from −20 °C to 120 °C.**

***Index Terms*—Duty-cycling, dynamic, Internet-of-Things (IoT), low power, power gating, resistive bridge, SAR ADC, temperature sensor.**

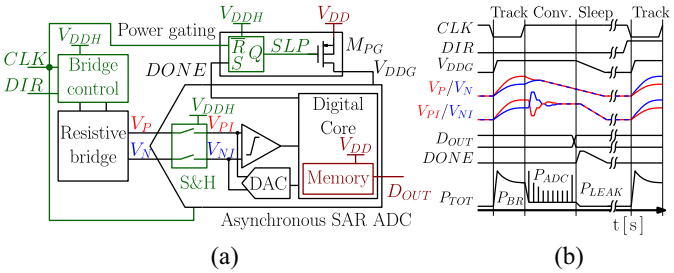

Fig. 1. (a) Fully dynamic temperature sensor with automatic power gating. (b) Timing: conversion started by *CLK*, *DONE* triggers power gating when finished.

I. Introduction

Temperature sensing in Internet-of-Things (IoT) and environmental monitoring applications typically needs ultra low-power circuits with moderate accuracy, low operating speeds, and/or long standby times. These applications benefit from low cost and small size, enabling integration in Systems-on-Chip (SoCs).

The state-of-the-art low-power sensors may have to compromise on power efficiency [1], [2] or require a larger than average silicon area [2], [3]. The state-of-the-art miniature sensors [4], [5] are mostly designed for thermal monitoring of high-power ICs and not as energy efficient. Designs that combine and balance high efficiency, low power, and small size are generally not leading at these individual performance parameters [6]. This letter aims for the state-of-the-art low absolute power while maintaining a competitive FoM, circuit size, and inaccuracy.

In mixed-signal systems, power is split between static and dynamic (switching) contributions (1). In low power systems which are not duty-cycled, the static power consumption P_{stat} is typically dominated by amplifier or transducer bias currents, limiting the power-efficiency at low operating speeds

$$P_{\text{tot}} = P_{\text{stat}} + E_{\text{dyn}} \cdot f_s. \tag{1}$$

This design [Fig. 1(a)] employs a fully dynamic architecture [3] to reduce static power consumption to leakage currents only and to allow fast duty-cycling of the sensor. This allows it to function efficiently at low speed but also to operate at high speed to implement burst measurements.

The fully dynamic architecture uses a duty-cycled resistive bridge. A resistive bridge has high temperature sensitivity due to its differential nature and because it enables combining both positive and negative temperature coefficient resistors [7], while duty-cycling helps optimization of circuit area and power consumption. Additionally, a novel floating bridge technique uses tri-state switching to reduce leakage currents in the duty-cycling switches.

To measure the output of the resistive bridge, this letter uses a 9-bit asynchronous SAR ADC with a unit-length DAC layout [8], which combines power efficiency and small size. Additionally, it introduces a novel automatic power gating scheme, which decouples the system leakage power from that of the ADC, reducing overall leakage current and allowing optimization of the ADC for performance and low dynamic power consumption.

A secondary V_{DDH} supply is used next to the core V_{DD} supply to reduce leakage current in the duty-cycling and power gating switches. The value of this supply is higher than V_{DD} but not critical, so an unregulated (battery) voltage or shared voltage from an SoC may be used.

II. Proposed Temperature Sensor

Fig. 1(a) shows the top-level schematic of the circuit. It uses a duty-cycled 100-kΩ resistive Wheatstone bridge, interfacing to a 9-bit asynchronous SAR ADC. Fig. 1(b) shows a timing diagram. V_{DD} is applied to the bridge and ADC at the falling *CLK* edge by the Bridge control block and M_{PG}, respectively. Within the *CLK* low time (100 ns), the bridge output voltages V_p and V_n as well as the internal ADC supply V_{DDG} settle and the ADC is initialized to a known state. A rising *CLK* edge powers down the resistive bridge and triggers the AD conversion. After conversion, the *DONE* signal, generated by the ADC, triggers the power gating block and V_{DDG} is disconnected to reduce leakage. The conversion memory remains powered to preserve the output data. The DIR signal implements double-sided measurements [3], a form of system-level correlated double sampling (CDS), which consists of taking two measurements at opposite bridge polarity. Taking the difference of these digitized samples, this technique improves accuracy by averaging DAC mismatch errors. Additionally, flicker noise and ADC offset are reduced. Currently, the CDS output is calculated off-chip. Implementing it on-chip requires a digital subtractor, but a one-sample memory remains sufficient. The circuit uses a core voltage V_{DD} of 0.6 V and a secondary 1 V V_{DDH} supply to

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The authors are with the Integrated Circuits Group, Eindhoven University of Technology, 5600MB Eindhoven, The Netherlands (e-mail: k.m.p.pelzers@tue.nl).

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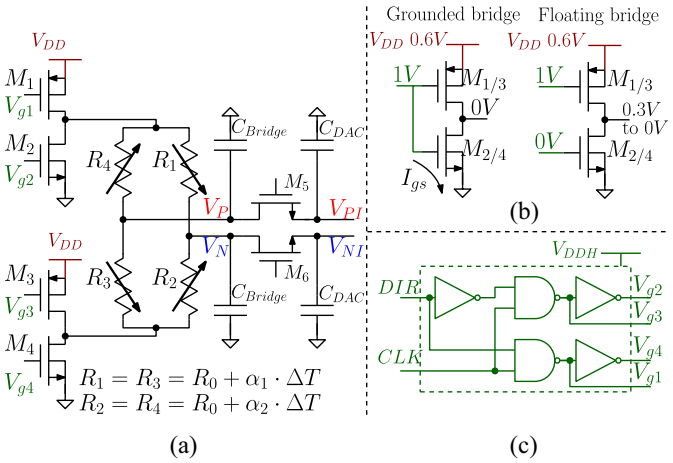

Fig. 2. (a) Resistive transducer bridge, (b) floating bridge technique, and (c) control logic.

reduce leakage power in the bridge control and power gating blocks, as will be explained in Sections II-A and II-C.

A. Resistive Bridge

A resistive transducer bridge [Fig. 2(a)] offers a differential output proportional to its supply. This can be conveniently connected to a differential ADC directly. By reusing the bridge supply as the ADC's DAC reference, a ratiometric measurement with improved PSRR is obtained. Thanks to the relatively high sensitivity of the resistive bridge, a low-power low-resolution ADC can be used without preamplification, enabling an all-dynamic design [3]. R_{1-4} form the temperature sensitive resistive bridge, which has a parasitic capacitance C_{Bridge}. M_{1-4} enable duty-cycling and CDS measurements. M_{5-6} are the sample & hold switches of the ADC and C_{DAC} is the aggregated DAC capacitance of the ADC. Duty-cycling limits static power dissipation and changes the bridge optimization strategy. In an always-on design, the theoretical energy consumed per conversion by the bridge is given by (2), and for minimum energy R_0 should be maximized, leading to large area. In a duty-cycled design with a 5τ settling time, assuming all nodes are discharged between samples, the dynamic energy consumed is given by (3), where the parasitic C_{Bridge} is proportional to R_0. In this case, minimizing energy consumption requires reducing R_0 (thereby reducing C_{Bridge}), which simultaneously reduces the chip area. However, when R_0 is too small, the size of the switches M_{1-4} needs to be prohibitively large, causing increased area and leakage. A resistance of 100 kΩ was chosen as a compromise between $E_{\text{dyn Bridge}}$, switch leakage current, and chip area

$$E_{\text{stat Bridge}} = \frac{V_{DD}^2}{R_0 \cdot f_s} \tag{2}$$

$$E_{\text{dyn Bridge}}(5\tau) = 3(C_{\text{Bridge}} + C_{DAC})V_{DD}^2. \tag{3}$$

The bridge output voltage $V_p - V_n$ is inherently nonlinear with the sensed temperature, as shown in (4). Here, $\alpha_{1,2}$ are the linear temperature coefficients of resistors $R_{1,2}$, R_0 is the nominal resistance, and ΔT is the deviation from the nominal temperature. Since this inherent nonlinearity is systematic, it is compensated by a fixed correction using off-chip post-processing on a nonpower-constrained base station, as will be shown in Section III. $R_{1,3}$ are N-type diffusion resistors with a positive α_1, while $R_{2,4}$ are P-type polysilicon resistors with a negative α_2. These resistors are selected for their small size, low parasitic capacitance, and medium sensitivity

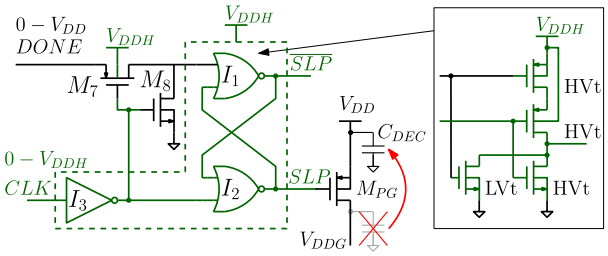

Fig. 3. Power gating circuit with CLK priority and modified trip-points in I_1 using high and low threshold (HVt and LVt) transistors.

$$V_p - V_n = \frac{(\alpha_1 - \alpha_2)V_{DD} \cdot \Delta T}{(\alpha_1 + \alpha_2)\Delta T + 2R_0}. \tag{4}$$

Similar to [3], the duty-cycling switches M_{1-4} are controlled by V_{DDH}, providing a positive gate–source voltage to $M_{1,3}$ to reduce drain–source leakage. In this letter, M_{1-4} are controlled as tri-state switches rather than inverters [Fig. 2(b)]. This allows the bridge to remain floating during the sleep state, rather than being tied to V_{DD} or ground, lowering the gate–source leakage through $M_{2,4}$. At the start of a conversion, all bridge nodes float at approximately $V_{DD}/2$. This improves sensitivity and linearity by reducing leakage currents (and their variation due to mismatch and temperature) through $M_{5,6}$, thereby preventing charge loss from the ADC's DAC. The V_{DDH} supply is used to provide a positive gate–source voltage to switches $M_{1,3}$, reducing drain–source leakage current at the cost of added leakage through their gates and in the control logic [Fig. 2(c)]. In simulation, the leakage of the bridge and control logic powered by V_{DD} would consume 1593 pW. The floating bridge concept would reduce it to 175 pW, while using V_{DDH} for the logic would reduce it to 111 pW. Combining both techniques reduces the leakage to 31 pW.

The required bridge on-time ($5\tau = 100$ ns) is independent of the operating frequency and currently generated off-chip. It could be implemented on-chip by means of an RC delay-line. At operating frequencies above 5 kHz, floating operation enables partial charge conservation on C_{Bridge}, saving 5% conversion energy compared to low speeds. The accuracy remains identical, as the bridge can always settle within 100 ns.

B. SAR ADC

The power consumption of SAR ADCs is mainly dynamic (apart from the static leakage). They have excellent power efficiency, making them ideal for a low power, all-dynamic design. This ADC uses the unit-length capacitor layout technique for DAC matching [8] and places the DAC in metal layers above the active area of both the ADC and transducer, with shielding layers in between, to minimize circuit area. This stacked design is shown in Fig. 6. A 9-bit asynchronous SAR ADC is implemented, with an input swing of ±155 mV and a total DAC capacitance of 256 fF, limited by the allowable kT/C noise. The energy-efficient dynamic comparator topology from [9] is used.

C. Automatic Power Gating

Power gating is a proven technique to reduce leakage power [10] and in this letter enables optimization of the ADC for dynamic power only, while the power gating switch M_{PG} and associated logic are optimized for low leakage. This design implements an automatic power gating scheme which does not require added external signaling. In Fig. 3, when CLK becomes low, the latch applies power to the ADC and initializes it to a known state. After the AD conversion

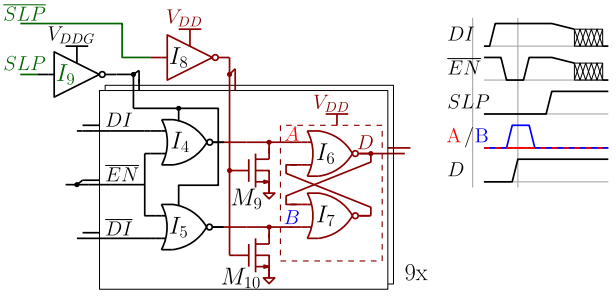

Fig. 4. Low leakage memory circuit with power gated inputs.

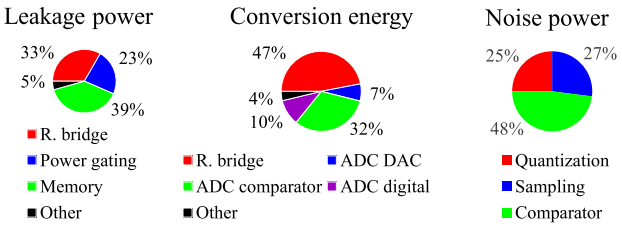

Fig. 5. Estimated distribution of power, energy, and noise without CDS at 27 °C.

finishes, *DONE* disables M_{PG} and disconnects V_{DDG}. During power-up, glitches can occur in the *DONE* signal, $M_{7,8}$ ensure priority of the *CLK* signal with minimal added leakage.

The latch is powered by V_{DDH} to reduce leakage of the 60-nm long by 12.8-μm wide power gating switch M_{PG} in a similar way as has been done in the bridge control (Section II-A), lowering the simulated overall leakage in the power gating circuitry from 1.6 nW to 17 pW. The NOR latch combines level shifting and memory to decrease leakage. One input of I_1 has a modified trip-point to interface the V_{DD}-level *DONE* signal to the V_{DDH}-level domain in a robust way, while the latch recovers and stores the signal. The transistor logic state minimizes leakage during sleep, for example, the drain–source voltages of various leakage-dominant devices such as $M_{7,8}$ and the LVt transistor in I_1 are at 0 V during sleep. At low operating speeds, the charge on V_{DDG} is fully drained between conversions by the leakage of the ADC. To minimize charge loss, the decoupling capacitance C_{DEC} downstream of M_{PG} is minimized and instead placed upstream of M_{PG}, on-chip. Consequently, a wider (thus higher leakage) switch M_{PG} is required to ensure low power supply impedance.

In sleep mode, the conversion memory remains active (Fig. 4). It uses a modified gated SR latch, with data input *DI*, latch disable input $\overline{EN}$, and output *D*. Memory corruption must be avoided while the parasitic capacitance on V_{DDG} is drained due to leakage during sleep mode. The local supply of buffers I_4 and I_5 is disabled by I_9 to prevent unwanted transients while M_9 and M_{10} ensure a defined state for I_6 and I_7 during sleep. Minimizing the amount of powered gates in this way leads to a leakage power of 2 pW per memory cell.

D. Power, Noise, and Area Breakdown

The estimated distribution of power and noise power is shown in Fig. 5. Power, energy, and comparator noise are simulated, while quantization and sampling noise are calculated. In terms of leakage, the power consumed by the transducer bridge, power gating logic, and memory are balanced. The conversion energy is dominated by the resistive bridge, which is in a tradeoff with lower leakage as explained in Section II-A. Following this, the dynamic comparator in the ADC uses most power but also contributes the highest noise. The compact layout of the sensor is made possible by the duty-cycled resistive bridge explained in Section II-A and the DAC design and placement discussed in Section II-B. This allows for a very compact integration, as shown in Fig. 6.

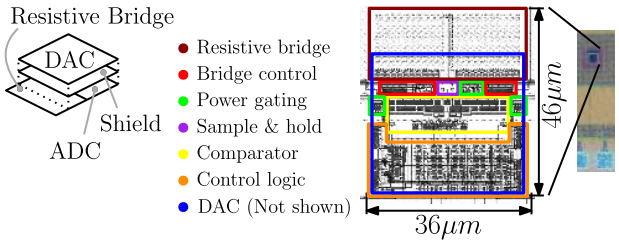

Fig. 6. Die photograph, IC layout, and 3-D sketch with DAC implemented in metal layers 6 and 7 above the other blocks separated by a shield on metal layers 4 and 5.

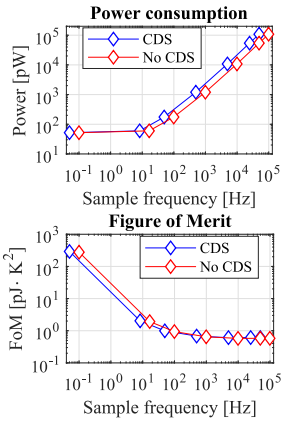

Fig. 7. Power consumption and FoM versus sample frequency, measured at room temperature.

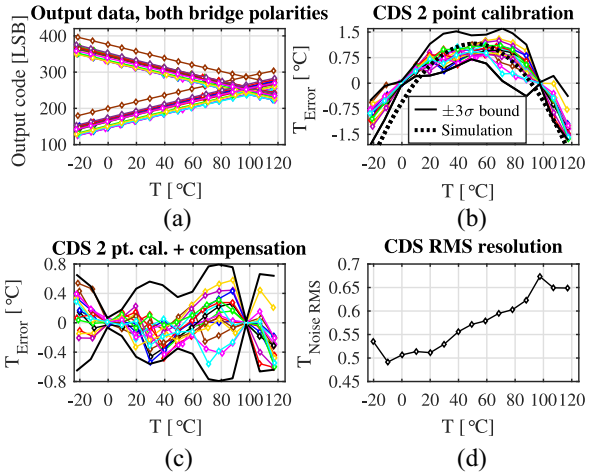

Fig. 8. (a) Sensor output code of both bridge polarities and (b) and (c) accuracy of output with $\pm 3\sigma$ boundaries of 16 samples. (d) RMS resolution.

III. Measurement Results

The temperature sensor is fabricated in a 65-nm CMOS technology and occupies 1656 μm^2. Power dissipation and FoM as a function of the operating frequency are shown in Fig. 7. The sensor has a conversion energy of 1.1 pJ at 99 kHz without CDS or 2.18 pJ at 49.5 kHz with CDS. A leakage power of 52 pW is measured

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

	This work			[3]	[2]	[6]	[7]	[11]	[4]	[5]
Type	Res			Res	MOS	MOS	Res	Res	BJT	MOS
Node $[nm]$	65			65	65	65	65	180	65	28
ADC	SAR			SAR	TDC	FDC	FDC	SD2	SD1	FDC
Area $[mm^2]$	0.0017			0.084[a]	0.15	0.013	0.007	0.12	0.003	0.001[b]
Temp. Range$[^\circ C]$	-20∼120			-10∼120	-20∼40	-20∼100	-40∼85	-55∼125	-10∼110	-5∼85
VDD $[V]$	0.6 and 1			0.6 and 1	0.5	0.5 and 0.9	0.85	1.8	1.3	0.9
Trim points	2/2[c]			2[c]	/	2	2	2[c]	2	1
	No CDS	With CDS								
Peak-peak inaccuracy $[K]$	4.3 / 2.5[c]	2.9 / 1.2[c]		0.63	3.86	4.5	0.24[d]	0.14 [d]	2.7[de]	2.7
Number of samples	16			10	4	7	16	20	25	21
Supply Sensitivity $[K/V]$	8.8 & 0.8[f]	2.6 & 0.6[f]		1	/	/	0.5	0.03	3 to 14	1.9
RMS resolution $[K]$	0.73	0.53		0.38	0.21	0.25	2.5m	0.16m	0.13	0.76
Conversion Time $[s]$	10μ	20μ		10μ	4.8	34.3m	1m	10m	4.1m	36μ
Sample frequency $[Hz]$	99k	49.5k	8.3	100k	0.208	29	1k	100	240	28k
Power$[nW]$	108[g]	108[g]	0.06[g]	571	0.113	0.64	68000	79000	111800	56000
Conversion Energy $[pJ]$	1.09	2.18	7.23	5.71	540	22	68000	790	460000	2000
FoM $[pJ \cdot K^2]$	0.59	0.61	2.0	0.82	23	1.4	0.43	0.02	7700	1200

[a]Includes other sensors. [b]11 sensor array + shared blocks, normalized to 1 sensor. [c]With fixed nonlinearity compensation
[d]3σ variation. [e]Includes supply sensitivity. [f]V_{DD} and V_{DDH}. [g]Excluding off-chip non-linearity compensation

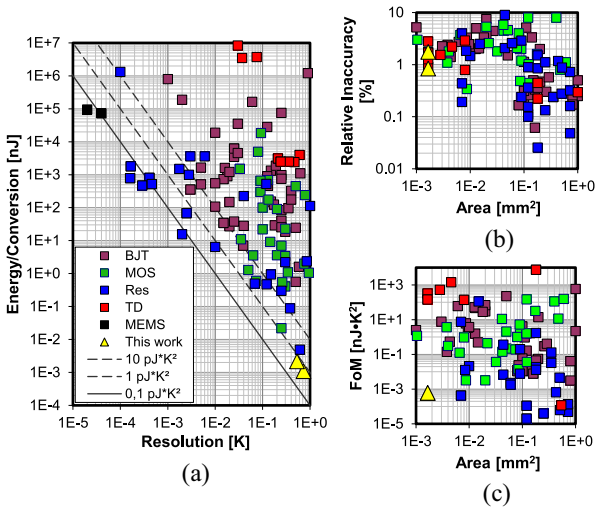

Fig. 9. Performance [1] with/without CDS with nonlinearity correction. (a) FoM. (b) Inaccuracy versus area. (c) FoM versus area.

at room temperature, which dominates the total power dissipation up to about 10-Hz sampling frequency. The circuit also works with V_{DDH} level supply voltages only but is not optimized for this operating mode: it will consume 2.8 times higher conversion energy and 30 times higher leakage. Fig. 8(a) displays the output codes for the two bridge polarities used in CDS. Fig. 8(b) shows the temperature error of 16 samples after an off-chip 2 point calibration applied to the CDS result, consisting mainly of a systematic nonlinearity (Section II-A). This inherent error is compensated for all sensors by a fixed batch correction based on averaged compensation using a third measurement point of all 16 samples [Fig. 8(c)]. Simulated nonlinearity could be used for compensation instead, but batch correction yields better accuracy. The RMS resolution for CDS measurements is 0.53 K at room temperature [Fig. 8(d)]. Table I and Fig. 9 show a performance summary of this letter and comparison against state-of-the-art. This letter achieves the lowest absolute power (Table I), the lowest conversion energy [Fig. 9(a)], a state-of-the-art FoM compared to similar low power designs [Fig. 9(a)], and a competitive inaccuracy and FoM for the given chip area [Fig. 9(b) and (c)].

IV. CONCLUSION

This letter presented a temperature sensor with a duty-cycled resistive bridge using a new floating bridge technique and existing system-level CDS measurement techniques. It used an SAR ADC with DAC capacitors above the active circuit area and implemented a novel automatic power gating scheme. This leads to the lowest reported conversion energy of 2.18 pJ and combines a competitive FoM of 0.61 pJ·K^2 with a small area of 1656 μm^2 and a reasonable inaccuracy of 1.2 K. At low speed, the power scales down to a lowest reported 60 pW.

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