A 2.5-V 10-b 120-MSample/s CMOS Pipelined ADC Based on Merged-Capacitor Switching

Sang-Min Yoo, Jong-Bum Park, Seung-Hoon Lee, and Un-Ku Moon

***Abstract*—This work describes a 10-b multibit-per-stage pipelined CMOS analog-to-digital converter (ADC) incorporating the merged-capacitor switching (MCS) technique. The proposed MCS technique improves the signal processing speed and resolution of the ADC by reducing the required number of unit capacitors by half in comparison to a conventional ADC. The ADC resolution based on the proposed MCS technique can be extended further by employing a commutated feedback-capacitor switching (CFCS) technique. The prototype ADC achieves better than 53-dB signal-to-noise-and-distortion ratio (SNDR) at 120 MSample/s and 54-dB SNDR and 68-dB spurious-free dynamic range (SFDR) for input frequencies up to Nyquist at 100 MSample/s. The measured differential and integral nonlinearities of the prototype are within ± 0.40 LSB and ± 0.48 LSB, respectively. The ADC fabricated in a 0.25-μm CMOS occupies 3.6 mm^2 of active die area and consumes 208 mW under a 2.5-V power supply.**

***Index Terms*—Analog-to-digital converter (ADC), merged-capacitor switching (MCS), multiplying ADC (MADC), pipeline.**

I. Introduction

THE dramatic growth in the high-tech sectors of the consumer market has created many unprecedented challenges in the area of integrated circuits. The present and future communication systems including high-speed modems and broadband wired and wireless communication subsystems require increasingly higher performance analog-to-digital converters (ADCs). The required level of accuracy can exceed 10 b at the conversion speed of hundreds of megahertz. The conventional pipelined architecture has been widely employed to meet the required performance in this arena due to properly managed tradeoffs between speed, power consumption, and die area [1]–[12]. Among a variety of pipelined ADCs, the multibit-per-stage architecture is more suitable for high resolution, as the single-bit-per-stage structure requires more stages, higher power consumption, and larger chip area. However, the multibit-per-stage architecture has a relatively low signal processing speed due to the reduced feedback factor in the closed-loop configuration of the amplifiers. In switched capacitor type multiplying digital-to-analog converters (MDACs) used in conventional pipelined ADCs, the mismatch between capacitors limits the differential nonlinearity (DNL) of ADCs. This is because each DNL step is defined by the random process variation of each unit capacitor value. A common centroid geometry layout technique can improve this capacitor matching for DNL, but it can not have an effect on random mismatch [13]. Naturally, increasing the capacitor size can directly improve the capacitor matching accuracy, but at the added cost of increased load capacitance. This means the amplifiers would dissipate more power or the ADC sampling speed would have to be reduced.

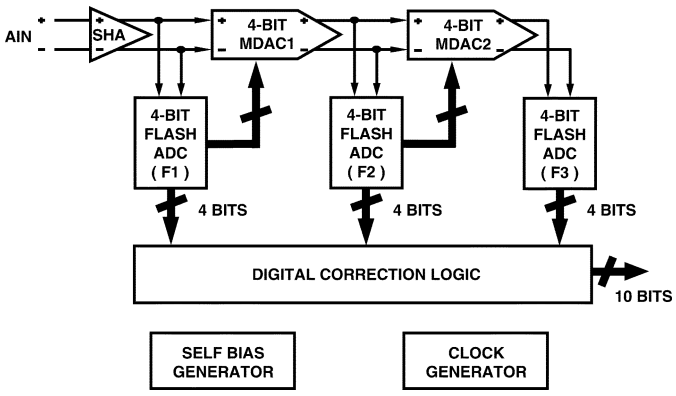

Fig. 1. Proposed 10-b 120-MSample/s ADC.

In this paper, the merged-capacitor switching (MCS) technique is proposed to improve the sampling rate and the resolution of an ADC, resulting in a single-channel 10-b 120- MSample/s performance [14], [15]. The prototype ADC based on the MCS technique enjoys the benefit of employing only eight unit-size capacitors for a 4-b MDAC instead of 16 capacitors normally required in the conventional MDAC architecture. The MDAC structure incorporating the proposed MCS technique can also lend itself to the commutated feedback-capacitor switching (CFCS) technique, which can increase the ADC resolution (DNL) even more [14], [16]. This paper is organized as follows. The ADC architecture with the proposed MCS technique is discussed in Section II. Section III deals with the CFCS technique based on the proposed MCS technique to achieve higher resolution. Circuit implementation is described in Section IV and the measured results of the prototype are summarized in Section V. Finally, the conclusions are given in Section VI.

II. ADC Architecture Based on Proposed MCS Technique

The block diagram of the proposed 10-b pipelined ADC is illustrated in Fig. 1. It is based on a conventional three-stage pipelined architecture. The ADC consists of an input

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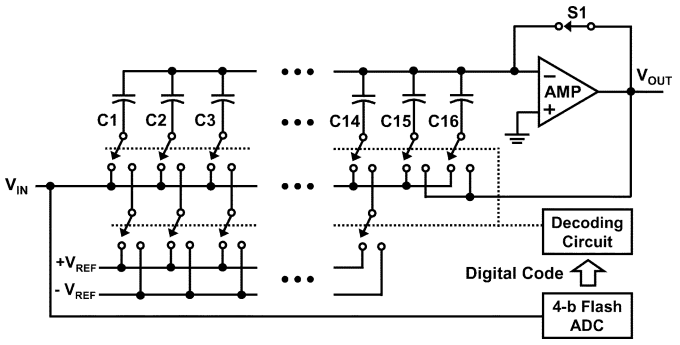

Fig. 2. Conventional 4-b MDAC.

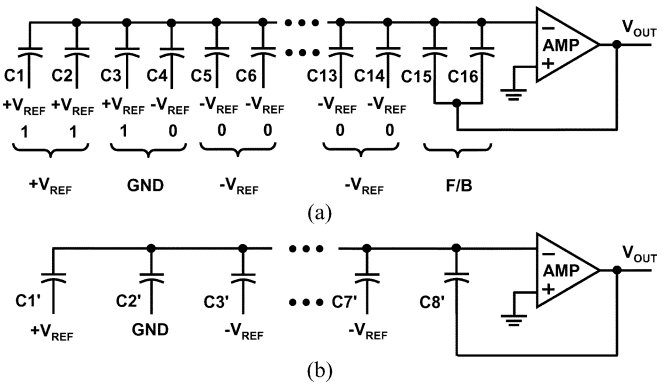

Fig. 3. MDAC during amplification based on (a) conventional and (b) proposed MCS techniques.

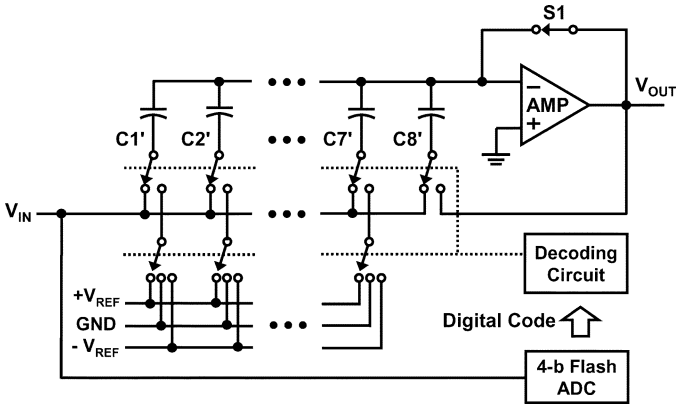

Fig. 4. The 4-b MDAC implementation based on the proposed MCS technique.

sample-and-hold amplifier (SHA), two 4-b MDACs, three 4-b subranging flash ADCs, and some extra supporting circuit blocks. Two nonoverlapping clock phases are internally generated for concurrent operations of all stages to convert analog input signals to digital output codes. Each of the three stages generates a 4-b digital code from the flash ADC, and the digital codes are processed in the digital correction/redundancy logic yielding a final 10-b word.

The proposed MCS technique, applied to capacitor arrays in the MDAC, merges two unit capacitors into one without affecting the performance of the remaining circuits of the ADC. This means the number of unit capacitors required in a conventional MDAC is reduced by 50%. For a given minimum-size unit capacitor, the operating speed of amplifiers can be increased with less power consumption since the total load capacitance is roughly reduced by a half. Alternately, the unit capacitor size may be doubled to obtain the better capacitor matching accuracy while speed and power consumption remain unchanged.

A conventional 4-b MDAC as shown in Fig. 2 has 16 unit capacitors, a residue amplifier, and a decoding circuit to control the switches connected to the capacitors. During the sampling phase, all the MDAC capacitor bottom plates are connected to the analog input voltage $V_{\rm IN}$, which is the output of the previous stage. During the following amplification phase, each bottom plate of capacitors $C1$ to $C14$ is connected to $+V_{\rm REF}$ or $-V_{\rm REF}$, depending on the digital code generated by the flash ADC. The two remaining capacitors $C15$ and $C16$ are connected to the amplifier output, $V_{\rm OUT}$, for proper residue amplification of $8\times$.

The MCS technique as illustrated in Fig. 3 reduces the required number of MDAC capacitors by a half, by merging eight pairs of capacitors, $C1\&C2, C3\&C4, \ldots, C15\&C16$, into eight new unit capacitors $C1'$to $C8'$. The function of the proposed MDAC employing the MCS is identical to that of the conventional MDAC. The only difference is that the signal ground (GND) is needed in the MCS technique, equivalent to when two different references ($+V_{\rm REF}$ and $-V_{\rm REF}$) are applied to two unit capacitors in the conventional MDAC. It is noted, for example, that $C3$ and $C4$ of Fig. 3(a) are directly mapped to the function of $C2'$ in Fig. 3(b).

The 4-b MDAC with the proposed MCS technique is implemented with eight unit capacitors connected to $+V_{\rm REF}$, GND, and $-V_{\rm REF}$, as shown in Fig. 4. The detailed connection of each capacitor bottom plate by the 4-b digital code from the flash ADC during MDAC residue amplification is summarized in Table I, where "0001" to "1111" in the left column are corresponding to the digital outputs from the 4-b flash subranging ADC and "F/B" indicates feedback connection. In a fully differential implementation, any fixed bias voltage can be employed so that the GND reference is not needed. The proposed fully differential 4-b MDAC is implemented as

TABLE I
MDAC CAPACITOR SWITCHING DURING AMPLIFICATION BASED ON THE PROPOSED MCS TECHNIQUE

	C1'	C2'	C3'	C4'	C5'	C6'	C7'	C8'
0001	-VREF	-VREF	-VREF	-VREF	-VREF	-VREF	-VREF	F/B
0010	GND	-VREF	-VREF	-VREF	-VREF	-VREF	-VREF	F/B
0011	+VREF	-VREF	-VREF	-VREF	-VREF	-VREF	-VREF	F/B
0100	+VREF	GND	-VREF	-VREF	-VREF	-VREF	-VREF	F/B
0101	+VREF	+VREF	-VREF	-VREF	-VREF	-VREF	-VREF	F/B
0110	+VREF	+VREF	GND	-VREF	-VREF	-VREF	-VREF	F/B
0111	+VREF	+VREF	+VREF	-VREF	-VREF	-VREF	-VREF	F/B
1000	+VREF	+VREF	+VREF	GND	-VREF	-VREF	-VREF	F/B
1001	+VREF	+VREF	+VREF	+VREF	-VREF	-VREF	-VREF	F/B
1010	+VREF	+VREF	+VREF	+VREF	GND	-VREF	-VREF	F/B
1011	+VREF	+VREF	+VREF	+VREF	+VREF	-VREF	-VREF	F/B
1100	+VREF	+VREF	+VREF	+VREF	+VREF	GND	-VREF	F/B
1101	+VREF	+VREF	+VREF	+VREF	+VREF	+VREF	-VREF	F/B
1110	+VREF	+VREF	+VREF	+VREF	+VREF	+VREF	GND	F/B
1111	+VREF	+VREF	+VREF	+VREF	+VREF	+VREF	+VREF	F/B

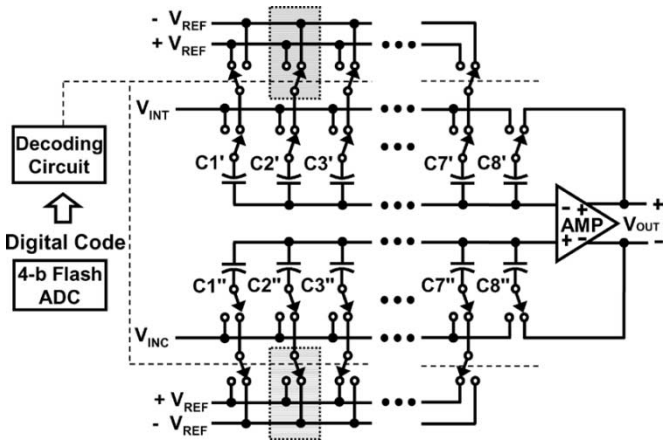

Fig. 5. Fully differential 4-b MDAC based on the proposed MCS technique.

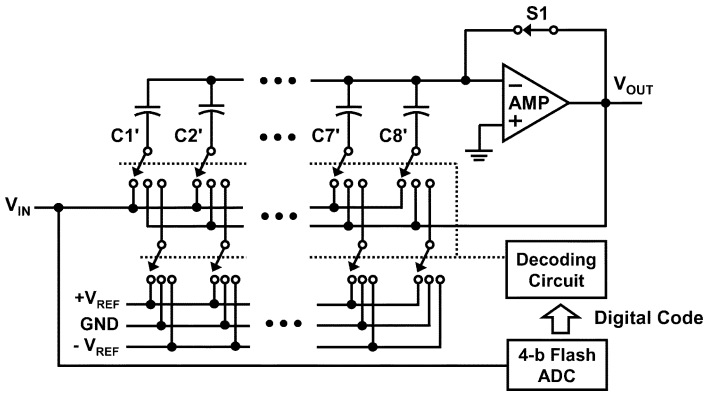

Fig. 6. Proposed 4-b MDAC implementation based on the MCS and CFCS techniques.

shown in Fig. 5. In this prototype integrated circuit (IC) implementation, $-V_{\rm REF}$ was employed for GND to simplify layout and to minimize floating nodes, instead of using a floating differential reset switch as in [17]. With this bias voltage, the input common-mode voltage of the MDAC amplifier changes approximately by 64 mV ($= 1/8$ of $-V_{\rm REF}$). Considering some amount of positive common-mode charge injection from the pMOS sampling switches turning off, the effect is negligibly small in this multibit MDAC.

III. Resolution Improvement Based on MCS Technique

A conventional CFCS technique that was developed for a 1- or 2-b per stage architecture with a single feedback capacitor in [16] can be extended to ADCs using the MCS technique. Since the conventional multibit MDAC architecture with digital error correction uses two unit capacitors as a feedback capacitor (Fig. 2), it is difficult to apply the CFCS technique directly. Although the CFCS technique can be applied to a modified MDAC architecture with digital error correction using one unit capacitor as the feedback capacitor, the resulting extension to the multibit MDAC becomes very complex due to extra dummy capacitors. However, the MCS structure using a single feedback capacitor can easily lend itself to the CFCS technique as follows.

The proposed 4-b MDAC based on both of the MCS and CFCS techniques is shown in Fig. 6. During the sampling phase, all the bottom plates of $C1'$ to $C8'$ are connected to the analog input voltage $V_{\rm IN}$. During the amplification phase, one of the eight capacitors $C1'$ to $C8'$ is used as a feedback capacitor depending on the digital code from the flash ADC and the remaining seven capacitors are connected to $\pm V_{\rm REF}$ or GND. Table II shows how to connect the eight MDAC capacitors depending on the 4-b digital code. All the capacitors are utilized as the feedback capacitor according to the digital code.

The corresponding residue plot of a typical 4-b MDAC is illustrated in Fig. 7. At the comparator decision boundary, the residue drop depends on the matching of the capacitors, which limits the DNL of the MDAC and the ADC. Capacitors with mismatches can be represented by

$$Ci' = C(1+\varepsilon_i) \qquad \text{for} \quad i = 1,2,\ldots,8 \tag{1}$$

TABLE II
MDAC Capacitor Switching During Amplification Based on Proposed MCS and CFCS Techniques

	C1'	C2'	C3'	C4'	C5'	C6'	C7'	C8'
0001	F/B	-$V_{\rm REF}$	-$V_{\rm REF}$	-$V_{\rm REF}$	-$V_{\rm REF}$	-$V_{\rm REF}$	-$V_{\rm REF}$	-$V_{\rm REF}$
0010	GND	F/B	-$V_{\rm REF}$	-$V_{\rm REF}$	-$V_{\rm REF}$	-$V_{\rm REF}$	-$V_{\rm REF}$	-$V_{\rm REF}$
0011	GND	GND	F/B	-$V_{\rm REF}$	-$V_{\rm REF}$	-$V_{\rm REF}$	-$V_{\rm REF}$	-$V_{\rm REF}$
0100	GND	GND	GND	F/B	-$V_{\rm REF}$	-$V_{\rm REF}$	-$V_{\rm REF}$	-$V_{\rm REF}$
0101	GND	GND	GND	GND	F/B	-$V_{\rm REF}$	-$V_{\rm REF}$	-$V_{\rm REF}$
0110	GND	GND	GND	GND	GND	F/B	-$V_{\rm REF}$	-$V_{\rm REF}$
0111	GND	GND	GND	GND	GND	GND	F/B	-$V_{\rm REF}$
1000	GND	GND	GND	GND	GND	GND	GND	F/B
1001	F/B	GND	GND	GND	GND	GND	GND	+$V_{\rm REF}$
1010	+$V_{\rm REF}$	F/B	GND	GND	GND	GND	GND	+$V_{\rm REF}$
1011	+$V_{\rm REF}$	+$V_{\rm REF}$	F/B	GND	GND	GND	GND	+$V_{\rm REF}$
1100	+$V_{\rm REF}$	+$V_{\rm REF}$	+$V_{\rm REF}$	F/B	GND	GND	GND	+$V_{\rm REF}$
1101	+$V_{\rm REF}$	+$V_{\rm REF}$	+$V_{\rm REF}$	+$V_{\rm REF}$	F/B	GND	GND	+$V_{\rm REF}$
1110	+$V_{\rm REF}$	+$V_{\rm REF}$	+$V_{\rm REF}$	+$V_{\rm REF}$	+$V_{\rm REF}$	F/B	GND	+$V_{\rm REF}$
1111	+$V_{\rm REF}$	+$V_{\rm REF}$	+$V_{\rm REF}$	+$V_{\rm REF}$	+$V_{\rm REF}$	+$V_{\rm REF}$	F/B	+$V_{\rm REF}$

where $C = \frac{1}{8}(C1'+C2'+C3'+C4'+C5'+C6'+C7'+C8')$. Each error term ε_i represents the mismatch of the capacitor Ci'.

In the proposed MDAC employing only the MCS technique, for example, the residue drop at the transition point from "0001" to "0010" can be calculated as follows (refer to Fig. 7 and Table I) :

$$V_1 \approx \left(\frac{1}{2}-\frac{3}{2}\varepsilon_8\right)\cdot V_{\rm REF}, \quad V_2 \approx -\left(\frac{1}{2}+\varepsilon_1+\frac{1}{2}\varepsilon_8\right)\cdot V_{\rm REF} \tag{2}$$

$$V_{\rm drop} = V_1 - V_2 \approx \{1+(\varepsilon_1-\varepsilon_8)\}\cdot V_{\rm REF}. \tag{3}$$

Voltages V_1, V_2, and $V_{\rm drop}$, are labeled in Fig. 7. If the MDAC capacitors have no mismatch, V_1 and V_2 are $V_{\rm REF}/2$ and $-V_{\rm REF}/2$, respectively, generating the residue voltage drop of $V_{\rm REF}$. Due to mismatches, the induced error $(\varepsilon_1-\varepsilon_8)\cdot V_{\rm REF}$ results as the DNL at this transition. This result is similar to the conventional MDAC without the MCS technique. Expressions similar to (3) can be derived for all other transition points.

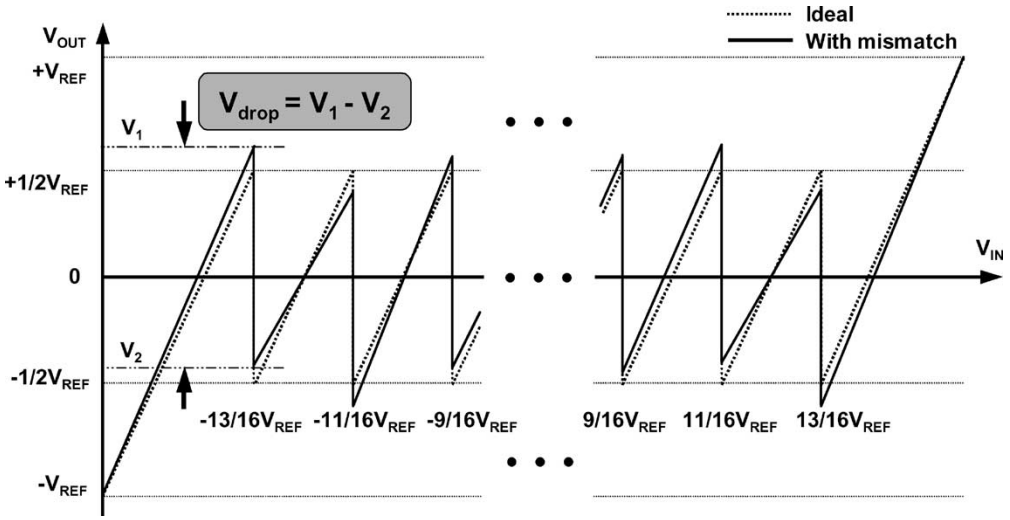

Fig. 7. Residue plot of a 4-b MDAC based on the combined MCS and CFCS techniques.

For an MDAC structure employing the MCS and CFCS techniques together, the residue drop with the same transition point from "0001" to "0010" can be calculated as follows (refer to Fig. 7 and Table II) :

$$V_1 \approx \left(\frac{1}{2}-\frac{3}{2}\varepsilon_1\right)\cdot V_{\mathrm{REF}},\ V_2 \approx -\left(\frac{1}{2}+\varepsilon_1+\frac{1}{2}\varepsilon_2\right)\cdot V_{\mathrm{REF}} \tag{4}$$

$$V_{\mathrm{drop}} = V_1 - V_2 \approx \left\{1+\frac{(\varepsilon_2-\varepsilon_1)}{2}\right\}\cdot V_{\mathrm{REF}}. \tag{5}$$

From (3) and (5), it is observed that the induced error at the same transition point is roughly reduced by a half, when the MCS and CFCS techniques are combined. The residue drops obtained at all other transition points also show similar trends. The reduced transition error at each residue drop (proportional to DNL) improves the ADC linearity. If desired, this can be further enhanced by increasing the unit capacitor size in the MDAC as much as the number of capacitors reduced by the MCS technique.

In this paper, only the MCS technique is implemented in the prototype IC to obtain a high-speed operation of 120 MHz at 10-b accuracy as described in Sections IV and V. The CFCS technique combined with the MCS technique for higher resolution is verified only by simulation as follows. One hundred ADC samples are simulated to verify the resolution and yield improvement. The DNL distributions of the simulated ADC samples are shown in Fig. 8. The ADCs have a 4-stage pipelined architecture (4-4-4-5) to obtain 14-b outputs. The unit capacitor mismatch of the conventional MDAC for simulation is set to 0.1% for a 12-b-level resolution, which is extracted from the measured prototype ADC [14]. The unit capacitor mismatch of the MDAC using both of the MCS and CFCS techniques is set to $0.1/\sqrt{2}\%$ assuming that the MCS MDAC capacitors employ the increased capacitor size by a factor of two to obtain the same loading condition as the conventional MDAC. About 70% of the conventional ADCs are at a 12-b level and about 80% of the proposed ADCs using the MCS and CFCS techniques are at a 13-b level. If the proposed design techniques and the layout techniques to improve capacitor matching are combined together, the resolution (DNL) of the prototype ADC can be extended significantly.

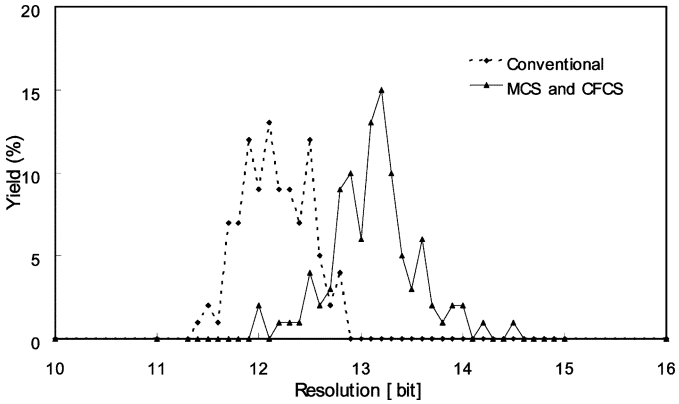

Fig. 8. DNL distributions of simulated ADC samples.

IV. 10-b 120-MSample/s ADC Implementation

A fully differential architecture is employed in all analog blocks to improve the converter performance. The ADC is optimized to operate with a maximum 2-$V_{\mathrm{p-p}}$ input signal swing with a 2.5-V supply voltage. The input SHA consists of CMOS switches, two input sampling capacitors, and a folded cascode amplifier with a loop gain bandwidth of 320 MHz. The ADC is optimized to handle both single-ended and differential input signals with a wide bandwidth for high dynamic performance up to 120-MHz sampling rate. The conventional two-sampling-capacitor architecture employed in the SHA is realized with small die area and low power consumption. Taking into consideration the thermal (kT/C) noise for 10-b accuracy, the sampling capacitance used in the SHA is 1.2 pF.

Each MDAC consists of opamp, capacitor arrays, and related switches. A two-stage Miller-compensated amplifier with a simulated dc gain of 100 dB is used in the MDAC and the proposed MCS technique is employed in the capacitor array. The unit capacitor size of the first- and second-stage MDAC is 0.2 pF and 0.1 pF, respectively, considering the adequate capacitor matching and thermal (kT/C) noise for the required res-

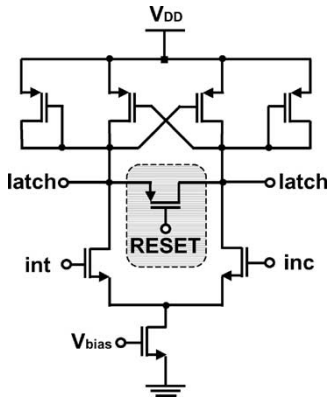

Fig. 9. Comparator preamp with reset switch.

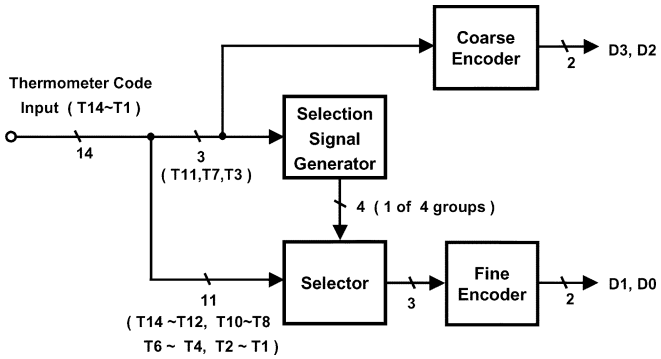

Fig. 10. Block diagram of the proposed encoding.

olution in each stage. The two-stage opamp of the first-stage MDAC has a loop gain bandwidth of 240 MHz with a phase margin of 63° for an approximate feedback factor of 2^{-3} to obtain a 7-b accurate settling time in less than 4 ns at the output.

The preamps in the flash subranging ADCs employ a small pMOS reset switch at the outputs as shown in Fig. 9 for low power consumption and high-speed operation. The proposed encoder in the flash ADCs employs a logic-based two-step encoding scheme to reduce chip area and power consumption instead of a conventional ROM-based encoding [15]. Fig. 10 shows the block diagram of the proposed encoding scheme and Table III illustrates the encoding from a thermometer code into a binary code implemented in the flash ADCs with redundant codes required for digital error correction. The proposed encoding circuit is partitioned into the coarse and fine encoders. Three bits of T11, T7, and T3 are used as inputs of the coarse encoder to select one group as inputs of the fine encoder between four groups of bits (T2-T1, T6-T5-T4, T10-T9-T8, and T14-T13-T12). Three bits of T11, T7, and T3 and the selected group of bits is passed to the coarse and fine encoders, which generate the two most significant bits and the two least significant bits, respectively. The number of MOS transistors and the power consumption required in the ROM-based encoder are reduced by a half compared with those of the logic-based encoder.

V. Prototype Measurements

The proposed ADC was fabricated in a 0.25-μm double-poly five-metal CMOS process. The prototype, shown in Fig. 11, occupies 3.6-mm^2 ($= 1.8 \times 2.0$ mm^2) active die area, and dissipates 208 mW when operated with a 120-MHz clock and a 2.5-V supply. In the IC measurements setup, external low-pass and/or band-pass filters at the inputs suppress the harmonics and noise from the test signal generator and a transformer provides a clean single to differential input signal conversion. External buffers connected to the ADC digital output drive high-speed measurement equipment directly at the full conversion speed. As shown in Fig. 12, the measured differential and integral nonlinearities show less than ± 0.40 LSB and ± 0.48 LSB at a 10-b accuracy. Fig. 13(a) and (b) shows the measured signal spectrum. The measured signal-to-noise-and-distortion ratio (SNDR) with a 10-MHz input sine wave at 100 MSample/s is 58 dB, and it drops by 6 dB at 120 MSample/s due to the increased noise

TABLE III
Encoding From Thermometer Code to Binary Code

THERMOMETER CODE													BINARY CODE			
T14	T13	T12	T11	T10	T9	T8	T7	T6	T5	T4	T3	T2	T1	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0
0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	1
0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1	0	0
0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1	0	1
0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	1	1	0
0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	1	1
0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0
0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	1
0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	1	0
0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	0	1	1
0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0
0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1
0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

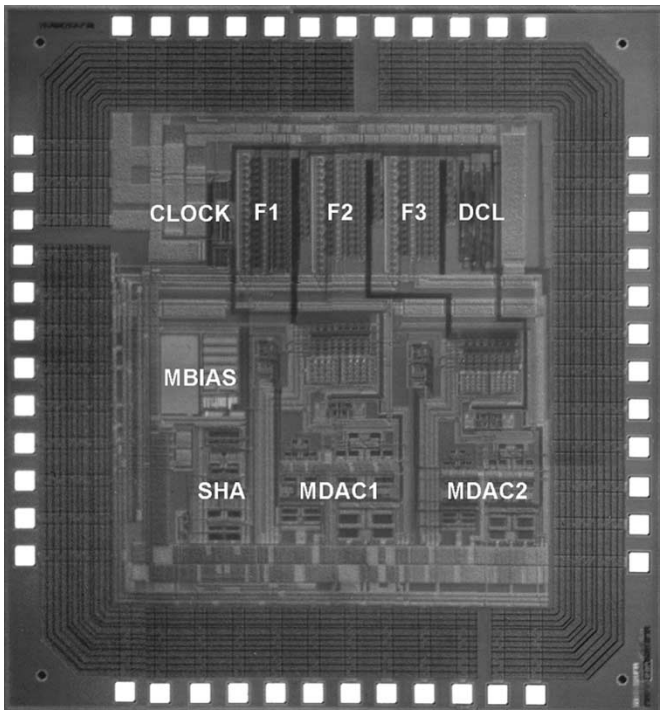

Fig. 11. Die photograph of the prototype ADC.

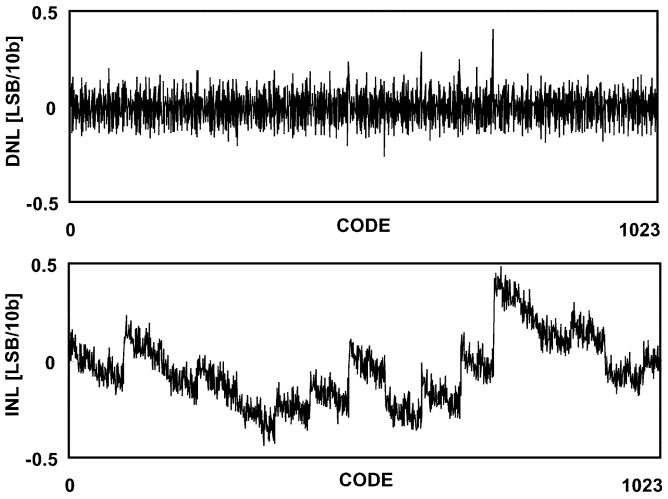

Fig. 12. Measured DNL and INL.

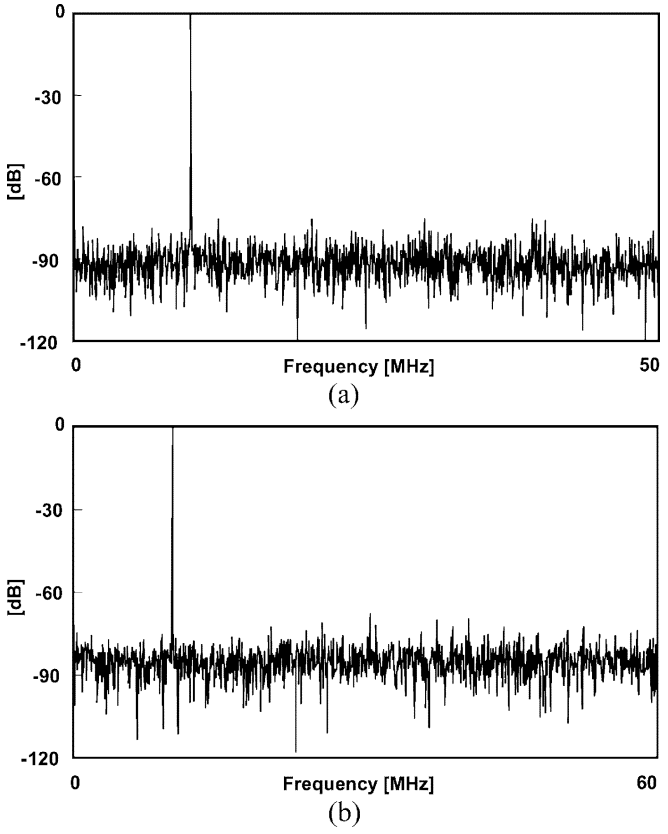

Fig. 13. Measured signal spectrum ($\mathrm{fin} = 10$ MHz) (a) at 100 MSample/s and (b) at 120 MSample/s.

floor level. However, the ADC achieves the spurious-free dynamic range (SFDR) of 68 dB at 120 MSample/s.Fig. 14(a) and (b) shows the dynamic performance of the prototype ADC. At the increased sampling rate of 120 MHz and the input frequency of 3 MHz, the measured SNDR demonstrates 53 dB. The multibit-per-stage architecture incorporating the MCS technique maintains the SNDR over 54 dB and the SFDR over 68 dB for signal frequencies up to Nyquist at a 100-MHz sampling rate. The measured results are summarized in Table IV.

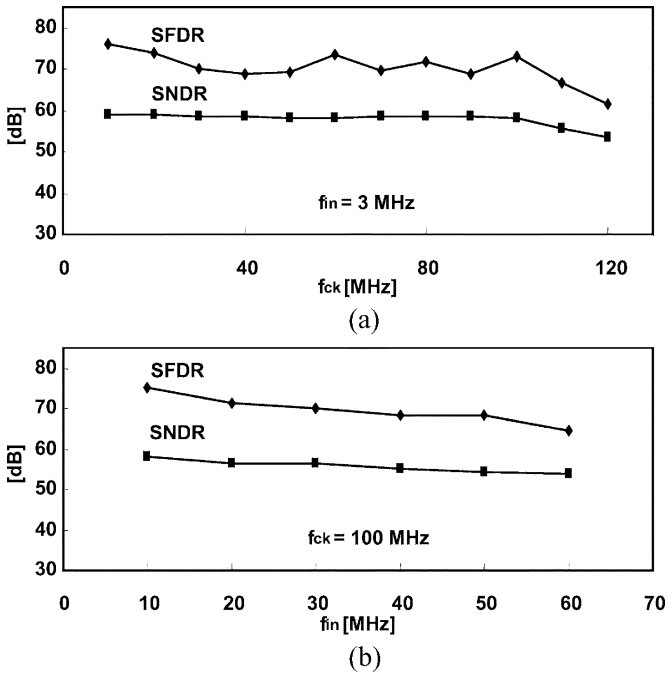

Fig. 14. Measured dynamic performance. (a) SFDR and SNDR versus sampling frequency and (b) SFDR and SNDR versus input frequency.

TABLE IV
PERFORMANCE SUMMARY

Resolution	10 bits
Max. Conversion Rate	120 MSample/s
Process	0.25-um double-poly CMOS
Input Range	2 V_{P-P}
SNDR (at 100 MS/s)	58.2 dB at f_{in} of 10 MHz 54.1 dB at f_{in} of 50 MHz
SFDR (at 100 MS/s)	75.3 dB at f_{in} of 10 MHz 68.4 dB at f_{in} of 50 MHz
DNL	±0.40 LSB
INL	±0.48 LSB
ADC Power	208 mW
Die Area	3.6 mm^2 (=1.8 × 2.0 mm^2)

VI. CONCLUSION

This paper describes circuit design techniques applicable to high-speed and high-resolution ADC systems. As a design example, a 10-b 120-MSample/s single-channel pipelined CMOS ADC has been demonstrated. The proposed MCS technique in a multibit-per-stage pipelined architecture achieves high conversion speed and high SFDR. It is verified in simulation that the ADC resolution can be improved further by employing the CFCS technique. Another important advantage of this MCS technique is that the amount of metal lines/routing, switches, and logic gates driving the affected capacitors is reduced by approximately 50%. This results in reduced load and parasitic capacitance, lower coupling noise, less power, and less chip area. The measurement results demonstrate the effectiveness of the MCS technique for speed and accuracy in the context of the multibit-per-stage pipelined ADC implementation.

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