A 2.5-V 45-Gb/s Decision Circuit Using SiGe BiCMOS Logic

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***Abstract*—A 45-Gb/s BiCMOS decision circuit operating from a 2.5-V supply is reported. The full-rate retiming flip-flop operates from the lowest supply voltage of any silicon-based flip-flop demonstrated to date at this speed. MOS and SiGe heterojunction-bipolar-transistor (HBT) current-mode logic families are compared. Capitalizing on the best features of both families, a true BiCMOS logic topology is presented that allows for operation from lower supply voltages than pure HBT implementations without compromising speed. The topology, based on a BiCMOS cascode, can also be applied to a number of millimeter-wave (mm-wave) circuits. In addition to the retiming flip-flop, the decision circuit includes a broadband transimpedance preamplifier to improve sensitivity, a tuned 45-GHz clock buffer, and a 50-Ω output driver. The first mm-wave transformer is employed along the clock path to perform single-ended-to-differential conversion. The entire circuit, which is implemented in a production 130-nm BiCMOS process with 150-GHz f_T SiGe HBT, consumes 288 mW from a 2.5-V supply, including only 58 mW from the flip-flop.**

***Index Terms*—BiCMOS, current-mode logic, flip-flops, low-noise, millimeter-wave (mm-wave), SiGe HBT, transformer, transimpedance amplifier.**

I. Introduction

SILICON germanium (SiGe) heterojunction bipolar transistors (HBTs) have become attractive for high-speed and millimeter-wave (mm-wave) applications. The high cutoff frequency of advanced SiGe HBTs, comparable to that found in III-V devices, has led to a number of record-breaking building blocks being reported in pure bipolar technologies [1], [2]. Furthermore, SiGe HBTs can be readily integrated with deep-submicrometer CMOS in a BiCMOS technology, paving the way for highly integrated broadband transceivers. However, power dissipation remains a concern in these systems, particularly from the packaging perspective as heat removal considerations limit the achievable level of single-chip integration. To date, little attention has been paid toward methods for reducing power consumption in high-speed SiGe HBT designs.

The main obstacle in lowering power dissipation in these circuits remains the $V_{\rm BE}$ of the SiGe HBT, which is presently approaching 1 V when the device is biased at the peak-f_T current density. High-speed digital building blocks are usually comprised of cascades of emitter followers and bipolar differential pairs. These topologies limit the available voltage headroom and result in supply voltages of 3.3 V for emitter-coupled logic (ECL) [2] and 5 V or higher in E^2CL [1]. Supply voltages encountered in MOS current-mode logic (CML) circuits are typically 1.5 V or lower for designs implemented in 130-nm technologies. When biased at peak f_T, standard and low threshold 130-nm nMOSFETs require gate-to-source voltages around 800 and 650 mV, respectively. Hence, replacing HBTs with MOSFETs is a logical option for reducing the supply voltage. As seen in Fig. 1, the f_T and $f_{\rm MAX}$ of a 130-nm nMOSFET are higher than those of 150-GHz SiGe HBTs for $V_{\rm DS}/V_{\rm CE}$ below around 600 mV. This marks a reversal of trends from the 0.5-μm technology node [3] and further supports the use of MOSFETs in low-voltage high-speed applications. Still, even in 90-nm technologies where reported f_T and $f_{\rm MAX}$ values rival those obtained in SiGe HBTs [4], performance in benchmark high-speed digital circuits such as multiplexers [5] lags that of SiGe implementations [2]. It must be demonstrated that MOSFETs can replace HBTs without sacrificing speed.

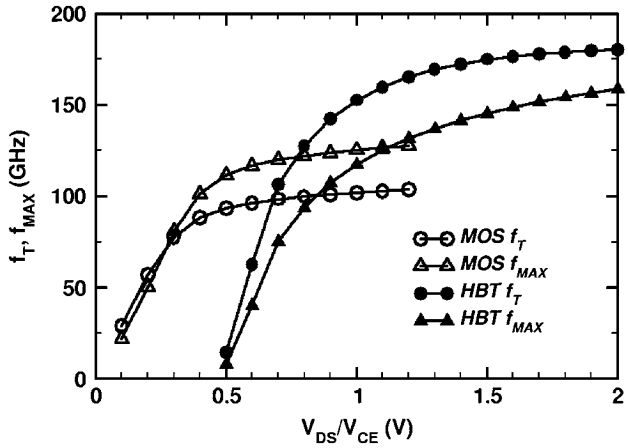

Fig. 1. Simulated f_T and $f_{\rm MAX}$ of a 150-GHz SiGe HBT and 130-nm nMOS as a function of $V_{\rm CE}/V_{\rm DS}$. Both devices are sized such that their peak f_T is obtained at collector/drain currents of 6 mA. Below $\sim$600 mV, the nMOS outperforms the SiGe HBT.

This paper reports on an effective combination of HBTs and MOSFETs in a high-speed logic family that allows for operation from lower supply voltages than pure bipolar topologies while maintaining the speed of SiGe HBT ECL. Section II examines the advantages and limitations of both MOS CML and HBT ECL families. MOS CML design is discussed, along with techniques for improving speed by minimizing voltage

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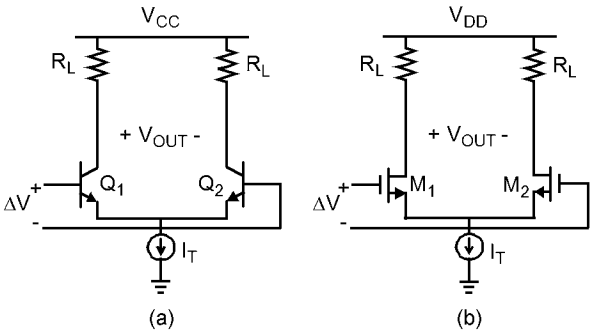

Fig. 2. Basic CML inverter implemented with (a) SiGe HBTs and (b) nMOSFETs.

swing. Cascode nMOS, bipolar, and BiCMOS topologies for high-speed digital as well as mm-wave applications are investigated in Section III which leads to an introduction of a true BiCMOS high-speed logic family. This topology, which places n-channel MOSFETs on high-speed signal and clock paths, takes full advantage of the best features of the MOSFET and of the SiGe HBT to produce a hybrid topology that is faster than its individual components. Section IV presents the design of a 45-Gb/s BiCMOS decision circuit. The circuit consists of a BiCMOS full-rate retiming flip-flop, a high-sensitivity transimpedance preamplifier, a tuned clock buffer with an integrated mm-wave transformer, and a broadband 50-Ω output driver. Experimental results for the decision circuit, implemented in a 130-nm SiGe BiCMOS technology [6], are reported in Section V.

II. Comparison of HBT and MOS Current-Mode Logic

While the f_T and $f_{\rm MAX}$ provide useful figures of merit for device performance, these metrics are not representative of the speed of digital circuits implemented in a given technology. Instead, it is well known that the attainable data rate in HBT or MOS broadband circuits is limited by the *RC* time constants of the circuit [7]. Thus, optimizing the performance of high-speed digital blocks becomes an exercise in minimizing these time constants.

The basic inverter (INV), shown in Fig. 2 for both HBT and MOS CML, serves as a useful reference for comparing high-speed digital circuit performance. Summing the open-circuit time constants for a chain of HBT or MOS CML INVs with a stage-to-stage size scaling factor of k provides a useful metric for comparing the digital speed of each technology [8].

$$\tau_{\rm HBT} \approx \Delta V \frac{C_{\rm BC}+C_{\rm CS}+C_{\rm INT}}{I_T} + \left(k+\frac{R_B}{R_L}\right)\Delta V \frac{C_\pi+(1-A_V)C_{\rm BC}}{I_T} \quad (1)$$

$$\tau_{\rm MOS} \approx \Delta V \frac{C_{\rm GD}+C_{\rm DB}+C_{\rm INT}}{I_T} + \left(k+\frac{R_G}{R_L}\right)\Delta V \frac{C_{\rm GS}+(1-A_V)C_{\rm GD}}{I_T}. \quad (2)$$

Here, ΔV is the (single-ended) voltage swing given by the product of the tail current I_T and the load resistance R_L. R_B and R_G represent the base resistance and gate resistance of the SiGe HBT and nMOSFET, respectively, while A_V is the low-frequency, small-signal voltage gain of the inverter. In both expressions, the first term describes the time constant at the output of the inverter and is approximately equal to the voltage swing divided by the intrinsic slew rate of the device. Since the collector-to-substrate capacitance $(C_{\rm CS})$ is smaller than the corresponding drain-to-bulk capacitance $(C_{\rm DB})$ of the MOSFET [9], the output time constant is lower in the SiGe HBT CML inverter for identical tail currents. Parasitic interconnect capacitance $(C_{\rm INT})$ loads the output and hence also degrades this time constant in both MOS and HBT circuits. The second terms in (1) and (2) account for the input time constant and are dominated in the low k limit by the R_BC_{BC} and $R_GC_{\rm GD}$ components, respectively, with $C_{\rm BC}$ and $C_{\rm GD}$ describing the base–collector and gate–drain capacitances. The small-signal voltage gain A_V exacerbates this time constant due to Miller multiplication, especially in HBT INVs. However, this problem is alleviated when employing cascode inverter topologies, as is often the case in clocked CML circuits. In SiGe HBTs, the intrinsic and extrinsic components of the base resistance can be reduced by increasing the emitter length or by using multiple emitter stripes, both of which increase base-to-collector capacitance. Hence, the $R_BC_{\rm BC}$ time constant is approximately constant for a given bipolar technology node. Reducing it has recently been identified as a critical challenge in high-speed SiGe HBT design [10]. For n-channel MOSFETs, the gate resistance of a multifinger device contacted on one side of the gate is determined from the polysilicon sheet resistance $(\rho_{\rm POLY})$, number of gate fingers (N_F), finger width (W_F), gate length (L), polysilicon-to-metal1 contact resistance $(R_{\rm CONT})$, and the number of contacts per gate finger $(N_{\rm CONT})$ as

$$R_G = \frac{1}{3}\frac{\rho_{\rm POLY}W_F}{N_F L} + \frac{R_{\rm CONT}}{N_{\rm CONT}N_F}. \quad (3)$$

For a given total gate width, the gate resistance can be reduced by increasing N_F. Since the gate periphery remains constant, the gate-to-drain capacitance is unchanged. Therefore, unlike the equivalent $R_BC_{\rm BC}$ time constant in SiGe HBTs, the $R_GC_{\rm GD}$ time constant of the n-channel MOSFET can be reduced through layout optimization.

Minimizing the voltage swing can further improve the delays given in (1) and (2). This voltage swing is determined by the minimum voltage required to fully switch the tail current in a differential pair. In bipolar CML, this minimum voltage is theoretically limited to about four times the thermal voltage V_T [11], but the voltage swing is typically chosen in the 200–300-mV range to ensure operation over all process and temperature corners [12] and to compensate for the voltage drop across the parasitic emitter resistance. Note that this choice of voltage swing also impacts A_V, setting it to between -4 and -6. In MOS CML designs, the required voltage swing is strongly dependent on the bias point. The effective gate voltage $(V_{\rm EFF}=V_{\rm GS}-V_T)$ value at which the peak f_T of the MOSFET occurs scales with technology, becoming smaller with every new generation. However, as the simulated data collected over three technology nodes in Fig. 3 indicates, the peak-f_T current density $(J_{\rm pfTMOS})$ remains approximately constant (between 0.3 and 0.4 mA/μm)

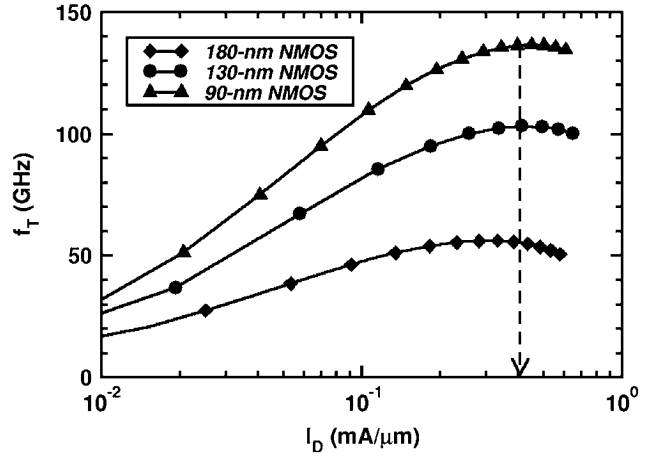

Fig. 3. Simulated f_T of nMOSFETs in 180-, 130-, and 90-nm technologies as a function of drain current density.

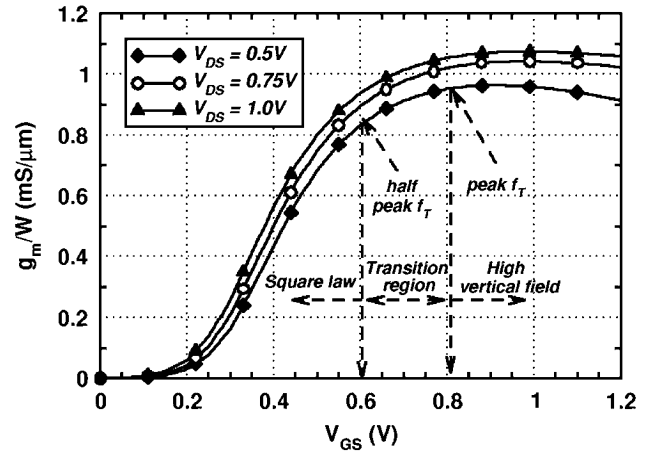

Fig. 4. Transconductance (g_m/μm) of a 130-nm nMOS for various $V_{\rm DS}$.

as the technology scales. This is true for all new MOS generations as a result of the constant field scaling that has been applied since the 0.5-μm technology node [3], [8]. Consequently, a current-density-centric design philosophy, similar to that which is commonly employed in bipolar designs [12], is more appropriate for foundry-independent design of MOS high-speed circuits than the $V_{\rm GS}$-centric design philosophy found in even the most recent textbooks (e.g., [11]). In a current-centric CML design scenario, the gate width W_G of the MOSFET is sized relative to the tail current (I_T) of the differential pair such that the device is biased at one-half of its peak f_T current density

$$W_G = \frac{I_T}{J_{\rm pfTMOS}}. \tag{4}$$

When the tail current is equally split between the transistors in the differential pair, this corresponds to a $V_{\rm EFF}$ of around 300 mV in a 130-nm technology. Biasing at a higher current density degrades the circuit performance, as will be explained below. Fig. 4 shows the transconductance g_m of a 130-nm nMOS as a function of gate voltage. Its shape is similar to that of the f_T dependence on $V_{\rm GS}$ and exhibits three regions, typical for all deep-submicrometer technologies. At low effective gate voltages, the device follows the classical square law model and the transconductance varies linearly with $V_{\rm GS}$ [8]. When biased in this region, the voltage swing required to completely switch the MOS differential pair is given by [11]

$$\Delta V > \sqrt{2} V_{\rm EFF}. \tag{5}$$

As the $V_{\rm EFF}$ at which peak f_T occurs is exceeded, the large vertical electric field leads to a significant degradation of mobility. As a result, g_m levels off and eventually decreases for large gate voltages. If the MOSFETs are biased in this region, the required voltage swing for full switching can be approximated by

$$\Delta V > 2 V_{\rm EFF}. \tag{6}$$

Thus, in the second bias region, both the scalar and $V_{\rm EFF}$ terms are larger, resulting in a greater input voltage to switch the differential pair. Consequently, for a given tail current, both terms in (2) increase and hence the bandwidth of the MOS INV is degraded when biased in this region. It should be pointed out that the bias point selected by (4) falls in a third bias region where the transition from the square-law region to the high vertical field regime occurs. The actual voltage swing required for complete switching in this region lies between the values predicted by (5) and (6). Nevertheless, these expressions, in conjunction with (2), highlight the need to minimize voltage swing in order to improve digital circuit speed.

It should be noted that, unlike that of HBT CML, the minimum MOS CML voltage swing given by (5) scales with the technology node. For example, in a 90-nm CMOS, the voltage swing should be approximately $\sqrt{2}$ less than that at the 130-nm technology node. While scaling will be advantageous for future MOS generations, overcoming the intrinsic slew rate limitation remains a challenge for MOS CML design. Still, with proper attention, MOS CML can be made to profit from its low input time constant. The contribution of the gate resistance can be diminished through layout techniques, and the Miller effect is reduced due to the low MOSFET gain. Note, however, that the gain must still be greater than unity to maintain regenerative properties within the logic family.

III. BiCMOS High-Speed Topologies

As mentioned earlier, supply voltages can be reduced by integrating MOSFETs into bipolar high-speed digital circuits. Noting that CML and ECL circuits such as multiplexers and latches consist of stacks of transistors similar to cascodes, it is beneficial to examine the frequency response of cascode amplifiers to determine the most efficient method for incorporating MOSFETs. The four cascode structures available in a BiCMOS technology are depicted in Fig. 5. The speed of cascode inverters implemented with each of these topologies can again be compared by examining the open-circuit time constants of a chain of such inverters

$$\begin{aligned}\tau_{\rm HBT-HBT} &\approx \Delta V \frac{C_{\rm BC}+C_{\rm CS}+C_{\rm INT}}{I_T} + \left(k+\frac{R_B}{R_L}\right)\Delta V \frac{C_\pi+2C_{\rm BC}}{I_T} \\ &\quad + \frac{C_\pi + C_{\rm CS}+C_{\rm BC}}{g_{m,\rm HBT}}\end{aligned} \tag{7}$$

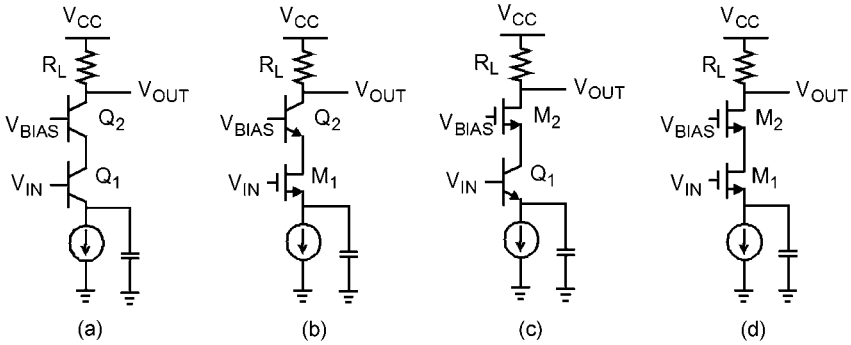

Fig. 5. Cascode topologies available in a BiCMOS technology. (a) HBT. (b) MOS-HBT (BiCMOS). (c) HBT-MOS. (d) MOS

$$\tau_{\mathrm{BiCMOS}} \approx \Delta V \frac{C_{\mathrm{BC}}+C_{\mathrm{CS}}+C_{\mathrm{INT}}}{I_T} + \left(k+\frac{R_G}{R_L}\right)\frac{\Delta V}{I_T}\left\{C_{\mathrm{GS}}+\left(1+\frac{g_{m,\mathrm{MOS}}}{g_{m,\mathrm{HBT}}}\right)C_{\mathrm{GD}}\right\} + \frac{C_\pi+C_{\mathrm{DB}}+C_{\mathrm{GD}}}{g_{m,\mathrm{HBT}}} \tag{8}$$

$$\tau_{\mathrm{HBT-MOS}} \approx \Delta V \frac{C_{\mathrm{GD}}+C_{\mathrm{DB}}+C_{\mathrm{INT}}}{I_T} + \left(k+\frac{R_B}{R_L}\right)\frac{\Delta V}{I_T}\left\{C_\pi+\left(1+\frac{g_{m,\mathrm{HBT}}}{g_{m,\mathrm{MOS}}}\right)C_{\mathrm{BC}}\right\} + \frac{C_{\mathrm{GS}}+C_{\mathrm{CS}}+C_{\mathrm{BC}}}{g_{m,\mathrm{MOS}}} \tag{9}$$

$$\tau_{\mathrm{MOS-MOS}} \approx \Delta V \frac{C_{\mathrm{GD}}+C_{\mathrm{DB}}+C_{\mathrm{INT}}}{I_T} + \left(k+\frac{R_B}{R_L}\right)\Delta V \frac{C_{\mathrm{GS}}+2C_{\mathrm{GD}}}{I_T} + \frac{C_{\mathrm{GS}}+C_{\mathrm{DB}}+C_{\mathrm{GD}}}{g_{m,\mathrm{MOS}}}. \tag{10}$$

As was the case for the HBT and MOS inverters analyzed earlier, the first two terms in (7)–(10) represent the output and input time constants, respectively. Similarly, the former is lower due to an HBT common-base output stage, while the latter can be reduced with a MOS common-source input stage. The third term accounts for the intermediate time constant at the collector (or drain) of the common-emitter (or common-source) input transistor and is inversely proportional to the f_T of the common-base (or common-gate) transistor. Fig. 6 illustrates the time constant contribution to the delay of each cascode amplifier as estimated from (7)–(10). Upon inspection, the BiCMOS cascode with MOS common-source and HBT common-base minimizes each of these terms and is expected to have the best frequency response.

To verify this assertion, the cascode structures were fabricated in a production 130-nm SiGe BiCMOS technology [6]. Each device was sized such that it reaches its peak f_T at a bias current of 6 mA. Gate finger widths of 2 μm were used for MOSFETs as a good compromise to lower the gate resistance without degrading f_T by increasing the contribution of the gate-to-well capacitance to the total gate capacitance. Small-signal S-parameters were measured up to 50 GHz for each amplifier, and the transducer gain S_{21} is plotted in Fig. 7. The measured 3-dB bandwidths of the HBT, HBT-MOS, and MOS cascodes are 25, 14.5, and 23.5 GHz, respectively, while that of the BiCMOS cascode exceeds the 50-GHz measurement capabilities. Despite operating from a lower supply voltage, the BiCMOS cascode outperforms even the HBT cascode and shows the benefits of combining the low gate resistance of the MOSFET with the small collector-to-substrate capacitance of the SiGe HBT. The latter is much lower than the corresponding drain-to-bulk capacitance of the nMOS, which is responsible for the lower 3-dB bandwidths of the two cascode topologies with MOS common-gate output transistors. Of additional concern with the HBT-MOS and MOS

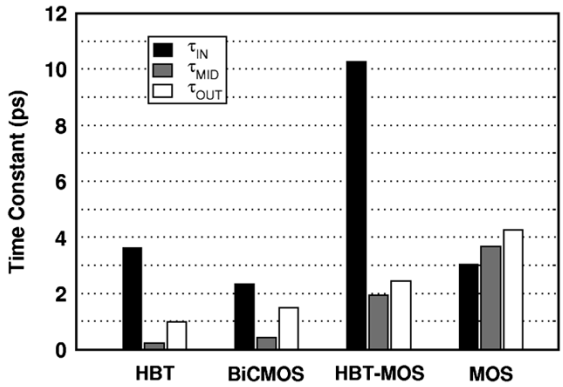

Fig. 6. Estimated time constants of the cascode amplifiers of Fig. 5 as predicted from (7)–(10) with a loading factor $k = 1$. τ_{IN} and τ_{OUT} represent the time constant at the input and output, respectively, while τ_{MID} accounts for the time constant at the collector (drain) of the common-emitter (-source) transistor.

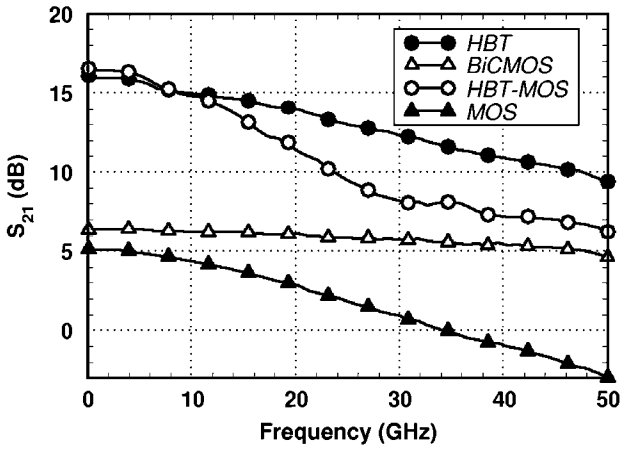

Fig. 7. Measured S_{21} for the four cascode amplifiers of Fig. 5.

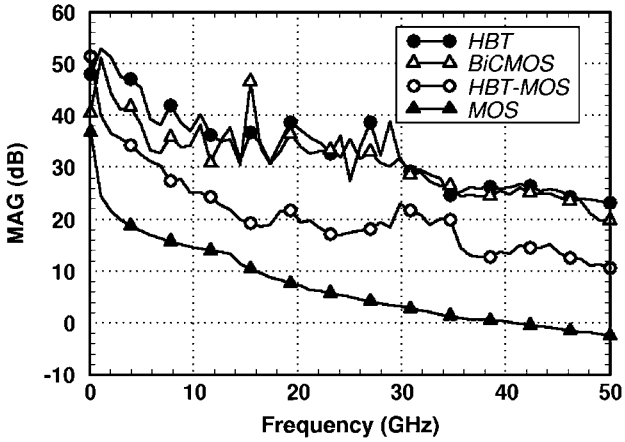

Fig. 8. MAG extracted from measured S-parameters for each of the cascode amplifiers.

cascode is the intermediate time constant at the source of the common-gate transistor, which is comparable to the input and output time constants and further degrades both the bandwidth and the stability of topologies with a MOS common gate. In fact, the detrimental impact of the intermediate time constant in the MOS cascode has led to the insertion of inductors at this node in certain MOS CML designs to mitigate its effects [13]. It is well known that the BiCMOS topology has excellent stability, prompting its use for lower frequency applications such as folded-cascode op amps [11].

It can be argued that the larger gain of the HBT cascode could be traded off to achieve better bandwidth than that of the BiCMOS cascode. However, to prove that this is not the case, as seen in Fig. 8, the measured maximum available gain (MAG) of the BiCMOS cascode, which is greater than 20 dB at 50 GHz, is comparable to that of the HBT. This makes the BiCMOS topology well suited for numerous high-speed and mm-wave applications, including low-noise amplifiers, voltage-controlled oscillators, broadband amplifiers, and high-speed digital logic. The latter will be explored in the following section.

IV. 45-Gb/s Decision Circuit Design

The role of the decision circuit is to retime data, potentially at low input levels, using a low-jitter full-rate clock, making it one of the most difficult blocks to design in a broadband serial receiver. A block diagram of the 45-Gb/s decision circuit is shown in Fig. 9. It consists of a BiCMOS D-flip-flop (DFF), a high-sensitivity transimpedance preamplifier, a tuned clock buffer with integrated transformer, and a broadband 50-Ω output driver. The design of each of these blocks will be discussed in this section.

A. BiCMOS D-Flip-Flop

The BiCMOS topology discussed in Section III in the context of CML inverters can readily be applied to more complex digital circuits such as latches or selectors. The BiCMOS implementation of a D-latch is illustrated in Fig. 10. It is emphasized that the highest frequency signal, the full-rate clock, is applied to the input of the device with lower f_T, the nMOS differential pair. A smaller time constant at this node is more important in maximizing the switching speed than the f_T of the transistor. SiGe

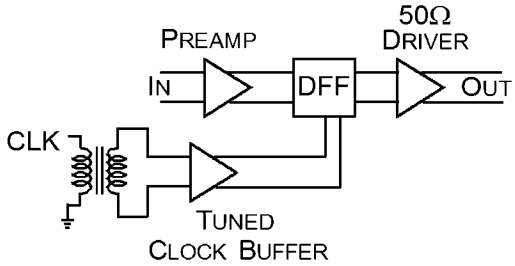

Fig. 9. Block diagram of a 45-Gb/s decision circuit.

HBTs are used for the upper level data inputs, as their high slew rate results in fast rise and fall times. MOS source-follower (SF) stages are employed instead of HBT emitter followers (EFs) to allow for operation from a 2.5-V supply. This is particularly important in the feedback path since the $V_{\rm BE}$ or $V_{\rm GS}$ of the follower limits the voltage headroom. Low-threshold nMOSFETs would further reduce the supply voltage to 1.8 V. With a 2.5-V supply, sufficient voltage headroom is available to use HBT EFs along the clock path to extend the frequency response beyond 50 GHz, but SFs would be required from a 1.8-V supply.

B. High-Sensitivity Transimpedance Preamplifier

Traditionally, INV, EF-INV, or EF-Cherry–Hooper topologies have been preferred for high-speed preamplifiers (e.g., [14]). All require on-chip 50-Ω matching resistors, which add noise and reduce the sensitivity of the preamplifier. While the use of EFs improves bandwidth, this form of series feedback at the input increases the already large optimal noise impedance of the transistors in the INV or Cherry–Hooper gain stages. Unless excessively large bias currents and transistor sizes are employed, a noise-impedance mismatch is produced when these preamplifiers are placed in a 50-Ω environment, which further degrades the sensitivity.

The transimpedance stage of Fig. 11 is instead employed as a preamplifier for the decision circuit. Amplifiers with transimpedance feedback have only recently been considered as low-noise voltage preamplifiers [15]. The use of shunt feedback lowers the optimal noise impedance, which improves sensitivity in a 50-Ω environment, with minimal current consumption. Appropriate choice of the loop gain A and feedback resistor resistor R_F results in a broadband impedance match given by

$$Z_o = R_{\rm in} = \frac{R_F}{1+A}. \tag{11}$$

A number of mm-wave inductors [16] are employed throughout the circuit to extend bandwidth without excessive power dissipation. The 40-fF pad capacitance $C_{\rm PAD}$ is absorbed in an artificial transmission line with input inductor L_B [17], while a feedback inductor L_F filters high-frequency noise from the feedback resistor [15]. L_C peaks the output node to ensure proper spacing of the open-loop poles for a maximally flat frequency response. The outputs are taken from the collectors of Q1 and Q2 to improve gain. A split-resistor load alleviates headroom concerns, with the ratio of R2 to R1 set to unity for maximum bandwidth [18]. A bipolar INV stage follows the transimpedance stage for additional gain.

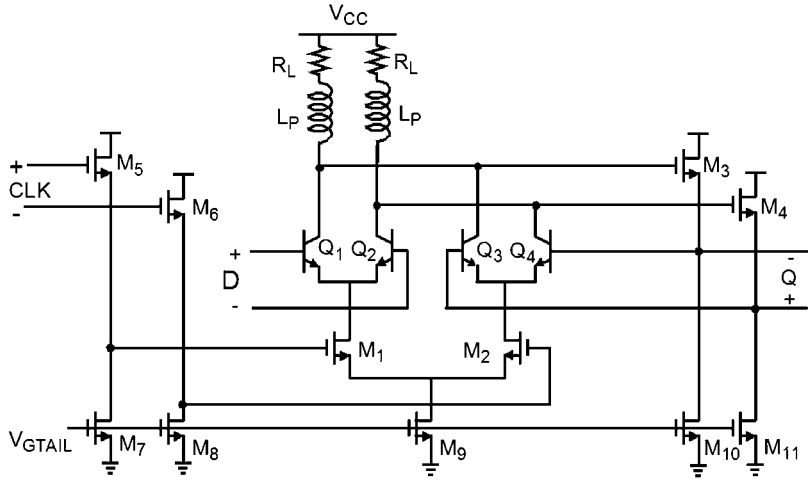

Fig. 10. BiCMOS implementation of a D-latch.

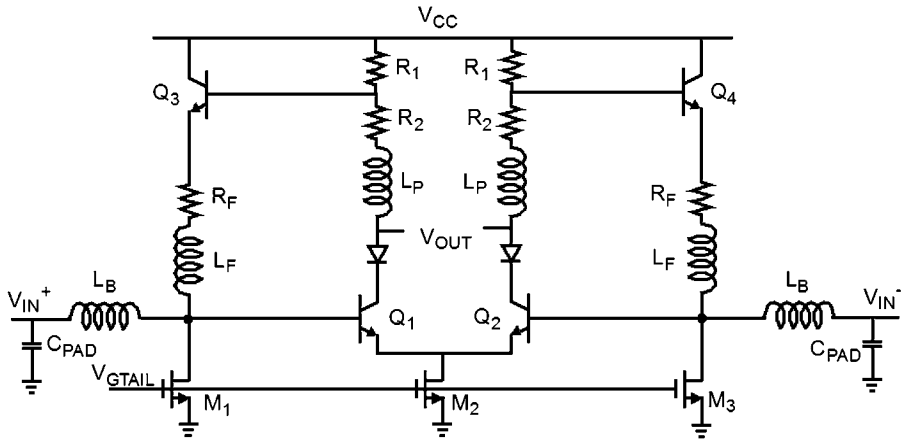

Fig. 11. High-sensitivity transimpedance preamplifier.

C. Clock Buffer With Integrated Transformer

The 45-GHz clock is the highest frequency signal in the decision circuit, making the design of a clock buffer challenging. Moreover, differential clock signals are required for high-speed logic, but only single-ended mm-wave signal sources are available for testing purposes. At lower frequencies, single-ended-to-differential conversion can be achieved via an active balun or a differential pair with the unused input terminated off-chip. However, at mm-wave frequencies, poor common-mode rejection renders this approach less effective, as the differential outputs exhibit amplitude mismatch and phase misalignment. Previous designs in the mm-wave regime have relied on expensive off-chip techniques [1] or on-chip components such as rat-race couplers at 80 GHz [19] to perform single-ended-to-differential conversion. Even at 80 GHz, a quarter-wavelength in silicon dioxide is about 470 μm, making the rat-race approach quite area-intensive. In this work, the first silicon-based mm-wave monolithic transformer is used to generate differential clock signals from a single-ended signal source. The transformer, whose die photo is shown in Fig. 12, consists of two coupled symmetric inductors and occupies an area of 45 μm $\times$ 45 μm, which is about 1/100th of the area of the 80-GHz rat-race coupler [19].

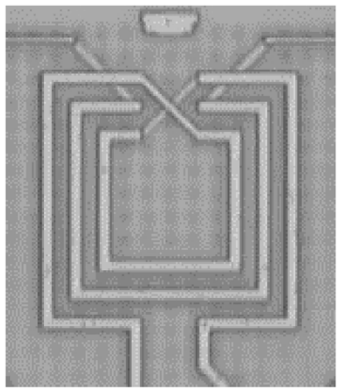

Fig. 12. Die photo of integrated mm-wave transformer. The outer diameter is 45 μm.

The schematic of the clock buffer is shown in Fig. 13. Two tuned stages are cascaded for additional gain to compensate for limited signal source power and losses in the cabling and transformer. The clock buffer makes use of the BiCMOS cascode introduced in Section III due to its excellent high-frequency performance. The series addition of small resistors intentionally degrades inductor quality factor and improves the bandwidth of the otherwise narrowband topology to allow for testing over a wide range of data rates.

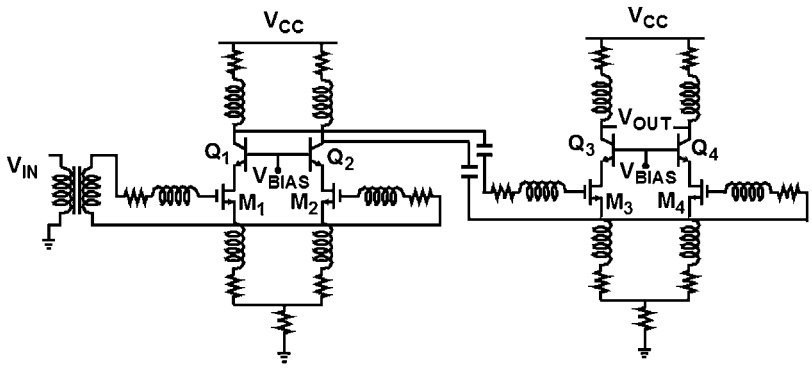

Fig. 13. Tuned clock buffer based on BiCMOS cascode (biasing details not shown).

D. 50-Ω Output Driver

A broadband output buffer was designed to drive external 50-Ω loads for testing purposes. The schematic, shown in Fig. 14, consists of inductively peaked bipolar INV and EF-INV stages. Load resistors in the final EF-INV stage are set to 50 Ω for impedance-matching purposes. When the external 50-Ω load is also considered, a significant 16 mA tail current in this final INV is required to generate a 400-mV swing per side. An additional bipolar INV is inserted between the retiming flip-flop and the output EF-INV stage to prevent overloading the flip-flop. Adjustable output swing is achieved by varying the tail current in the output driver. Emitter degeneration in the output INV stage not only increases bandwidth, but also lessens the impact of varying tail current on the input impedance of the INV. Output swings adjustable between 100–400 mV are achieved through this technique.

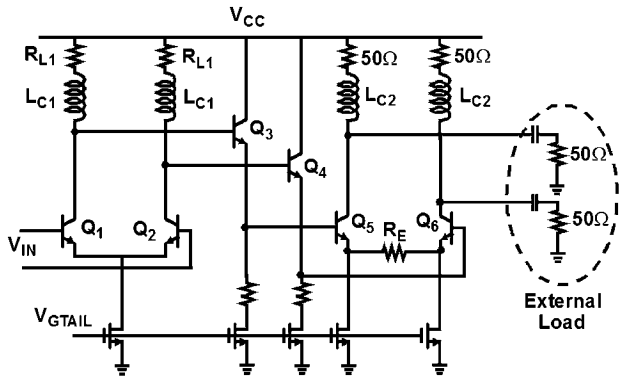

Fig. 14. Schematic of 50-Ω output driver.

V. Experimental Results

The 45-Gb/s decision circuit was implemented in the 0.13-μm SiGe BiCMOS process mentioned earlier. The chip microphotograph is shown in Fig. 15 and employs a total of 24 mm-wave inductors and one mm-wave transformer. To obtain adequate self-resonant frequency for mm-wave applications, it is critical to minimize the inductor footprint over the substrate [15]. As each passive device is at most 45 μm $\times$ 45 μm, it is feasible to integrate such a large number of them on a single die without consuming an exorbitant area. The total chip area is 1.0 mm $\times$ 0.8 mm.

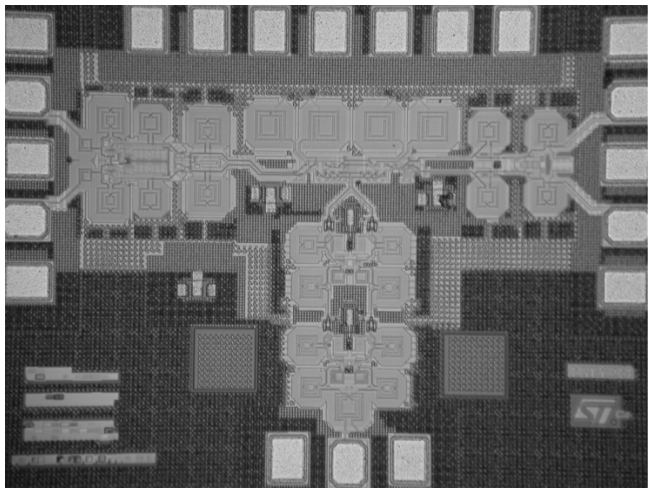

Fig. 15. Die photo of the 45-Gb/s decision circuit.

A separate test chip was also fabricated, consisting of the transimpedance preamplifier and broadband output driver. Fig. 16 shows the single-ended S-parameters of this differential test structure, which were measured on-wafer up to 50 GHz with the unused input and output terminated off-chip at 50 Ω. The 3-dB bandwidth is approximately 45 GHz, and the input and output return losses are both less than -10 dB over the entire measured frequency range. Since feedback is used to set the input impedance, it is observed that the single-ended and differential impedance matches are not identical. Note that, if a signal is applied only to the positive input of Fig. 11 and the negative input is terminated, only a portion of this signal is amplified and fed back to the positive input. The remainder is injected through the emitters of Q1 and Q2 into the other half-circuit of the differential amplifier. Nonetheless, despite this amplifier being designed for a differential 100-Ω impedance match, single-ended measurements still show a close match to the 50-Ω signal source.

Eye diagrams for the 45-Gb/s decision circuit were also measured on-wafer using 65-GHz GGB probes, 12-in 2.4-mm cables and an Agilent 86 100A DCA with the 86 118A 70-GHz dual remote sampling heads and external precision timebase. As the Anritsu MUX delivers a fixed 2-$V_{\rm PP}$ swing to a 50-Ω load, power attenuators were inserted between the output of the MUX and the input of the decision circuit to reduce the signal level to as low as 40 mV, and as high as 200 mV. This signal was

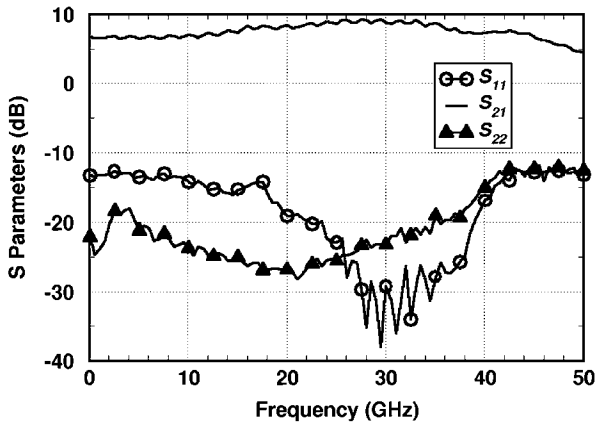

Fig. 16. Measured single-ended S-parameters of a transimpedance preamplifier and broadband output driver.

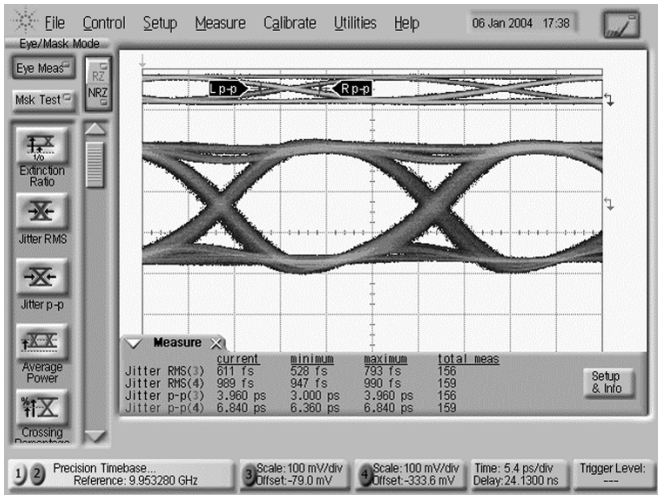

Fig. 17. Measured 40-Gb/s input (top, channel 4) and output (bottom, channel 3) eye diagrams for a 60-mV single-ended $2^{31}-1$ PRBS signal applied to one side of the differential input.

applied to one side of the differential circuit, with the unused input terminated off-chip in 50 Ω. As shown in Figs. 17–19, operation up to 45 Gb/s was verified by applying a $2^{31}-1$ PRBS pattern and 45-GHz clock from an Anritsu 43.5-Gb/s MP1801A MUX and pattern generator to the data and clock inputs, respectively. These measurements exceed the factory-specified range of the Anritsu MUX, which led to a slight increase in both input clock and data jitter when measured at 45 Gb/s. Fig. 17 presents 40-Gb/s input and output eye diagrams for a 60-mV single-ended (30 mV per side) input signal, indicating excellent sensitivity due to the low-noise input transimpedance stage. The high dynamic range of this input stage also allows for larger input amplitudes, as demonstrated in Fig. 18. Finally, a 45-Gb/s output eye is shown in Fig. 19. Although the high slew rate suggests operation could exceed 45 Gb/s, the bandwidth of the tuned clock buffer limits testing. In 48-Gb/s measurements, significant jitter was observed at the output and indicates that the clock no longer performs the retiming function. Circuit performance, including a breakdown of power consumption per block, is summarized in Table I.

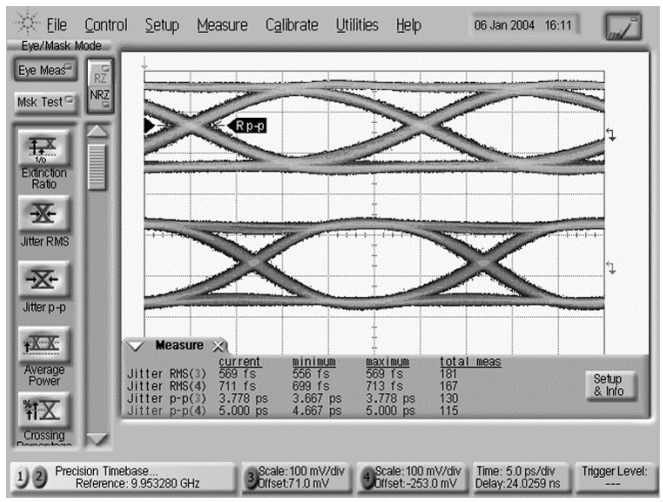

Fig. 18. Measured 40-Gb/s input (top, channel 4) and output (bottom, channel 3) eye diagrams for 200-mV single-ended input amplitude.

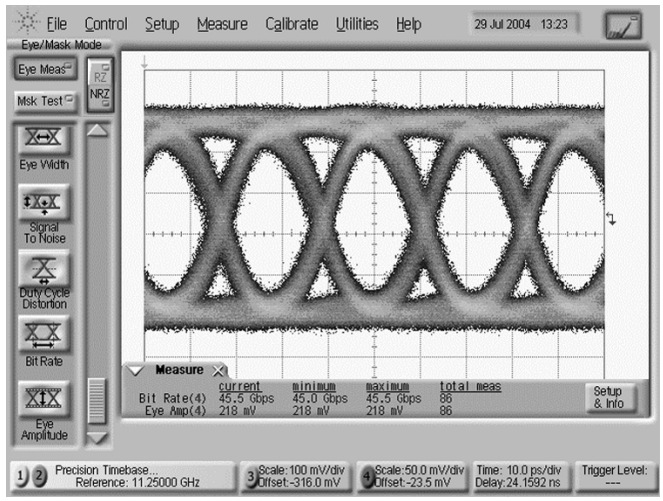

Fig. 19. Measured 45-Gb/s output eye diagrams.

TABLE I
PERFORMANCE SUMMARY OF 45-Gb/s DECISION CIRCUIT

Technology	SiGe BiCMOS (130-nm CMOS, 150-GHz SiGe HBT)
Supply Voltage	2.5 V nominal, 2.2 V minimum
Maximum Data Rate	45 Gb/s
Power Consumption	288mW
D-Flip-flop	58 mW
Preamplifier	70 mW
50-Ω Driver	68 mW
Clock Buffer	92 mW
Output jitter	580 ps (RMS)
Phase Margin	207° @ 40-GHz
Rise/fall times	7.5 ps
Output swing	100 mV – 400 mV per side (adjustable)
Input sensitivity	40 mV single-ended (20 mV per side)
Chip Size	1.0 x 0.8 mm^2

VI. CONCLUSION

A novel BiCMOS topology, based on a BiCMOS cascode, has been introduced which takes full advantage of the best features of both the n-channel MOSFET and SiGe HBT to

maximize high-speed performance. The large gain and bandwidth of the BiCMOS cascode make it well suited for mm-wave applications, such as the tuned 45-GHz clock buffer employed in this decision circuit. When applied to high-speed logic circuits, the topology allows for a reduction in supply voltages over pure SiGe HBT implementations without compromising speed. A 45-GHz retiming flip-flop which consumes 58 mW from a 2.5-V supply was implemented in a 0.13-μm SiGe BiCMOS process using this logic family. CML 60-Gb/s circuits with 30-GHz clocks have recently been reported in 90-nm CMOS [5], suggesting that 40-Gb/s full-rate retiming may not be feasible in CMOS until the 65-nm technology node. The full-rate 45-GHz clock in this work is applied to a 130-nm nMOS differential pair, making this DFF the fastest digital circuit using MOSFETs reported to date. Furthermore, previous demonstrations of full-rate retiming at 43 Gb/s in comparable SiGe technologies have operated from a supply voltage of at least -3.6 V [20]. These results indicate that the proposed BiCMOS logic topology is two generations ahead of pure CMOS while at the same time operating from lower supply voltages than ECL SiGe HBT implementations.

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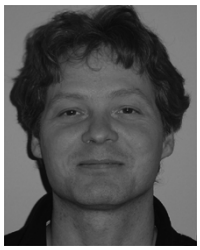

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