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A 2.53 NEF 8-bit 10 kS/s 0.5 µm CMOS Neural Recording Read-Out Circuit with High Linearity for Neuromodulation Implants

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Abstract: This paper presents a power-efficient complementary metal-oxide-semiconductor (CMOS) neural signal-recording read-out circuit for multichannel neuromodulation implants. The system includes a neural amplifier and a successive approximation register analog-to-digital converter (SAR-ADC) for recording and digitizing neural signal data to transmit to a remote receiver. The synthetic neural signal is generated using a LabVIEW myDAQ device and processed through a LabVIEW GUI. The read-out circuit is designed and fabricated in the standard 0.5 µm CMOS process. The proposed amplifier uses a fully differential two-stage topology with a reconfigurable capacitive-resistive feedback network. The amplifier achieves 49.26 dB and 60.53 dB gain within the frequency bandwidth of 0.57–301 Hz and 0.27–12.9 kHz to record the local field potentials (LFPs) and the action potentials (APs), respectively. The amplifier maintains a noise–power tradeoff by reducing the noise efficiency factor (NEF) to 2.53. The capacitors are manually laid out using the common-centroid placement technique, which increases the linearity of the ADC. The SAR-ADC achieves a signal-to-noise ratio (SNR) of 45.8 dB, with a resolution of 8 bits. The ADC exhibits an effective number of bits of 7.32 at a low sampling rate of 10 ksamples/s. The total power consumption of the chip is 26.02 µW, which makes it highly suitable for a multi-channel neural signal recording system.

Keywords: LabVIEW; neural amplifier; neuromodulation implants; noise–power tradeoff; read-out; SAR-ADC; two-stage OTA

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1. Introduction

Recent advancements in neuropotential recording pave the way for observing and understanding the various neurophysiological disorders [1–3]. Recording various neural activities also enables control of machines such as prosthetic limbs and other communication tools with the help of brain–machine interfaces (BMI) [4]. In addition to these, multi-channel recording with an estimation of neural biomarkers in a closed-loop neuromodulation system improves the treatment of Parkinson's disease by implementing deep brain stimulation (DBS) [5]. Developing a device with biomarker detection and controlling stimulation at a high spatial and temporal resolution, simultaneously recording from multiple sites, is imperative [6–8]. This necessitates the design of a low-power neural signal recording system with a very small footprint [9]. A customized application-specific integrated circuit (ASIC) would be a good choice for meeting these requirements.

Several implantable multi-channel wireless neural signal recording architectures are proposed in the literature [10–13]. One of the most common architectures is the one that has one shared analog-to-digital converter (ADC) among all the channels through an analog multiplexer (MUX). Alternatively, another architecture is proposed where each recording channel has an individual ADC for every amplifier [14], which obviously results in more power consumption. Finally, there is another architecture that has been proposed, which has m rows and n columns of channels [15]. Each column uses one ADC, and there are n number of ADCs implemented in the implant. This architecture is usually used for a large

number of recording channels. This paper utilizes the first architecture: one shared ADC for all the channels, which is shown in Figure 1. Using the analog MUX leads to a simpler architecture and lower power consumption compared to the other two techniques. As the prototype of an on-chip neural implant, a single-channel amplifier is implemented in this work. The implantable neural signal recording system includes neural amplifiers, an analog multiplexer, an ADC, a transmitter (TX), and an on-chip antenna for wireless transmission of the acquired data. The time-division multiplexing (TDM) technique could be used in designing the multiplexer for multiplexing the recording from the multiple sites in the analog domain [16,17]. Direct transmission of the multiplexed analog data has the advantage of a straightforward architecture and lower power dissipation [18]. As the number of channels increases, the sampling frequency of the multiplexer increases. An effective and precise acquisition system includes multi-channel recordings from a large number of neural probes, which are connected to the same number of amplifiers. The total power budget limits the high-density recording read-out circuit since the surrounding tissue of the probes could be damaged due to excessive power dissipation [19]. Another important consideration for designing the recording unit is the reduction of the chip area in order to minimize the surgical effects or neuronal damage, risk of infection, and risk of trauma, which could impact the behavioral study of the small subjects, such as mice or rats [20–23]. Moreover, a large number of recording sites may cause electromagnetic interference (EMI) and noise at the electrode–tissue interface, which degrades the performance of the system [24]. Thus, the analog read-out circuit design should target low-noise performance [25,26]. Hence, the objective of this simultaneous multi-channel neuropotential recording system is to meet the constraints of low power, low noise, and minimized chip area to perceive brain signal insights [16,27].

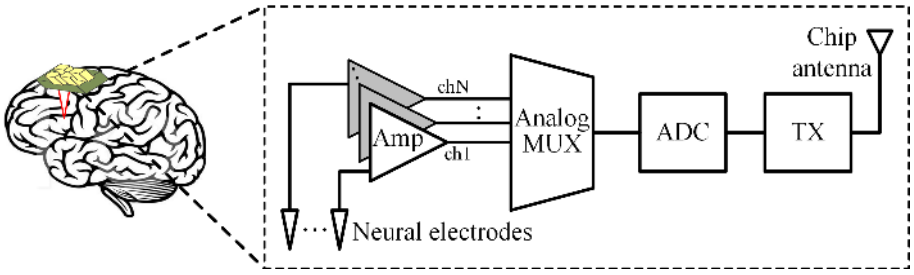

Figure 1. Overview of the neural signal recording system for brain neuromodulation implant.

The neuropotential signal of interest containing biomarkers for neuroscience research and other BMI applications are mostly the local field potentials (LFPs) and the action potentials (APs). They occupy different frequency bandwidths as well as maintain different amplitude levels. Typically, LFPs have peak amplitudes of about several mVs while occupying the frequency range of 0.1–250 Hz [28]. The peak amplitude of APs can be about a few μV within the 0.25–5 kHz of frequency bandwidth [29]. Since the neural signals can be as low as few μVs, the amplifier gain should be as high as ∼60 dB, with the low-frequency pole being as low as 500 mHz to detect them accurately [2,30]. Since a large number of recording sites would dissipate high power, the single-unit amplifier requires very high energy efficiency (noise efficiency factor (NEF) ∼1) [31,32]. This necessity for low-power consumption poses a tradeoff with noise performance, as the input-referred noise voltage is inversely correlated with the total power consumption [33]. Several architectures have been proposed in the literature considering these constraints [34–37]. The folded-cascode technique as the operational transconductance amplifier (OTA) along with the current-reuse or current-splitting technique is widely used for improving noise–power efficiency [38,39]. Current-reusing among the differential pair of transistors and the folded-cascode branches may affect current mirroring as well as supply voltage variation due to the large source degeneration. In order to improve the noise–power efficiency, this paper presents a two-stage amplifier architecture. The proposed closed-loop amplifier also

minimizes the large electrode-DC-offset (EDO) with a high power-supply rejection ratio (PSRR) to prevent saturation.

The neural signal recording read-out circuit includes an ADC to digitize both the APs and the LFPs faithfully. The ADC requires 7–8 effective number of bits (ENOB) at the minimum to reconstruct the acquired neural signal reliably as well as to maintain the signal integrity [1,29,40]. Several architectures are reported in prior work, such as the successive approximation register (SAR) [41], logarithmic pipeline [42], sigma-delta modulators [43,44], and dual-mode single-slope ADC [45], for biomedical system-on-chip (SoC) applications. Most of them suffer from oversampling data conversion compared to Nyquist-rate, large area, and high power consumption. Considering all these limitations, SAR is the most widely used ADC architecture due to its high energy efficiency and modest resolution data conversion at a low sampling rate [46]. Since the unit capacitance of the binary parallel capacitor array could be miniaturized without affecting the ENOB, the SAR architecture can achieve low-input capacitance [47]. The SAR-ADC featuring a simple architecture is suitable for a low-frequency neural signal recording system at a sampling rate of kHz order of magnitude. This paper presents a single-ended output 8-bit SAR-ADC considering the constraints and specifications for neural signal recording. For the sake of reducing the total power consumption of the whole recording unit, a low-sampling rate of 10 ksamples/s is used in this work. The single-ended configuration allows us to have a fixed reference voltage for the comparator as half of the supply voltage, thus reducing the complexity. The proposed capacitor array in the ADC is designed manually with poly layers since the process design kit does not have laid-out capacitors. The common-centroid routing technique is adopted in the charge-scaling digital-to-analog converter (DAC) of the ADC. Common-centroid placement alleviates the systematic mismatches as well as the parasitic capacitance, which is induced in the layout [48,49]. Poly layers are used instead of metal layers to prevent the charges from getting lost to the substrate. The design achieves exact capacitance values in the post-layout simulation, which improves the linearity of the ADC.

In order to experimentally validate the performance of the designed on-chip neural amplifier and the SAR-ADC, most prior work without undergoing the in vivo/in vitro measurements perform standalone bench-top measurements [50–52]. This work proposes an approach to generate the neural signal using National Instrument's LabVIEW and applies a synthetic signal to the read-out circuit through the myDAQ data acquisition device. A LabVIEW-based graphical user interface (GUI) is employed along with a myDAQ device to characterize the neural signal recording system.

The objective of this work involves designing a recording read-out circuit with high gain while minimizing the NEF level. The system is biased in the subthreshold region to reduce power consumption even with a high process supply voltage. The digitization part achieves high linearity, which results in more accurate and precise measurements. The contributions of the paper are as follows: (i) development of a neural signal recording read-out circuit with a low-power and low-noise configuration considering the noise–power tradeoff, (ii) digitization of the acquired signal at a low sampling rate, and (iii) a LabVIEW-based GUI to process and analyze the signal from the read-out circuit. Part of the design of the amplifier is published in [30], while additional simulation and experiments are conducted in this work. The organization of the paper is as follows: Sections 2 and 3 discuss the detailed architectures and design of the amplifier and ADC, respectively. All of the experimental results are included in Section 4, which is then followed by a concluding remark in Section 5.

2. Amplifier Architecture

A neural signal recording system requires very low power consumption in order to ensure the functionality and compatibility of an implantable system and to support a large number of recording sites. Hence, the front end needs to have low-noise performance while also minimizing the EDO. Additionally, in order to prevent saturation due to the

large input DC current resulting from the electrode offset, a large DC input impedance of greater than 100 MΩ is suitable for the neuropotential recording system. The equivalent input impedance in the AP and the LFP frequency bandwidth should also be large enough to match the electrode impedance.

Figure 2 presents a full schematic of the closed-loop amplifier with the two-stage OTA. A fully differential architecture was employed with a resistive-capacitive (R_f–C_f) feedback network. An input capacitance (C_{in}) was used as the AC-coupling capacitor to eliminate the large DC offset voltage at the electrode–tissue interface. The mid-band gain of the amplifier was set by the ratio of the input and the feedback capacitor (C_{in}/C_f). The gain was designed to be 1000 V/V (60 dB) to amplify the APs, which can be as low as ∼1μV, setting the values of C_{in} as 1 nF and C_f as 1 pF. Similarly, C_{in} and C_f were chosen to be 31 pF and 12 nF for detecting the mV-level LFPs with a gain of >50 dB. The low-pass corner frequency (f_L) was determined by the feedback resistor and capacitor, ($f_L = 1/(2 \times pi \times R_f \times C_f)$) and was set to be 0.5 Hz and 250 Hz to accurately detect the LFPs and the APs, respectively. The feedback resistor value R_f was set to be 10 GΩ for a low pole frequency of 0.5 Hz. Another high-pass frequency was achieved by setting R_f as 649 MΩ. Though pseudo-resistors could be one option for the implementation of a high-valued resistor, they may result in higher total harmonic distortion (THD), poor filter performance, and noise due to variation in the process of the chip, supply voltage, and the ambient temperature [53,54]. Since the process design kit does not provide controllable resistors, surface mount off-chip resistors were used in this work to implement the feedback network to achieve the reconfigurable bandwidth. The high-pass corner frequency was set to be ∼300 Hz and ∼15 kHz.

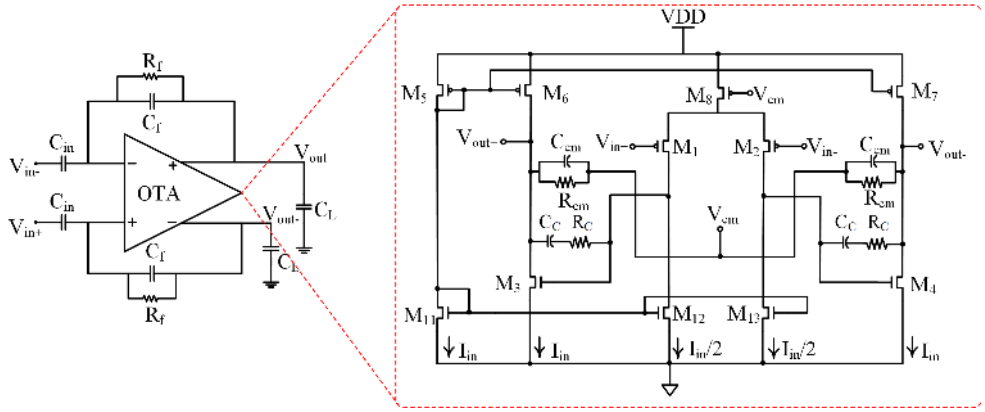

Figure 2. Schematic of the amplifier with the operational transconductance amplifier (OTA).

A fully differential two-stage topology was employed as the OTA in the amplifier design due to its simple and robust architecture [30]. It provides a high DC gain, wide output voltage swing, and good linearity, which are the significant specifications in designing the amplifier. The two-stage OTA also achieves a high common-mode rejection ratio (CMRR) and power supply rejection ratio (PSRR) in comparison with the single–stage counterpart [55]. In this work, the transistors were optimized considering the noise–power tradeoff. To correlate the amplifier performance specifications, this work took into account all the core elements, such as the total bias current, the transistors sizing, and the values of the compensation capacitors and resistors. In order to bring the total power dissipation below 5 μW, the bias current for each branch (I_{in}) was set to 250 nA. At this low bias current, the input transistors were sized to operate in the sub-threshold region. Two PMOS transistors (M_1–M_2) with a large channel width were chosen as the input pair to reduce the low-frequency flicker noise components. The PMOS input transistors also achieve lower common-mode voltage than the NMOS input pair. M_1–M_2 was designed to have the size of 120/1 μm/μm. They achieved a high transconductance over the DC drain current ratio (g_m/I_D) of 28.13 V^{-1}, operating in the weak inversion region, resulting in a high total transconductance of the OTA. NMOS and PMOS current mirror transistors such as

M_{11}, M_{12}, M_{13}, and M_5, M_6, M_7, respectively are used to supply the bias current through each branch. The aspect ratios (W/L) of the transistors, as well as the g_m/I_D are presented in Table 1.

Table 1. Transistor parameters of the operational transconductance amplifier (OTA) shown in Figure 2.

Transistors	W/L (μm/μm)	$\mathbf{g_m/I_D(V^{-1})}$
M_1, M_2	120/1	28.13
M_3, M_4	10/1	22.7
M_{11}	40/1	22.76
M_{12}, M_{13}	20/1	23.5
M_5	120/1	23.82
M_6, M_7	30/1	23.54
M_8	120/1	23.8

Transistor M_8 is biased with the common-mode voltage (V_{cm} in Figure 2) of the OTA, which is set by the common-mode feedback (CMFB) circuitry (1.65 V). In order to ensure stability of the amplifier, a zero is introduced by implementing the common-mode resistance (R_{cm}) and capacitance (C_{cm}). R_{cm} and C_{cm} are designed to be set as 10 kΩ and 1 pF, respectively.

Both the flicker noise ($1/f$ noise) and the thermal noise components contribute to the input-referred noise of the amplifier. The channel gate width of the input pair transistors is set to a high value in the interest of reducing $1/f$ noise since $1/f$ noise is inversely proportional to the channel area [56]. The thermal and $1/f$ noise can be expressed as follows [56].

$$v_{ni,thermal}^2 = \frac{16kT}{2g_{m_1}}\Delta f \tag{1}$$

$$v_{ni,1/f}^2 = \left(\frac{1}{C_{ox} \times \Delta f}\right)\left(\frac{K_n g_{m_1}^2}{(WL)_{M_1}}\right)\left(\frac{1}{g_{m_1}^2}\right) \tag{2}$$

$$v_{ni,1/f}^2 = \frac{K_n}{C_{ox} \times \Delta f}\left(\frac{1}{(WL)_{M_1}}\right) \tag{3}$$

where g_{m_1} is the transconductance of the input transistor M_1–M_2, T is the ambient temperature (300 K), and k is the Boltzmann constant. In this design, g_{m_1} of the input pair is kept high to reduce the effects of thermal noise. The amplifier bandwidth (Δf) is maintained within the neural signal frequency. In the flicker noise Equation (2), the input-referred noise includes the process parameter (K_n), the gate dielectric capacitance per unit area (C_{ox}), and the channel area of the transistor ($W \times L$).

3. ADC Architecture

A low-power ADC architecture is required for the sake of achieving a prolonged battery life for the implantable neural interfaces. To meet the requirements of low power consumption (below 25 μW), low sampling rate (below 100 ksamples/s), and resolution (8–10 b), several architectures are proposed in prior work, such as oversampling modulators [57], single-slope (SSR) or multiple-slope ramp (MSR) ADCs [58], and SAR-ADCs [52]. In this paper, the SAR-ADC architecture is designed due to its simpler architecture as well as meeting all the above criteria.

Figure 3 presents a schematic of the 8-bit SAR-ADC. To reduce the power consumption, a single-ended ADC architecture is implemented in this work. While the single-ended configuration could be prone to common-mode noise, it is mostly eliminated by a high CMRR of the front-end amplifier. It includes an 8-bit charge-scaling digital-to-analog converter (DAC), a sample and hold circuit, a dynamic comparator, and a SAR logic. The sample and hold stage samples the analog input signal and holds until the next sampling

period of the ADC. After sampling, the analog input is compared with the output voltage of the charge-scaling DAC. The output of the comparator is sent to the SAR-logic block. The SAR logic includes a 3-bit counter, D flip-flops, and 3-bit shift registers. After eight consecutive clock cycles, the digital output bits are evaluated and applied to the DAC capacitor array. The clocks at the flip-flops are generated externally using a crystal oscillator.

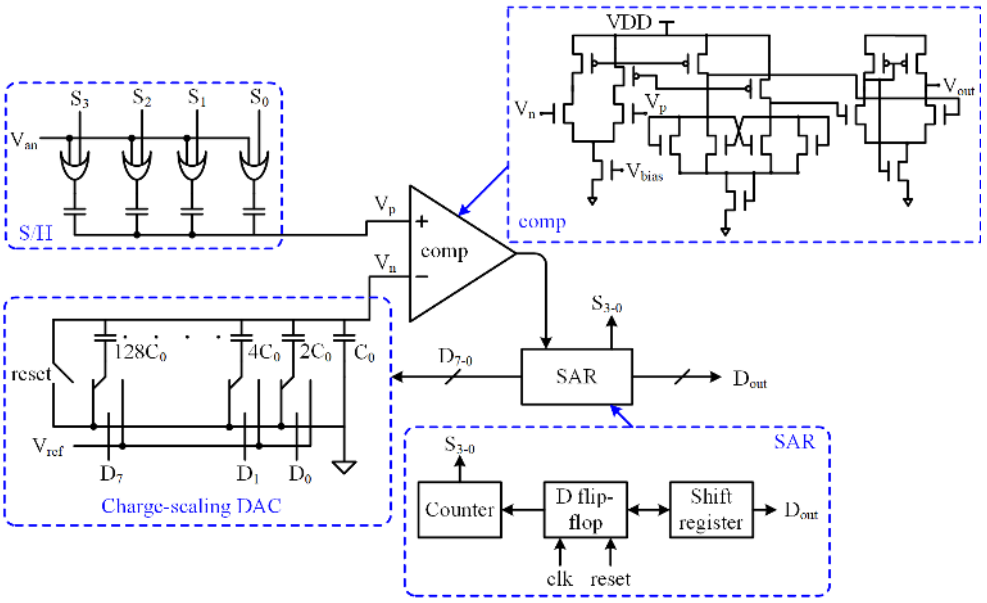

Figure 3. Schematic of the 8-bit successive approximation register analog-to-digital converter (SAR-ADC).

3.1. Charge-Scaling DAC

The charge-scaling DAC is comprised of a parallel array of binary-weighted capacitors. The unit capacitor (C_0) value was chosen to be 35 fF, which resulted in the total capacitance of the array as 8.96 pF. The unit capacitors were designed from the process design kit of the 0.5 µm library. The capacitor was manually laid out from the poly-poly2 layer, which forms the capacitor's top and bottom plate, respectively. Poly-metal1 and poly2-metal1 contacts were used for the layout configuration of the capacitors. The overall capacitance per unit area is found to be 0.048 fF/µm^2 from the post-layout simulation of the DAC. Common centroid placement was adopted for the layout of the capacitors to avoid mismatches.

At the beginning of the digitization, the reset switch at the charge-scaling DAC (Figure 3) was turned on and all the capacitors were switched to reset. During the sampling phase, the analog input V_{an} was sampled and fed to the comparator as V_p. After the sampling period and the initial discharging through the reset, the largest capacitor 128 C_0 was connected to V_{ref}, and the other capacitors were connected to the ground. Since the rest of the capacitor array's total capacitance was equal to 128 C_0, the analog output (V_n) from the DAC after the voltage division became half of V_{ref}. V_n was compared with V_p in the comparator. If the DAC output was greater than the analog input signal, the comparator output V_{comp} changed the most significant bit (MSB) of the SAR logic, which was initially set to 1 while keeping the other bits at 0. Then, in the next clock cycle, the second-largest capacitor 64 C_0 was switched to V_{ref} for the next comparison while still keeping the rest of the capacitors (except 128 C_0) connected to the ground. The comparator repeats the procedure depending on the comparator output until the least significant bit (LSB) is found.

3.2. Comparator

The designed comparator consists of a pre-amplifier, a decision stage, and an output buffer, as shown in Figure 3. In order to improve the comparator sensitivity, the analog input signal is amplified in the pre-amplifier stage. The decision stage (positive feedback)

makes a decision about which input is of higher amplitude. Lastly, the latch provides the output as a digital bit.

The pre-amplifier stage takes the two analog input signals V_n and V_p. The transconductance of the input transistors determines the gain of the amplifier. This stage is employed to reduce the offset and to eliminate kickback noise (switching noise) by separating the sensitive input from the positive feedback stage. The decision stage utilizes positive feedback from the cross-gate connection to further amplify the gain from the decision circuit. The output buffer was employed as the final stage, which converts the decision element into the logic bits (either 0 or V_{DD}). The buffer used in this design is a PMOS differential amplifier driving an inverter.

4. Measurement Results and Discussion

The neural signal recording read-out circuit was designed in the standard 0.5 µm CMOS process. The characterization of each block and the recording and digitization of the synthetic neural signal are described in the below subsections.

4.1. Amplifier Characterization

The neural amplifier was characterized to measure the gain, bandwidth, noise, and power performance. The measured closed-loop gain with the capacitive-resistive feedback network is presented in Figure 4a. The mid-band gain within the LFP bandwidth (0.57–301 Hz) is found as 49.26 dB. In the AP bandwidth of 0.27–12.9 kHz, the gain is measured as 60.53 dB. In order to estimate the gain variability from channel-to-channel mismatches, a Monte Carlo simulation was performed on the closed-loop gain of LFPs. The mean of the simulated AC gain is found to be 49.65 dB for 200 samples, which implies device and process mismatches. The standard deviation of the mid-band gain is evaluated as 276 mdB, which exhibits a trivial effect on the whole circuit. As can be seen from Figure 4b, very few samples go beyond the gain variation window (48.2–49.8 dB). The high gain of the amplifier within the reconfigurable bandwidth of APs and LFPs allows us to achieve a high CMRR, which helps to eliminate common-mode noise. The open-loop gain performance is measured as 67.18 dB, with 14.3 kHz as the unity gain frequency. The DC-offset voltage of the amplifier with the DC-blocking capacitor is measured to be 12 mV.

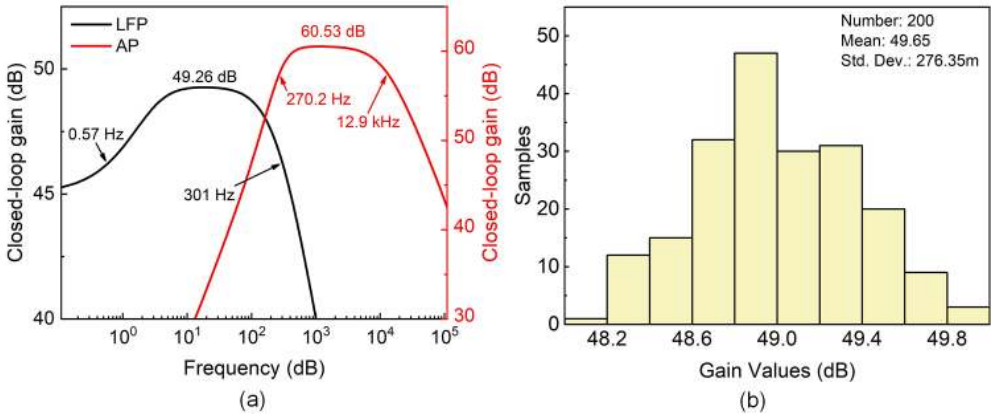

Figure 4. (**a**) Measured closed-loop gain of the amplifier for detecting both the action potential (AP) and the local field potential (LFP) in different bandwidths, (**b**) Monte Carlo simulation of the AC gain of LFPs for 200 samples.

The noise efficiency factor (NEF) of the amplifier estimates the tradeoff between the power consumption and the input-referred noise calculated from Equations (1) and (2). It can be approximated from the following Equation [30]:

$$NEF = v_{ni,rms}\sqrt{\frac{2I_{bias}}{\pi.U_t.4kT.\Delta f}} \quad (4)$$

where $v_{ni,rms}$ is the rms value of the input-referred noise voltage in the bandwidth of interest (Δf). U_t represents the thermal voltage, which is 25 mV. The total bias current through all the branches of the amplifier is I_{bias}. Since the ideal value of the NEF is 1, the lower the NEF, the better the tradeoff performance of the amplifier. Looking into Equations (3) and (4), it can be seen that increasing the channel area (channel width and length) improves the NEF performance. From Equation (4), the NEF is calculated as 2.53 within 0.5 Hz to 12.9 kHz of the frequency bandwidth. In this work, the noise level is kept below 4 µVrms while also minimizing the power consumption as 4.12 µW, which maintains the noise–power tradeoff. The measured CMRR and PSRR of the neural amplifier are found to be 97.1 dB and 84.4 dB.

Table 2 shows the performance metrics of the neural amplifier compared to other prior work. The recording front-end achieves the lowest NEF and the highest gain within the reconfigurable neural signal bandwidth. Although [59] exhibits lower NEF compared to this work, their gain is too low to amplify µV-level signals.

Table 2. Amplifier Performace Comparison.

Amp.	Process (µm)	Supply (V)	Gain (dB)	Power (µW)	BW (Hz)	IRN (μV_{rms})	NEF	CMRR (dB)	PSRR (dB)
Lee et al. [2]	0.035	1.8	40	19.3	1–10 k	2.9	nr	56.4	65.5
Kim and Cha [60]	0.18	1.2	39.2	2.4	1–10 k	5.79	3.2	78	85
Ng and Xu [61]	0.035	3.0	38.1	6	1–9 k	13.3	7.87	74	55
Ng and Xu [62]	0.065	1.0	52.1	2.8	1–8.2 k	4.13	2.93	90	78
Abdelhalim et al. [63]	0.13	1.2	54–60	3.5	10–5 k	5.1	4.4	78	nr
Lee et al. [59]	0.18	1.0	40	0.95	nr	2.88	2.38	nr	nr
Rodovalho et al. [64]	0.18	0.3	51	0.5	0.1–10 k	25.6	nr	37	41
Samiei and Hashemi [65]	0.18	1.2	41–59	2.6	0.5–5 k	3.2	3.2	70	nr
Jomehei and Sheikhaei [66]	0.18	±1.2	60	7.68	102–10 k	3.87	2.65	>50	>53
Nikas et al. [67]	0.18	1.8	37.5	23	1–5 k	7.3	14.2	90	92
This work	0.5	3.3	49.26, 60.53	4.12	0.5–301, 270.2–12.9 k	3.16	2.53	97.1	84.4

IRN: input-referred noise, nr: not reported.

4.2. ADC Characterization

The SAR-ADC was measured using National Instrument's (NI) myDAQ data acquisition device (part number: 781326-01, National Instrument, Austin, TX USA) in LabVIEW GUI. The myDAQ device was used as an interface between the test board and the GUI. The digital i/o pins of the myDAQ card were connected with the ADC's 8-bit outputs. A sinusoidal AC voltage of 100 mV and 1 kHz frequency were applied as the analog inputs to the ADC. The digitized data were collected and converted back to the analog domain to observe the reconstructed signal. The sampling rate of the ADC was set to be 10 ksamples/s, maintaining the Nyquist-rate for the highest frequency of neural signals. The performance of the ADC was validated for the parameters such as the differential nonlinearity (DNL), the integral nonlinearity (INL), the total harmonic distortion (THD) power spectrum, and the signal-to-noise ratio (SNR).

Figure 5 presents the results describing the characteristics of the ADC. In order to be 8-bit accurate, the ADC is required to have a DNL and an INL less than ±0.5 LSB. The measured DNL and INL are 0.32/−0.24 LSB and 0.17/−0.28 LSB, respectively (Figure 5a,b), which confirm less than the maximum error of the data conversion and high linearity.

Figure 5c shows the power spectrum for the fundamental signal and the harmonics. The fundamental signal (set to be 1 dB below full scale) frequency is at 10 kHz. The first harmonic is found to be −59.8 dB. The THD is expressed as the ratio of the summation of the first five harmonics to the power of the fundamental component. Hence, the less the THD is, the more accurate the ADC output would be. The lower amplitude values of the harmonics demonstrate a lower THD. The SNR is found to be 45.75 dB, which is calculated from the ratio of the power of the fundamental input signal to the power of the noise associated with it. The SNR power spectrum is shown in Figure 5d. The ENOB is one of the significant parameters in characterizing the ADC, which expresses the actual bits of resolution. ENOB is calculated from the THD with noise, also known as signal-to-noise-and-distortion (SINAD), and is calculated as below:

$$SINAD = \frac{P_{sig} + P_n + P_{distort.}}{P_n + P_{distort.}} \tag{5}$$

$$ENOB = \frac{SINAD - 10log(3/2)}{20log2} \tag{6}$$

where P_{sig} is the power of the input signal. P_n and $P_{distort.}$ are the noise and other spectral components of the harmonics. The ENOB of the designed ADC is calculated as 7.32 from Equations (5) and (6). The total power consumption of the ADC is measured to be 21.9 µW, with a voltage supply of 3.3 V.

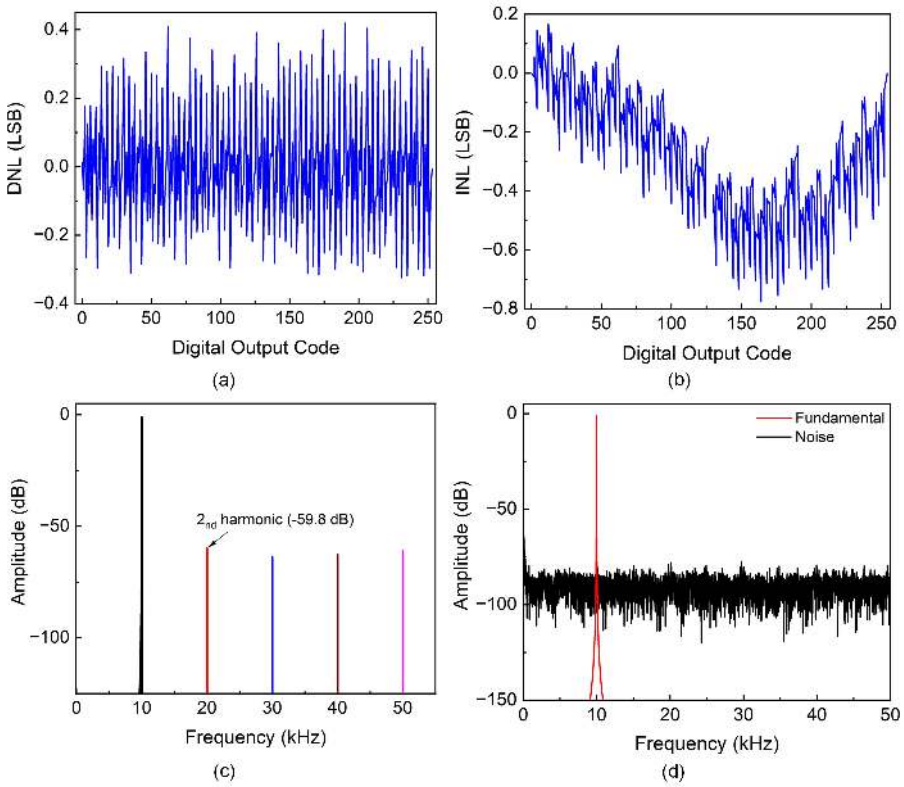

Figure 5. (**a**) ADC differential nonlinearity (DNL), (**b**) ADC integral nonlinearity (INL), (**c**) ADC total harmonic distortion power spectrum (fundamental vs. harmonics), and (**d**) signal-to-noise ratio power spectrum (fundamental vs. noise).

Table 3 presents the performance comparison of the ADC among the prior works. The SAR-ADC exhibits a good SNR value at a lower sampling rate compared to prior work. The figure of merit (FoM) [68] of the proposed ADC is calculated from the Nyquist rate as 31.4 fJ/conversion step, which is better than that presented in prior work. Although [69,70] shows better FoM than this work, the power consumption is very high. While [40,63,68,71]

exhibited a lower power consumption compared to this work, they have a higher DNL and INL, which degrades the linearity performance of the ADC. They also exhibit a lower ENOB. The DNL and the INL in the proposed work present the best linearity performance among the previous works with respect to the 1 LSB change (in volts) in analog signal. The SNR of the proposed work also performs better than most of the works with a comparably lower sampling rate. The SNR shows the ADC's sensitivity to ENOB to effectively digitize analog signals.

Table 3. ADC performance comparison.

ADC	Process (µm)	Supply (V)	Res./ ENOB	DNL (LSB)	INL (LSB)	SNR (dB)	S. Rate (S/s)	Power (W)	FoM (fJ/C-s)
Zou et al. [1]	0.18	1.0	9.5/8.3	0.55/−0.55	1.20/−1.20	51.5	24.5–245	21.66 µ	nr
Shahrokhi et al. [40]	0.35	3.3	8/6.2	nr	nr	nr	111 k	15.5 µ	nr
Wang et al. [41]	0.18	1.8	10/9.77	0.57/−0.47	0.40/−0.38	61.2	25 k	24.81 µ	129
Abdelhalim et al. [63]	0.13	1.2	8/7.6	0.60/−0.60	0.70/−0.70	47.5	100 k	10 µ	nr
Jiang et al. [72]	0.028	1.2	7/nr	0.86/−0.98	1.50/−1.40	36.4	2 G	7.62 m	70.8
Xu et al. [70]	0.055	1.0	8/6.9	0.21/−0.22	0.42/−0.25	43.5	320 M	1.2 m	30
Wang et al. [73]	0.055	1.2	8/6.05	0.93/−0.85	0.71/−0.91	31.8	2.6 G	60 m	348
Chaturvedi et al. [71]	0.13	1.0	8/7.7	0.26/−0.67	0.60/−0.70	48.0	1 M	8.8 µ	42.3
Li et al. [74]	0.065	1.2	8/nr	0.90/−0.60	0.70/−0.70	45.7	350 M	2.1 m	38.1
Oh et al. [69]	0.028	1.1	8/7.36	0.59/−0.58	0.82/−0.82	45.0	1.0 G	2.55 m	16.6
Reyes et al. [75]	0.13	1.2	8/7.12	0.76/−0.58	0.65/−1.08	44.6	3.2 G	3.28 m	218
Aiello et al. [68]	0.04	1.0	8/6.4	1.90/−1.90	1.50/−1.50	40.4	2.8 k	7.3 µ	30.9 k
This work	0.5	3.3	8/7.32	0.32/−0.24	0.17/−0.28	45.8	10 k	21.9 µ	31.4

nr: not reported.

4.3. Neural Signal Amplification and Digitization

The test setup to experimentally validate the fabricated on-chip amplifier and ADC performances are shown in Figure 6. Figure 6a shows a block diagram of the setup, whereas Figure 6b presents the actual test board and LabVIEW myDAQ card with the fabricated chip microphotograph. The single-channel amplifier occupies an area of 0.0144 mm^2, which is very low in the multi-channel neural signal recording configuration. The area of the ADC is 0.375 mm^2, which will be eventually shared among all the channels. The dimension of the designed fabricated chip is 1.5 mm × 1.5 mm, which is packaged in a 7 mm × 7 mm quad-flat no-lead (QFN) packaging.

Synthetic neural signals are generated from Matlab [76] and then applied to the amplifier to amplify the signal using the myDAQ acquisition device. After the amplification, the on-chip SAR-ADC is used to digitize the signal. The same myDAQ device is used to process the digitized data. LabVIEW GUI is used again as the digital-to-analog converter (DAC) to reconstruct the analog neural signal. The NI measurement and automation explorer (NI MAX) from National Instrument, Austin, TX, USA is used to apply the analog input to the amplifier and to acquire the digital output from the ADC.

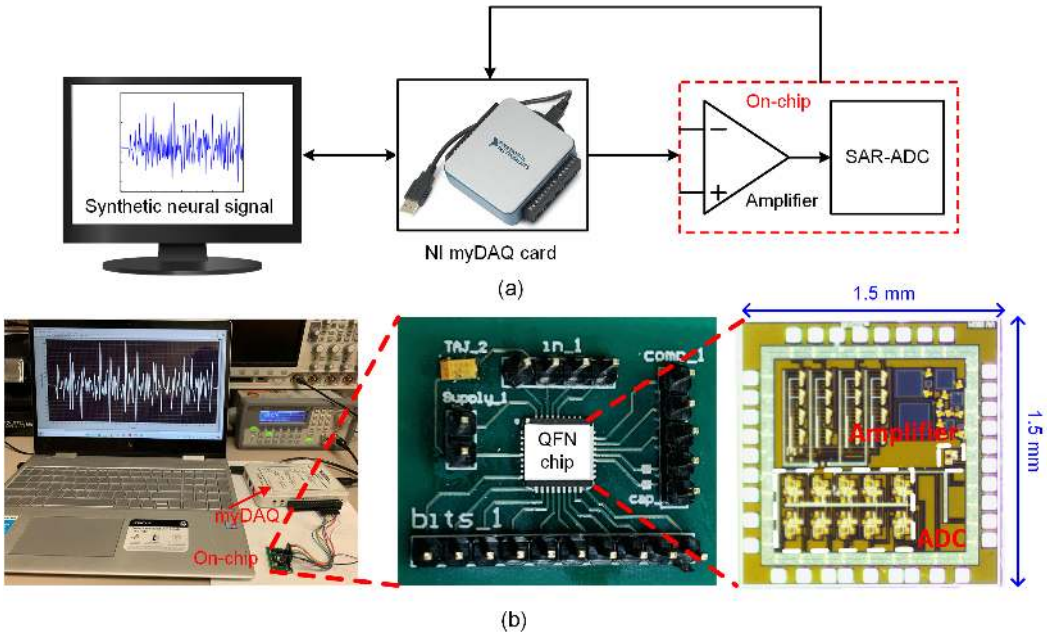

Figure 6. (**a**) Block diagram of the experimental test setup of the system, (**b**) actual test-setup with the quad-flat no-lead (QFN) chip and chip microphotograph.

Figure 7a presents the amplified neural signal for 10 s. The peak-to-peak voltage is 2 V, which shows the amplification of the low-amplitude neural signal of several μVs. This amplified signal is digitized using the proposed ADC and then again reconstructed to compare with the original signal.

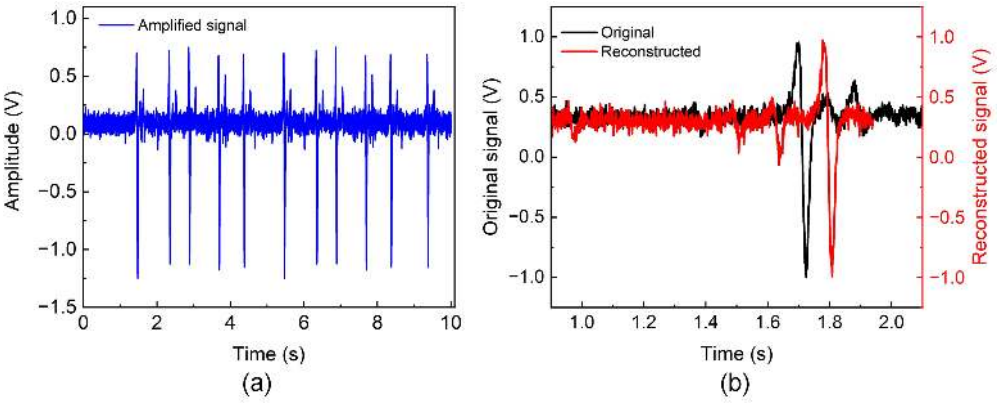

Figure 7. (**a**) Amplified synthetic neural signal, (**b**) reconstructed signal after the digital to analog conversion.

Figure 7b presents the amplified original signal and the reconstructed signal for 1 s as the zoomed view of the full signal. It can be seen from the figure that the reconstructed signal matches the original signal in terms of amplitude and peaks. There exists some time delay between the two signals, which could be due to the RC delay coming from the additional wires, which are used to connect the myDAQ card with the chip. The spikes are detected properly in terms of peak amplitude and frequency of occurrences of the spikes. The standard deviation of the percentage error $((V_{actual} - V_{reconstructed})/V_{actual} \times 100\%)$ between the two signals is calculated as 0.87, which shows the high accuracy performance of the digitization of the ADC. Overall, the high-gain low-noise neural signal recording amplifier along with the ADC in this paper performs well with low power consumption and a high SNR value.

5. Conclusions

This paper presents a power-efficient and low NEF approach for neural signal recording systems. The full system includes a reconfigurable bandwidth amplifier and an 8-bit SAR-ADC, operating at a lower sampling rate with high linearity yet able to construct the signal reliably. This paper also discusses an approach for the measurement system using LabVIEW myDAQ card and GUI for the validation before the in vivo experiment.

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