# A 2.5D Integrated Voltage Regulator Using Coupled-Magnetic-Core Inductors on Silicon Interposer

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***Abstract*—An integrated voltage regulator (IVR) is presented that uses custom fabricated thin-film magnetic power inductors. The inductors are fabricated on a silicon interposer and integrated with a multi-phase buck converter IC by 2.5D chip stacking. Several inductor design variations have been fabricated and tested. The best performance has been achieved with a set of eight coupled inductors that each occupies 0.245 $\mathrm{mm}^2$ and provides 12.5 nH with 270 m$\Omega$ DC. With early inductor prototypes, the IVR efficiency for a 1.8 V:1.0 V conversion ratio peaks at 71% with FEOL current density of 10.8 $\mathrm{A/mm}^2$ and inductor current density of 1.53 $\mathrm{A/mm}^2$. At maximum load current, 69% conversion efficiency and 1.8 V:1.2 V conversion ratio the FEOL current density reaches 22.6 $\mathrm{A/mm}^2$ and inductor current density reaches 3.21 $\mathrm{A/mm}^2$.**

***Index Terms*—Buck converter, DC-DC power conversion, Integrated Voltage Regulator (IVR), switched inductor, 2.5D integration.**

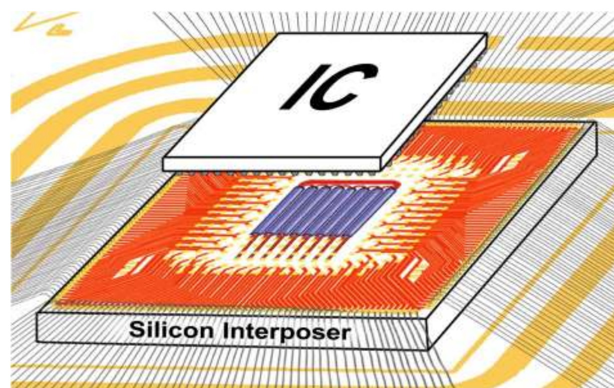


Fig. 1. Diagram of 2.5D integrated voltage regulator (IVR) chip stack. IC with buck converter and load circuitry flips onto interposer with power inductors, which wirebonds to a ball grid array substrate.

## I. Introduction

THE integration of efficient power converters will enable improved performance-power-watt across the full spectrum of digital computing devices, from high-end servers to smart phones. Increasingly, the processors employed in these computing platforms take the form of multicore architectures where workload is shared or parallelized across multiple independent computing cores on the same chip. Energy efficient operation of these cores requires highly granular, active power management, where each core (or even parts of a core) require dynamic supply voltage scaling to allow energy-delay trade-offs to be performed in the presence of workload variability [1]–[3]. At times, these active power management schemes will scale supply voltages to less than 0.5 V in order to achieve circuit operation at minimum power consumption. Voltage transitions will occur within nanoseconds, timescales that are relevant to high-performance digital logic, and voltage regulators will suppress large voltage droops that would otherwise cause the processor to skip operating cycles while the power supply recovers.

Current power delivery implementations employ off-chip, board-level voltage regulator (VR) integrated circuits (along with board level passives) to down-convert independent supply voltages, which are then distributed to a processor through board interconnect and IC packaging. Delivering many supply voltages in this manner requires many external VR modules, an implementation that rapidly becomes interconnect limited both in the distribution of a large number of supplies and in losses associated with moving currents over long interconnect distances. Likewise, the slow switching frequencies of board-level VRs extend supply voltage transition periods to microseconds, while the parasitic interconnect impedance between board VR and processor inhibits the regulator's ability to suppress voltage droop during load current transients. In short, current power delivery technologies based on discrete, board-level VRs are unable to support the type of active power management required of future computing devices.

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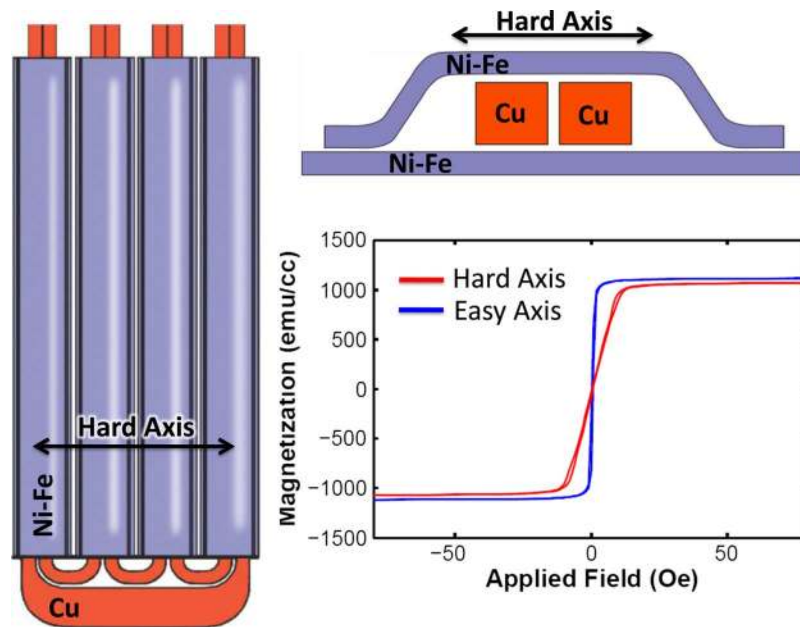


Fig. 2. Top view of four single-turn, coupled power inductors (left), cross-section of magnetic cores and windings (top right) and magnetization curves for the Ni-Fe core material (bottom right).

Switched inductor integrated voltage regulators (IVRs) will operate $\sim$ 100$\times$ faster than board level VRs, enabling dynamic voltage and frequency scaling (DVFS) on nanosecond time scales [4], [5]. Furthermore, IVRs improve efficiency by enabling power delivery at higher voltages in the packaging, reducing $I^2R$ losses in the power delivery network (PDN) and required supply voltage margins. The primary obstacle facing development of IVRs is integration of suitable power inductors that can carry high current levels within a constrained area. This work demonstrates how the challenge of inductor integration can be overcome with an early prototype switched-inductor IVR using thin-film magnetic power inductors that are integrated by 2.5D chip stacking as shown in Fig. 1 [6]. Section II of this paper describes the design and fabrication of the magnetic core inductors that enable the integration of high current density voltage regulators. Section III details the buck converter circuitry that has been designed and fabricated for an IVR test chip. Section IV describes the 2.5D chip stacking method that is used to integrate the magnetic power inductors with the IVR test chip and Section V presents experimental results for the IVR prototype.

## II. Magnetic Core Inductors

Efficient power conversion in a switched-inductor IVR requires inductors that deliver both high current density and high effective inductor efficiency [7]. Planar spiral or other inductor topologies that can be constructed using the interconnects of a typical CMOS process are too resistive to provide efficient on-chip power conversion at reasonable current densities [8]. The efficient use of surface mount technology (SMT) air-core inductors, which can provide a current density up to $\sim$1.7 A/mm$^2$, has been successfully demonstrated [5], [9]–[11]. However, the size and discrete nature of these devices hinders the scalability of any IVR incorporating discrete SMT inductors. Fortunately, advances have recently been made in the development of integrated magnetic-core power inductors that are highly scalable and capable of delivering current densities as high as 8 A/mm$^2$ [12]–[14]. These inductors have been included in IVR prototypes by on-chip integration [15] and chip stacking, as described here. The inductors utilized in this work have been described separately in [14], where several types of inductors were fabricated, both for individual electrical test and integration with a buck converter.

### A. Inductor Design

The power inductor topology that has been chosen for this work is an elongated spiral inductor where two layers of high permeability magnetic material form a cladding around the copper conductor, as shown in Fig. 2, boosting the inductance of the device. Similar topologies have shown high inductance density and quality factor at relevant frequencies [12], [13]. The magnetic cladding is anisotropic. As a result, the hard axis of magnetization, which typically exhibits a more linear relationship between the applied magnetic field and magnetization, is designed to take the same orientation as the induced magnetic field from the elongated dimension of the inductor.

Fig. 2 shows four inductors, where each inductor is coupled with those on either side of it through the magnetic cladding. The outside inductor wraps around so that all of the inductors are symmetrically coupled with their neighbors. In order to achieve inverse coupling, the inductors are driven by the buck converter such that the DC currents through the windings within a magnetic cladding travel in opposite directions. This inverse coupling helps to avoid magnetic saturation in the cladding, improving maximum achievable current densities [16]. This is possible in the case of a multi-phase buck converter because the DC current through each of the inductors is balanced such that the DC magnetic field from adjacent windings is equal and

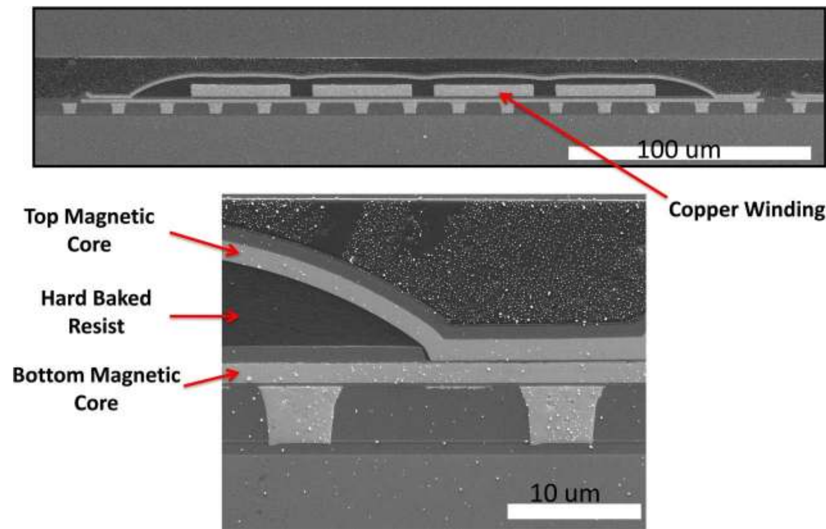


Fig. 3. SEM cross section of magnetic power inductors.

opposite, effectively canceling the DC field in the magnetic cladding. This inverse coupling also reduces inductor current ripple and improves transient response [17]. The current density benefit that is obtained from inverse coupling for the case of a two-phase buck converter with our inductor structures is modeled and verified in [18]. Similarly, the improvement in effective inductor efficiency and current density obtained with inverse coupling in multi-phase buck converters is modeled in [7].

## B. Inductor Fabrication

The inductors are fabricated on 200 mm silicon wafers in the Microelectronics Research Laboratory (MRL) at the T. J. Watson Research Center. The bottom and top inductor yokes are electroplated galvanostatically in a paddle cell. Physical vapor deposited (PVD) $\mathrm{Ni_{80}Fe_{20}}$ films, 65 nm thick, are used as the electroplating seedlayers; a bias magnetic field is applied during seedlayer deposition to produce magnetic anisotropy. The magnetic yokes are plated through photoresist-defined molds (thru-mask plating method). This method gave smooth yoke edges, edge smoothness being important to avoid the nucleation of magnetic domains and pinning of domain walls. To ensure good yoke deposit thickness and composition uniformity, the field around the yokes is also plated up at the same time as the yokes, a thin resist frame separating both plated regions. During plating, a dc magnetic field is applied along the longest axis to define the magnetic anisotropy of the yokes. The presence of the field material ensures continuous magnetic flux across the whole 200 mm wafer, which is critical for obtaining good magnetic anisotropy.

After yoke plating, resist mask stripping, and plated field and seedlayer etching, a bilayer of PECVD SiNx and TEOS dielectric ($\sim 1\ \mu\mathrm{m}$ in total thickness) is used to encapsulate the yokes. After bottom yoke fabrication, the magnetic vias, where the top and bottom yokes contact, are opened by reactive ion etching (RIE). Following plating seedlayer deposition, copper coils are electroplated through resist masks to a thickness of about 5 $\mu\mathrm{m}$.

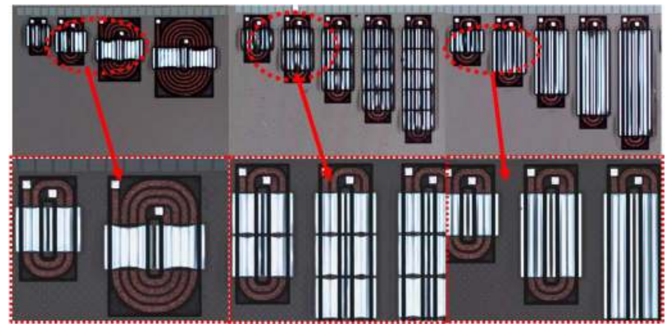

Fig. 4. Pictures of magnetic core inductors fabricated for individual electrical test.

After resist mask and seedlayer removal, 6-$\mu\mathrm{m}$-thick photoresist (AZ Electronics P4620) is used to encapsulate the coils. After patterning, the photoresist is briefly reflowed at 120°C to give sloped sidewalls, ensuring that the top yokes gradually extended to the magnetic via, avoiding the formation of any abrupt angle, which could saturate or pin domain walls. Finally, the photoresist is hard-baked at 200°C for 2 hours to form a rigid encapsulant. The hard-baked photoresist structures exhibit smooth and partially planar surfaces in advance of top yoke plating.

After top yoke fabrication and encapsulation by a bilayer of PECVD SiNx and TEOS, inductor fabrication is concluded by opening the electrical contacts (Cu pads) using RIE. Fig. 3 shows cross-sections of a single-turn inductor and a magnetic via, while Fig. 4 shows several non-coupled inductors that are fabricated specifically for electrical test.

## C. Magnetic Material Properties

The resistivity of the electroplated $\mathrm{Ni_{45}Fe_{55}}$ is measured to be about 45 $\mu\Omega \bullet \mathrm{cm}$ using the four-point probe method, which is double the resistivity of Permalloy ($\mathrm{Ni_{81}Fe_{19}}$). This higher resistivity helps to reduce eddy current at high frequency. Fig. 2 shows the magnetic hysteresis loops, which are obtained using a vibrating sample magnetometer (VSM), of a plated

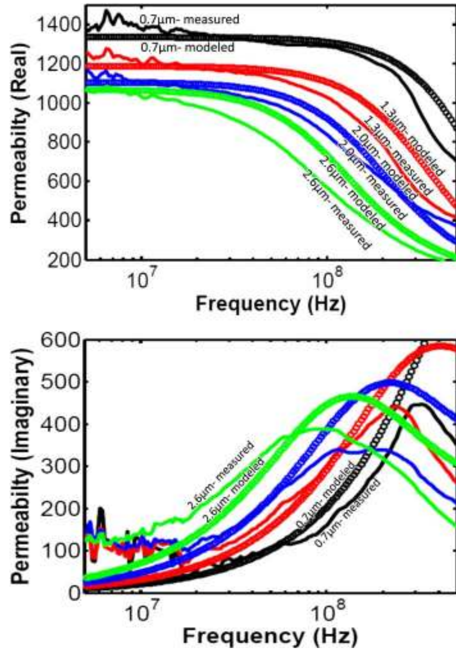


Fig. 5. Complex permeability spectra of $Ni_{45}Fe_{55}$ films with different thicknesses. For comparison, theoretical permeability spectra are also shown in the circle lines.

$Ni_{45}Fe_{55}$ film with a thickness of 2.0 $\mu$m. The film shows clear anisotropy with a low coercivity of 0.2 Oe along both easy and hard axes. Saturation magnetization and anisotropy fields are 1.5 T and 13 Oe, respectively. Complex permeability spectra are obtained by measuring the impedance of a single-stripe loop fixture loaded with magnetic films. Fig. 5 shows the real and complex permeability spectra of plated $Ni_{45}Fe_{55}$ films with different thicknesses. For comparison, theoretical permeability spectra are also shown in the circle lines. The low frequency permeability reaches a value of 1300 for the 0.7 $\mu$m films. As the thickness of the film increased, the value decreases to about 1000 for the 2.6 $\mu$m film due to the shape anisotropy induced in the thicker films. In addition, due to eddy current and skin effects, the roll-off frequency decreased from 200 MHz to 50 MHz as the thickness increases.

## III. Integrated Buck Converter

An eight-phase buck converter has been designed to drive the magnetic core power inductors. The controller is designed to accommodate any number of inductor phases up to eight, with variations of inductance values and coupling strengths. The buck converter IC is designed and fabricated in IBM's 45 nm SOI technology. The IC is shown in Fig. 6 and includes the buck converter, a network-on-chip that acts as a realistic on-chip load, an artificial load used for characterizing the buck converter, and input and output decoupling capacitance. Within the buck converter, the control circuitry occupies 0.178 $\mathrm{mm}^2$, while the bridge FETs occupy 0.1 $\mathrm{mm}^2$. The bridge FETs are thick-oxide devices, capable of withstanding a maximum $V_{ds}$ of 1.8 V. A total of 48 nF of deep-trench (DT) and thick oxide MOS capacitance decouples $V_{OUT}$ and occupies 0.40 $\mathrm{mm}^2$, while 21 nF of DT occupying 0.52 $\mathrm{mm}^2$ decouples the 1.8 V input supply to compensate for the large PDN impedance (due primarily to the wirebond connections in this prototype).

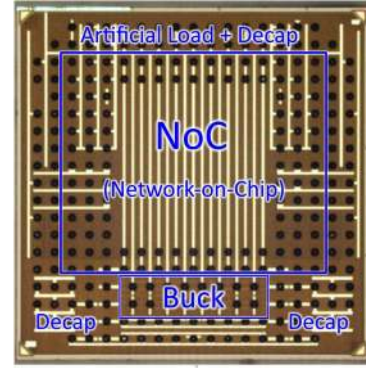


Fig. 6. Photograph of buck converter IC.

### A. Feedback Controller

Fig. 10 shows a system level diagram of the IVR. The buck converter control circuitry resides on the IC and is composed of two control loops, a slow voltage-mode outer loop that provides low-frequency regulation and a fast inner loop that responds to high-frequency load transients. The digital pulse-width modulator (DPWM) receives an eight-bit voltage identifier code (VID), from which it derives up to eight pulse-width modulation (PWM) signals with programmable switching frequency, $f_s$, and phase relationships. The resolution of the DPWM is limited to the 250-ps period of a high-frequency reference clock provided by an on-chip PLL. The DPWM also generates an analog reference voltage, $V_{REF}$, from a clean 1.8 V for the outer feedback loop. The compensator for the outer feedback loop is a low-pass filter with programmable pole frequency, typically chosen 10 to 16 times lower (depending on inductance value) than the effective switching frequency $Nf_s$, where $N$ is the number of phases in operation. The outer feedback voltage, $V_{FB,O}$, drives a delay line that modulates the DPWM output to create the reference PWM signal, $V_{PWM}$, which subsequently drives the fast non-linear inner control block.

The fast inner loop is shown in Fig. 7. Signal $V_{PWM}$ drives an RC filter to generate the inner reference voltage, $V_{REF,I}$, while the bridge output voltage for each phase, $V_{BRIDGE}$, drives another RC filter to generate the inner feedback voltage, $V_{FB,I}$. The pole in both RC low-pass filters is chosen to be below $f_s$ so that the steady state amplitude of $V_{REF,I}$ and $V_{FB,I}$ is around 150 mV, which gives a small signal feedback gain of ~30 V/V and ensures stable loop dynamics. In steady state, $V_{FB,I}$ will slew behind $V_{REF,I}$ and the resultant evaluation of the comparator causes $V_{BRIDGE}$ to closely track $V_{PWM}$. In the event of a large load current transient, the error in the output voltage, $V_{OUT}$, will couple across $C_{FB}$ onto $V_{FB,I}$ and the comparator will react immediately to reduce overshoot in $V_{OUT}$. This fast non-linear response can reduce the required decoupling capacitance on the output voltage $V_{FB,I}$.

### B. Integrated Network-on-Chip Load

Also residing on the IC is a 64-tile network-on-chip (NoC) consisting of four parallel, heterogeneous, physical network

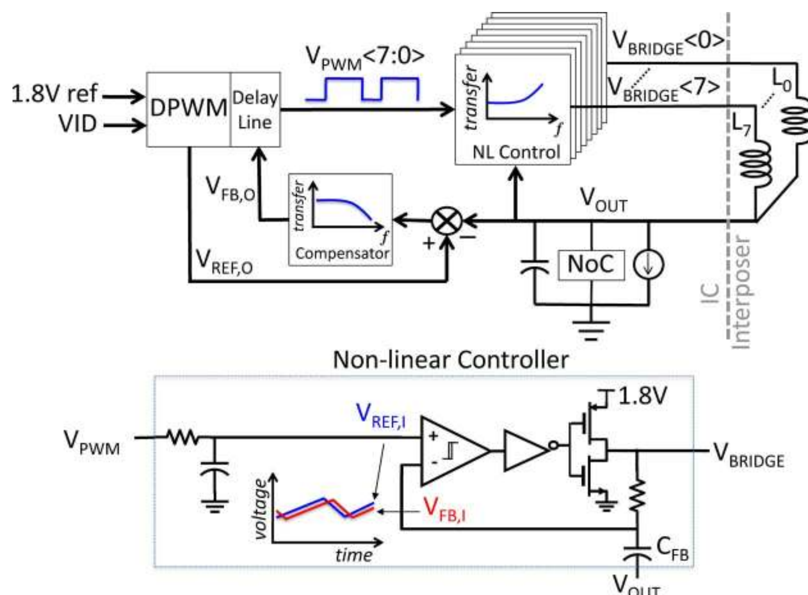


Fig. 7. Complete IVR system overview (top) and fast non-linear control loop (bottom).

planes with independent frequency domains. The NoC provides a highly scalable platform for exploring granular power distributions given the ease with which traffic patterns can be used to modulate load currents and transients. NoCs are becoming the basic interconnect infrastructure for complex SoCs. Since communication plays a key role in SoCs and given the very strict energy and performance requirements imposed on NoCs, recent designs have reserved a separate voltage-clock domain for the NoC alone [2]. The NoC provides realistic load behavior and supports experimentation on supply noise and DVFS. In addition, an artificial load on the IC is capable of generating large current transients with ~0.02 A/ps slew for characterization of the feedback controller.

## IV. 2.5D Chip Stacking

Fig. 8 shows a photograph of the complete 2.5D chip stack. The buck converter IC is flip-chip attached to the silicon interposer, which holds the custom fabricated coupled power inductors while breaking out signals and the 1.8 V input power supply to wirebond pads on the perimeter of the interposer. These signal and power nets are wirebonded to a generic BGA laminate, which is subsequently placed in a socket for electrical test. Once the buck converter IC has been attached to the interposer, the bridge FETs on the IC are able to drive current from the 1.8 V input supply through the inductors on the interposer. This current will pass through the inductors and then back into the IC through C4 bumps where it is then distributed to the load across the on-chip power distribution network. Four variations of power inductor have been fabricated on the silicon interposer as shown in Fig. 9: four uncoupled two-turn inductors (type 1), eight single-turn coupled inductors (type 2), eight two-turn coupled inductors (type 3) and two sets of four single-turn coupled inductors (type 4). The C4 footprint of the prototype IC is designed to leave a total of 3.2 $\mathrm{mm}^2$ in the center of the interposer for the inductors, although most inductor variations use less than the available area.

The power inductors are not integrated in the front-end-of-line (FEOL) of the CMOS technology and so the area consumed

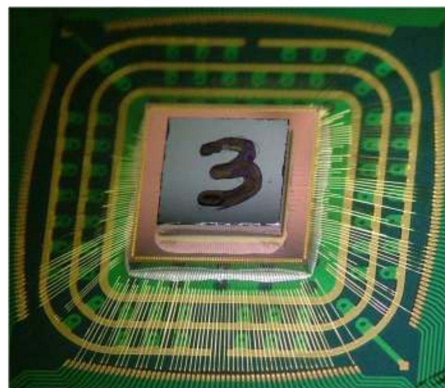

Fig. 8. Photograph of packaged 2.5D IVR chip stack.

by these devices comes at substantially reduced cost. For this reason, the primary constraint on the inductor area in a chip stacking integration scheme is set by the scalability of the IVR solution, rather than cost of area consumed by the power inductors. The maximum current density of a candidate inductor topology must match, or exceed the current density of the load. This will allow the inductor to reside within the perimeter of the load, and in the case of a multi-core architecture, would provide perfect scalability, where multiple cores can be stamped across the load IC, with their corresponding set of inductors stamped across the interposer in the same way. In a worst case, modern high performance digital logic can consume current at levels as high as 2 $\mathrm{A/mm}^2$, current density levels that are exceeded by the power inductors employed here.

A significant downside to the 2.5D chip stacking method is the large impedance of the power delivery network (PDN). The combined impedance in the PDN from the socket, package, wirebonds, and interposer traces is 70 $\mathrm{m}\Omega$ at DC, and increases with frequency due to the inductance of the wirebonds and other traces. The resistive losses from the PDN are a major source of inefficiency for the system, and the high frequency impedance severely impairs the ability of the voltage regulator to suppress

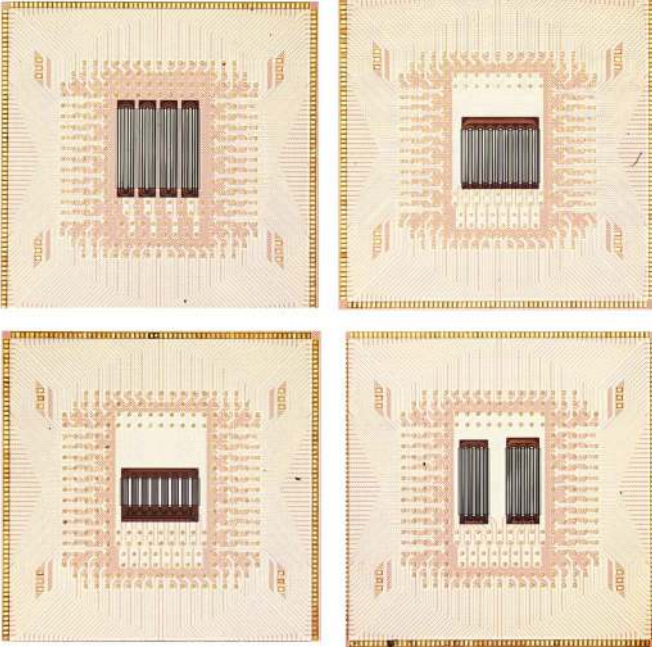

Fig. 9. Photographs of the four types of silicon interposer that were tested with the buck converter IC: Four uncoupled two-turn inductors (type 1—upper left), eight single-turn coupled inductors (type 2—upper right), eight two-turn coupled inductors (type 3—lower left) and two sets of four single-turn coupled inductors (type 4—lower right).

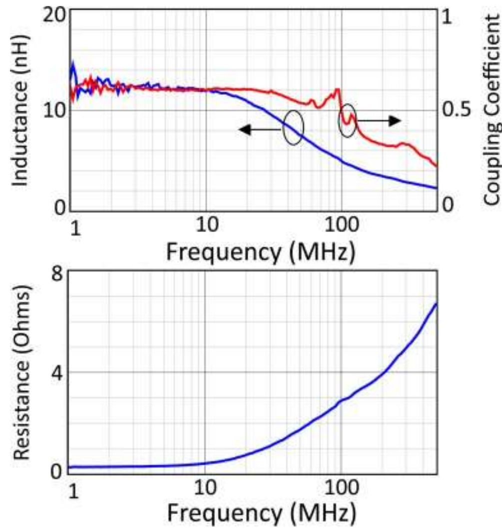


Fig. 10. Inductance (L), coupling coefficient (K) and resistance (R) of coupled single-turn inductors.

voltage droop during load current transients. For this reason, a fully 3D integration approach that incorporates thru-silicon-vias (TSVs) in the interposer would be favorable for high current applications, as it would result in substantially reduced PDN impedance.

## V. Experimental Results

### A. Magnetic Core Inductors

The inductance, coupling coefficient and resistance of a single turn, 1200 $\mu$m inductor with 2 $\mu$m thick magnetic layers is shown in Fig. 10. The performance exhibited here is representative of the coupled, single-turn inductors that have been fabricated on

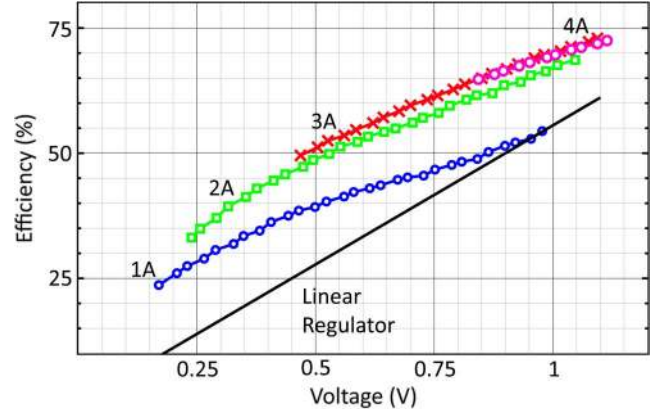


Fig. 11. Efficiency as a function of output voltage at various load currents for the IVR with Type 2 silicon interposer.

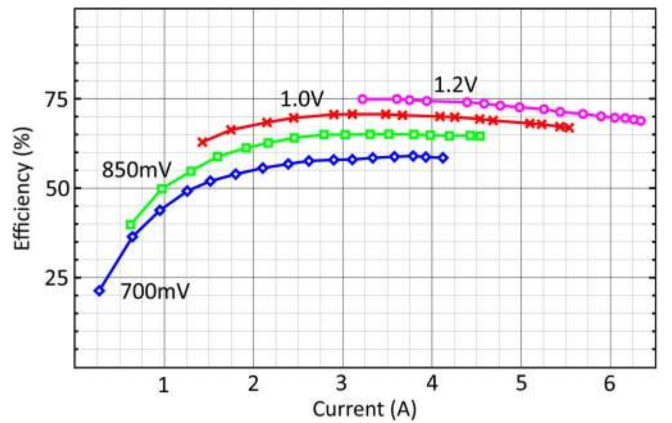


Fig. 12. Efficiency as a function of load current at various output voltages for an IVR with Type 2 silicon interposer.

the interposer. The DC inductance of 12.5 nH is suitable for integrated power conversion, but eddy currents are induced in the magnetic core starting in the 10–100 MHz range, which subsequently causes the inductance and eventually the coupling to fall off. At the same time we see that the eddy currents in the core, as well as the winding skin depth and proximity effect result in an increase in the winding resistance over the same switching frequency. This performance is consistent with the measurements of permeability shown in Fig. 5, and is expected to improve significantly with the addition of insulating laminations in the magnetic core, which will suppress eddy currents.

### B. Integrated Voltage Regulator

The 2.5D IVR chip stack has been assembled and tested in order to verify functionality. In all DC measurements, the resistive losses from the PDN have been excluded and the input voltage has been compensated, such that the input voltage at the IC is truly 1.8 V. All measurements have been conducted with the silicon interposer carrying eight single-turn coupled inductors, unless otherwise noted, as this inductor configuration provides the best performance.

*1) Efficiency:* The efficiency as a function of output voltage and load current for the IVR is shown in Figs. 11 and 12. The efficiency peaks at 75% with output voltage of 1.2 V and load current of 3.2 A. The peak efficiency at 1 V is 71% when the load current is 3 A. The maximum load current that has been

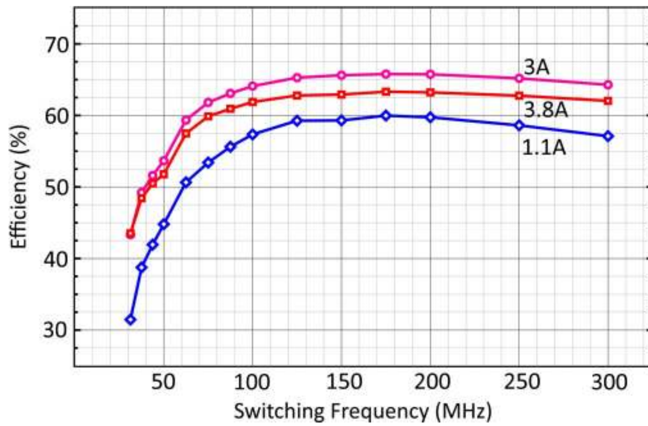

Fig. 13. Efficiency as a function of switching frequency at various load currents for an IVR with Type 2 silicon interposer.

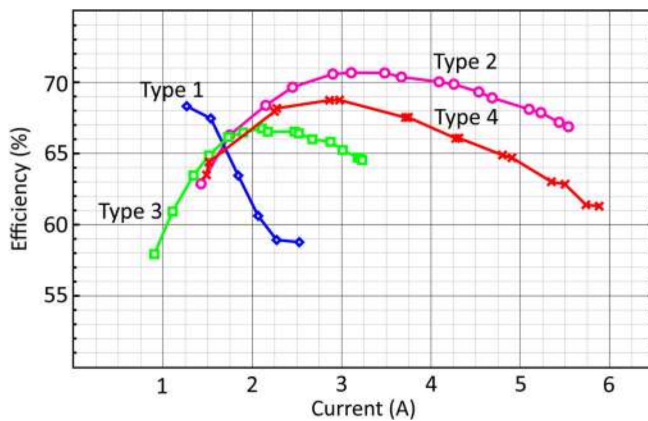

Fig. 14. Efficiency as a function of load current at 1 V output voltage for IVRs with four different kinds of power inductor.

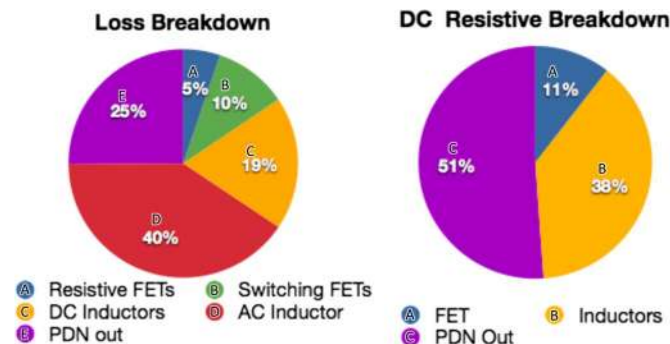

Fig. 15. Loss breakdown and resistive breakdown for an IVR with Type 2 silicon interposer operating with 1 V output and 3 A load current.

measured for the IVR is 6.3 A, limited by the on-chip load. Fig. 13 shows the efficiency of IVR when operated at various switching frequencies and load currents. The optimal switching frequency for the IVR is in the range of 125 to 200 MHz. The efficiency as a function of load current for each of the four inductor variations is shown in Fig. 14, where the eight single-turn coupled inductors configuration (type 2) is clearly the most efficient. A breakdown of the IVR losses is shown in Fig. 15 for the case of a 1 V output voltage and 3 A load current. At this operating point, approximately 40% of all inefficiency is due to

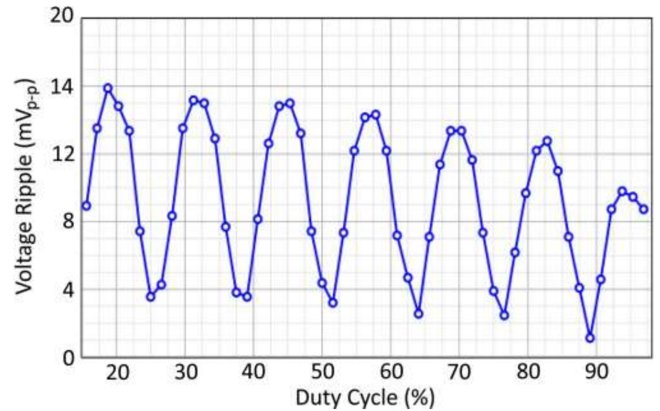

Fig. 16. Output voltage ripple of an IVR with Type 2 silicon interposer operating at 100 MHz switching frequency.

the high-frequency losses in the inductor, which can primarily be attributed to the formation of eddy currents in the magnetic core, as described in Section V-A.

Another major source of loss is the on-chip power distribution network resistance, as described in Section IV. This IVR prototype is designed to act as a flexible platform for testing various power inductor topologies. Therefore, in the case of the power distribution network, optimal design has to be compromised for flexibility. In this prototype, once the load current passes through the inductors it enters the on-chip power distribution network through C4 bumps near the buck converter. The load current then travels across the on-chip power distribution network (approximately 3 mm) to the artificial load, where the output voltage is measured. The on-chip power distribution network resistance of approximately 45 $\mathrm{m\Omega}$, is accountable for 25% of the converters losses. The remainder of the conversion loss is attributed to the DC resistance of the inductors and the switching and resistive losses of the bridge FETs.

The IVR that integrates eight single-turn coupled inductors (type 2) down converts with peak efficiency at a load current of 3 A, and achieves a maximum current of at least 6.3 A. The inductors occupy 1.96 $\mathrm{mm}^2$. Current density for these devices at peak efficiency is 1.53 $\mathrm{A/mm}^2$, and the peak current density is 3.21 $\mathrm{A/mm}^2$. The FEOL area consumed by the buck converter, controller, bridge FETs and some input decoupling capacitance is 0.278 $\mathrm{mm}^2$. At peak efficiency, therefore, the FEOL current density for this IVR is 10.8 $\mathrm{A/mm}^2$, while the maximum current density is 22.7 $\mathrm{A/mm}^2$. In this calculation we exclude the area of some input decoupling capacitance, as this capacitance would not be required in a fully 3D integration approach, where the PDN impedance would be lower.

*2) Voltage Ripple:* Fig. 16 shows the output voltage ripple from the IVR as a function of duty cycle when the buck converter is operating at a switching frequency of 100 MHz. The peak voltage ripple is 14 mV peak to peak, this occurs when $1/16 = mod(D, 1/8)$, where D is the duty cycle. The best case voltage ripple of 3 mV peak to peak occurs when $0 = mod(D, 1/8)$, when the inductor current ripple from each of the eight phases almost perfectly cancel. The IVR voltage ripple is expected to improve dramatically as insulating laminations are added to the magnetic yoke of the inductors, which will improve high frequency inductance.

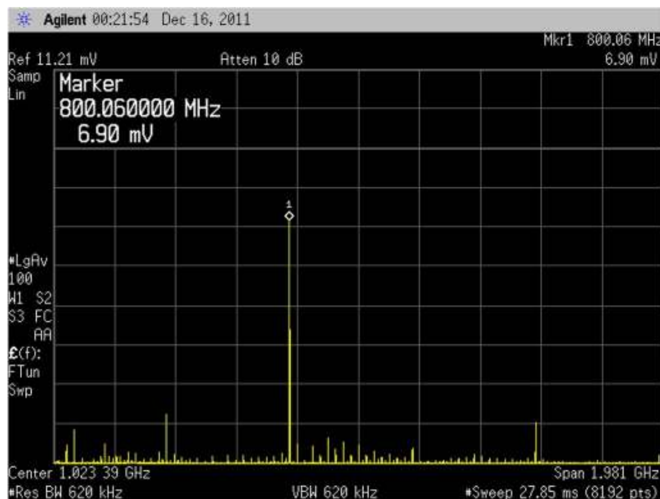


Fig. 17. Frequency spectrum of output voltage for IVR with Type 2 silicon interposer operating with switching frequency of 100 MHz.

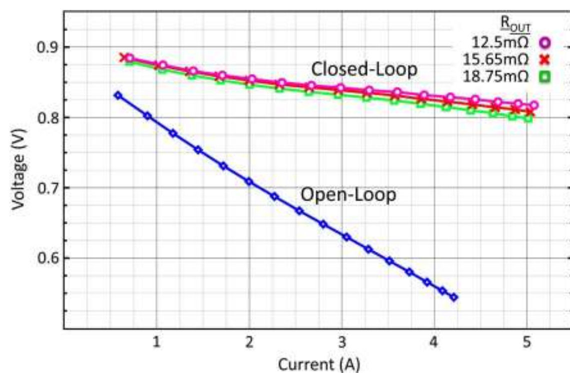


Fig. 18. Output voltage as a function of load current for IVR with Type 2 silicon interposer operating with various feedback settings.

*3) Supply Noise:* Fig. 17 shows the frequency spectrum of the output voltage when the buck converter is switching at 100 MHz. The dominant tone in the output voltage occurs at 800 MHz, which is the eighth harmonic of the switching frequency and is consistent with expectations for an eight-phase buck converter. The limited spectral content at other harmonics of the switching frequency indicates that the current through each of the eight inductors is well balanced. This result confirms that asymmetry in the inductor design, which results from having the outside inductor phase wrap around as shown in Fig. 2, has negligible impact on the inductor current balance.

*4) Voltage-Mode Feedback Controller:* The large impedance of the input PDN significantly impairs the ability of the feedback controller to suppress load current transients, as the input power supply droops significantly. However, the load-line regulation capability of the outer voltage-mode feedback loop is confirmed in Fig. 18, where the closed loop output impedance is significantly reduced with respect to the open loop output impedance. The gain of the error amplifier in the outer feedback loop can be increased, within the feedback stability constraints, to reduce the closed loop output impedance of the IVR.

## VI. Conclusions

An eight-phase integrated buck converter that utilizes custom fabricated thin-film magnetic power inductors has been demonstrated. The IVR prototype provides exceptional current density; however, conversion efficiency has been hampered by the occurrence of eddy currents in the inductor's magnetic core material. The incorporation of insulating laminations into the core, or the development of suitable magnetic materials with higher resistivity, will significantly improve the inductor's efficiency, and will enable the integration of high current density power converters on a large scale. This type of highly integrated power converter will enable significant improvements in performance-per-watt across the scope of digital computing platforms. IVRs will enable precise control of the supply voltage so that power consumption closely tracks computational demand, significantly improving energy efficiency of the system.

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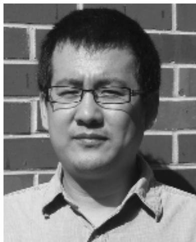

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