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A 2-D Distributed Power Combining by Metamaterial-Based Zero Phase Shifter for 60-GHz Power Amplifier in 65-nm CMOS

Wei Fei, *Student Member, IEEE*, Hao Yu, *Member, IEEE*,
Yang Shang, *Student Member, IEEE*, and Kiat Seng Yeo, *Senior Member, IEEE*

***Abstract*—Based on a newly introduced zero phase shifter (ZPS), a 2-D distributed power-combining network is developed in this paper to provide simultaneous distributed amplification and power combining. One type of metamaterial, called the composite right/left-handed transmission line, is deployed to design ZPS with detailed considerations to achieve low loss and wideband performance. The proposed 2-D distributed power combining is implemented for one 60-GHz power amplifier (PA) design by a UMC standard 65-nm CMOS process. Measured results show that the fabricated PA has 0.39-mm^2 area, 8.3-dB gain, 7.1% power-added efficiency, and 9.7-dBm P1 dB with 16-GHz bandwidth (44–60 GHz).**

***Index Terms*—Metamaterial, millimeter-wave integrated circuits, power amplifiers (PAs), power combining, 65-nm CMOS.**

I. Introduction

THE PRIMARY design challenges of CMOS power amplifiers (PAs) at 60 GHz for high data-rate communication systems [with ∼9-GHz bandwidth (BW)] [1]–[7] are mainly *low output power/power-added efficiency (PAE)* and also *narrow BW*. Although the maximum radiation power for 60-GHz systems is allowed up to 40 dBm according to the Federal Communications Commission (FCC) regulations [8], the low supply voltage and breakdown voltage of deeply scaled CMOS technologies severely limit the achievable output power for one single transistor with reasonable gain. Lossy substrate aggravates this problem with limited PAE. On the other hand, the wide spectrum at the millimeter-wave region along with large process variation in advanced CMOS technology calls for a wideband performance. Existing techniques such as negative feedback and resistive matching are no longer viable for 60-GHz applications [9]. One recent technique by shifted matching is proposed in [9]. Although a flat wideband performance is achieved using this method, the measurement shows a low PAE. In conclusion, achieving the power and BW requirements is a challenge due to low breakdown voltage and relatively large parasitic capacitance for CMOS devices [9]. Design iterations between PAE and BW have become more and more complicated, while sufficient power gain and linearity should still be maintained within a compact layout.

Power combining can improve output power and PAE at 60 GHz [3], [5]. Numerous power-combining techniques have been published for 60-GHz CMOS applications [3], [5], [8], [10]–[12]. The most straightforward method is to use a Wilkinson power divider/combiner, as implemented in [8]. It has the advantage of easy implementation, low loss, and good isolation between ports. However, the required $\lambda/4$ transmission line (T-line) occupies a large area. Two modified techniques are implemented in [5] and [3]. The first one merges the power-combining/dividing function into the existing matching network, which is still bulky in area. The latter one, on the other hand, uses a 0° power divider instead, which eliminates the resistor and is much more compact. Its limitation is the stringent requirement for all signals to have the same frequency, phase, and amplitude for proper combining. Another widely explored device for power combining is the transformer. The distributed active transformer (DAT) has been proven as an efficient method for power combining [10], [11], [13]. However, the maximum output power density that can be achieved by the transformer is still limited due to its 1-D power-combining nature. New combining methods with novel concepts, such as the electrical funnel [14], have also been explored in the millimeter-wave region and beyond, but issues such as large size and low PAE still remain unresolved.

Wide BW, on the other hand, is usually achieved by distributed amplification in the millimeter-wave region. One major limitation for traditional distributed PA is its low PAE. As shown in Fig. 1(a), each transistor outputs different power; therefore the transistors cannot be optimized simultaneously [2]. The power wasted in the resistive terminations further degrades the efficiency. Both T-line and transistor sizes are tapered in [2] to realize the maximized output voltage swing at all distributed stages [see Fig. 1(b)]. Although each transistor still outputs different power, the same voltage swings are maintained due to scaled transistor sizes. However, the large scaling ratio between transistor stages limits the achievable number of distributed stages and thus output power. What is more, resistive terminations still consume power and degrade efficiency. A new distributed amplifier (DA) called the dual-fed distributed

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The authors are with the School of Electrical and Electronic Engineering, Nanyang Technological University, 639798 Singapore (e-mail: haoyu@ntu.edu.sg).

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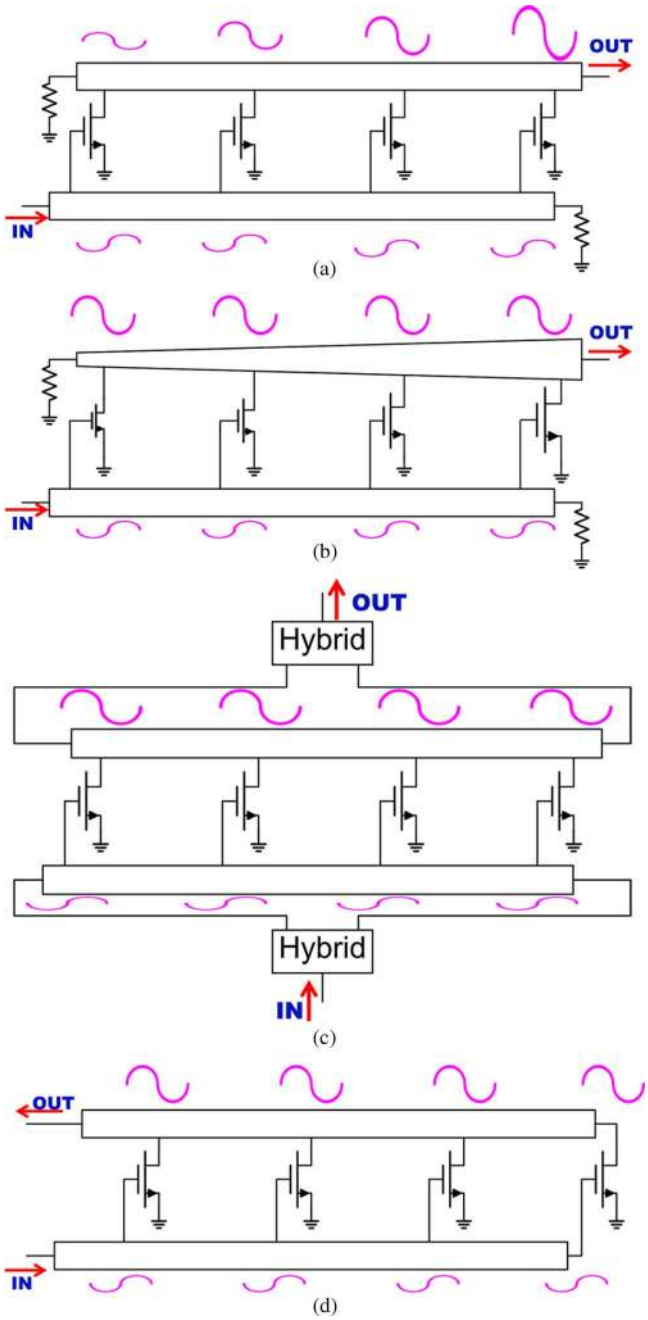

Fig. 1. DA topologies. (a) Conventional DA. (b) Tapered DA [2]. (c) DFDA [15]. (d) SEDFDA [17].

amplifier (DFDA) was proposed in [15], which can significantly improve the PAE limitation for distributed PAs. As shown in Fig. 1(c), the input signal is split into two paths and fed into both ends of the gate line. The two outputs from the drain line are then combined again as the output signal. It has been proven that when a phase shift of $\pm n\pi$ $(n = 0, 1, 2, \ldots)$ is maintained between transistors in both gate and drain lines, all transistors can see the same load, and output the same power [16]. As a result, they can be optimized simultaneously. Moreover, the resistive terminations are eliminated in the DFDA, and there is no additional power wasted. As a result, the PAE limitation of distributed PAs can be resolved fundamentally. The DFDA is further developed in [17] as single-ended to eliminate the need of a hybrid. The resulted topology is shown in Fig. 1(d), which is called the single-ended dual-fed distributed amplifier (SEDFDA). Both input and output signals propagate to the open-circuit ends and are reflected back. Since both forward and reflected signals add up to each other under certain phase shift of the T-line, the power gain is further improved.

Note that both the DFDA and SEDFDA require a phase shift of $\pm n\pi$ $(n = 0, 1, 2, \ldots)$ to be maintained between transistors in both gate and drain lines. Since zero phase shift $(n = 0)$ is impossible to be realized by the traditional T-line (which introduces phase shift proportional to the T-line length), a $\lambda/2$ T-line is used at the printed circuit board (PCB) level to fulfill the phase-shift requirement, which is, however, too bulky and lossy for on-chip implementation. One type of metamaterial called the composite right/left-handed (CRLH) T-line can be used to realize a real zero phase shift, and is implemented for DA design in [16] and [18] at the PCB level for gigaheretz region applications. However, at this frequency region, the CRLH T-line is too bulky and lossy for on-chip implementation in CMOS technology.

With frequency pushed into the millimeter-wave frequency region, such as 60 GHz, the lumped capacitor and inductor to build CRLH T-line structures are more compact and less lossy, and hence, feasible for on-chip implementation in the CMOS process. In this paper, the CRLH T-line-based zero phase shifter (ZPS) is studied for the first time during the on-chip PA design at 60 GHz. Detailed design considerations are studied for ZPS to achieve low loss and wideband performance for 60-GHz PA applications. With the use of a CRLH T-line-based ZPS, a novel 2-D power-combining topology is introduced by us in [19], which leverages both *serial power combining* from an SEDFDA and *parallel power combining* from a 0° power combiner. With ZPS implemented for the SEDFDA, it can be shown that both power and BW performance of the PA are improved with the minimum implementation expense such as area. The proposed 2-D power combining is implemented for one 60-GHz PA design using a UMC standard 65-nm CMOS process. Measured results show that the fabricated PA has 0.39-mm^2 area, 8.3-dB gain, 7.1% PAE, and 9.7-dBm P1 dB with 16-GHz BW (44–60 GHz).

This paper is organized as follows. Section II analyzes the SEDFDA's application for an on-chip 60-GHz PA, which defines the design specification for the need of ZPS. Section III then shows a detailed design of an on-chip CRLH T-line-based ZPS, which becomes the foundation of the proposed 2-D distributed power combining in Section IV. Section V provides detailed implementation for both ZPS and the according PA prototype at 60 GHz in a 65-nm CMOS, with measurement results presented in Section VI. This paper concludes in Section VII.

II. SEDFDA-Based PA Design

Both the DFDA and SEDFDA have been analyzed in [16] and [20], but targeted for PCB design at the gigahertz level, where T-lines are normally assumed ideal. For on-chip PA design at 60 GHz and beyond, T-lines are no longer ideal and the amplifier performance can be greatly affected. In the following, we present the design analysis background of the SEDFDA, and

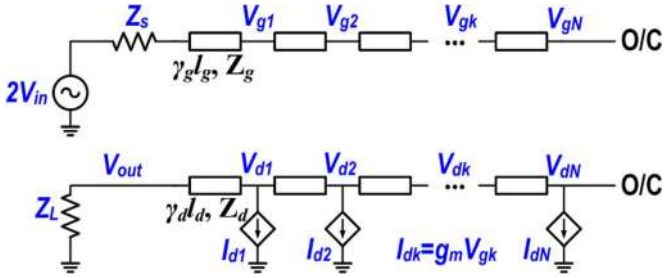

Fig. 2. Equivalent circuit for SEDFDA.

then show the design implications when considering the non-ideal T-line targeted for on-chip 60-GHz applications.

A. SEDFDA Performance Analysis Under Ideal T-Line Model

Fig. 2 shows the equivalent circuit for one N-stage SEDFDA. The upper half is the gate line and the lower half is the drain line. All parasitic components from transistors can be absorbed into the T-line model. Resulted T-lines for each section in both gate and drain paths are then characterized with characteristic impedance Z_g/Z_d, propagation constant γ_g/γ_d, and physical length l_g/l_d. The input impedance and load impedance are termed as Z_S and Z_LPerfect open circuits are assumed for terminations on both gate and drain lines. The input signal travels along the gate line, meets open-circuit termination, and is reflected back again. Forward and backward signals add up together to form transistor gate voltage V_{gk} (for the kth distributed stage), which controls the corresponding drain current I_{dk}. Assume $Z_S = Z_g$, gate voltages for all transistors can be calculated by directly adding the forward and backward voltages

$$V_{gk} = V_{\text{in}} \left[e^{-k\gamma_g l_g} + e^{(2N-k)\gamma_g l_g} \right]. \tag{1}$$

One special property for the DA is that transistor drain voltage (V_{dk}) is affected by all transistor drain currents. Assume $Z_L = Z_d$, with a similar method as [16], all drain voltages for the SEDFDA can be calculated

$$V_{dk} = \frac{g_m V_{\text{in}} Z_d (A1 + A2 + B1 + B2)}{1 + coth\left[(N-K)\gamma l_d\right]} \tag{2}$$

where $A1, A2, B1, B2$ are

$$\begin{aligned}
A1 &= e^{-k\gamma_g l_g} \times e^{-k(\gamma_d l_d - \gamma_g l_g)/2} \\
&\quad \times \frac{\sinh\left[(k-1)(\gamma_d l_d - \gamma_g l_g)/2\right]}{\sinh\left[(\gamma_d l_d - \gamma_g l_g/2)\right]} \\
A2 &= e^{-(2N-k)\gamma_g l_g} \times e^{-k(\gamma_d l_d + \gamma_g l_g)/2} \\
&\quad \times \frac{\sinh\left[(k-1)(\gamma_d l_d + \gamma_g l_g)/2\right]}{\sinh\left[(\gamma_d l_d + \gamma_g l_g/2)\right]} \\
B1 &= e^{-k\gamma_g l_g} \times e^{-(N-k)(\gamma_d l_d + \gamma_g l_g)/2} \\
&\quad \times \frac{\sinh\left[(N-k+1)(\gamma_d l_d - \gamma_g l_g)/2\right]}{\sinh\left[(\gamma_d l_d - \gamma_g l_g/2)\right]} \\
B2 &= e^{-(2N-k)\gamma_g l_g} \times e^{-(N-k)(\gamma_d l_d - \gamma_g l_g)/2} \\
&\quad \times \frac{\sinh\left[(N-k+1)(\gamma_d l_d - \gamma_g l_g)/2\right]}{\sinh\left[(\gamma_d l_d - \gamma_g l_g/2)\right]}.
\end{aligned}$$

The load line impedance for all transistors can then be obtained

$$Z_{dk} = \frac{V_{dk}}{I_{dk}} = \frac{V_{dk}}{g_m V g_k}. \tag{3}$$

If the same load line impedance can be maintained for all transistors, their power performance can be optimized simultaneously. For a lossless T-line, as in the case for the gigahertz region applications at the PCB level, it can be achieved by maintaining a same phase shift $\pm n\pi$ $(n = 0, 1, 2, \ldots)$ in both gate and drain lines

$$Z_{dk} = N Z_d \text{ when } \beta_d l_d = \beta_g l_g = \pm n\pi, \qquad n = 0, 1, 2, \ldots \tag{4}$$

where β_g and β_d are the phase constants for T-lines on gate and drain paths, respectively. In this case, all transistors can be fully utilized, and efficiency of the whole amplifier depends on that of each transistor. For example, for class-A amplifier design, the optimized efficiency can be achieved by implementing $Z_{dk} = (V_{\max} - V_{\min})/I_{\max}$, where $V_{\max}$ and $V_{\min}$ are the maximum and minimum output voltage for class-A operation and $I_{\max}$ is the maximum output current [16].

The improvement in efficiency can also be observed through the improvement in power gain. With (4) is satisfied, the power gain can be calculated as

$$\text{Gain} = \frac{P_{\text{out}}}{P_{\text{in}}} = 4N^2 g_m^2 Z_g Z_d \tag{5}$$

which is 16 times larger than the conventional DA with the same number (N) of transistors.

However, for on-chip DA design at 60 GHz and beyond, T-lines can no longer be assumed as ideal. Large parasitic components of the transistor, which are absorbed into the T-line design, further degrades its performance. Both loss (denoted in Section II-B) and phase error (denoted in Section II-C) on the T-line can severely degrade amplifier performance, and therefore should be taken into consideration with detailed analysis, as shown below.

B. Effect of T-Line Loss on SEDFDA

As frequency pushes up into the millimeter-wave region and the transistor size shrinks down to below 100 nm, and the lossy substrate, thin metal layer, and strong coupling between them severely degrades the quality factor of passive components. What is worse, the large and low-Q parasitics of transistor, which are absorbed into the T-line design, can severely degrade the effective Q factor of the T-line. For a practical on-chip amplifier such as PA design at 60 GHz, loss on the T-line must be taken into consideration.

Recall that (4) and (5) assumed an ideal T-line in both the gate and drain paths, i.e., $\alpha_d l_d = \alpha_g l_g = 0$, where α_g and α_d are the attenuation constants for T-lines on the gate and drain paths, respectively. For the practical on-chip design, α_g and α_d can no longer be assumed zero and are used to represent the loss on the T-line. As a result, the conclusion in (5) can be affected.

The impact of T-line loss to the SEDFDA design is further illustrated by one simulation example. Fig. 3 shows the impact of T-line loss on SEDFDA power gain. Here, g_m is assumed to be 20 mS and characteristic impedance on both gate and drain

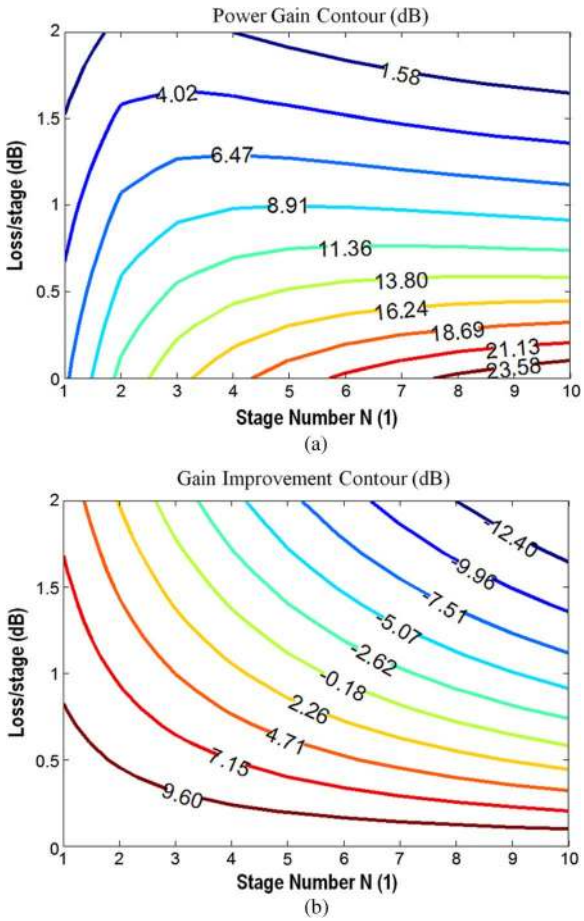

Fig. 3. Effect of T-line loss on SEDFDA performance.

lines are set as 50 Ω. Loss per distributed stage on the T-line are defined as $\alpha_g l_g$ $(\alpha_d l_d)$ and assumed identical on both the gate and drain paths. As Fig. 3(a) shows, loss on the T-line severely degrades the power gain in an exponential manner. For example, for a ten-stage SEDFDA, the power gain reduces from above 25 dB to below 0 dB as loss on the T-line increases from 0 to 2 dB/stage. It can also be observed that the impact of loss on power gain becomes more severe as the number of stages (N) increases. This can be understood that as N increases, the signal needs to propagate through more lossy stages to the output, and therefore, it experiences more degradation. As a result, there exists an optimum N for a specific value of loss in order to achieve the highest power gain. This optimum N decreases as loss per stage increases. In other words, loss on the T-line limits the maximum number of stages that can be implemented in the SEDFDA.

The advantage of the SEDFDA over the conventional DA is its improvement on power gain and efficiency. As (5) shows, an ideal SEDFDA can improve power gain by 12 dB, and improves the efficiency proportionally. However, as loss on the T-line increases, this advantage gradually diminishes. Fig. 3(b) shows the impact of T-line loss on the power gain improvement, which is calculated by dividing the obtained power gain to the power gain of a conventional DA with the same number of stages and with an ideal T-line. As shown in Fig. 3(b), in the high loss region, the gain ratio decreases below 0 dB. This effect again becomes more severe as N increases. In other words, loss on the T-line again limits the maximum number of stages (N) that can be implemented in the DA. For example, with loss of 2 dB per stage, the SEDFDA with a stage number above 2 can have no advantage over the conventional topology (with an ideal T-line) on power and efficiency performance.

Note that although identical loss is assumed on both gate and drain lines here for easy simulation, a similar conclusion can be drawn if divergent losses are used.

C. Effect of T-Line Phase Error on SEDFDA

As mentioned above, the performance of the SEDFDA is optimized when the phase shift in both gate and drain lines are identical and is equal to $\pm n\pi$ $(n = 0, 1, 2, \ldots)$. It is relatively easy to keep identical phase shift in the gate and drain line, but very difficult to maintain the phase shift to a fixed value. The major reason is that phase shift in the T-line is often frequency dependant. At 60 GHz and beyond, it is very expensive to implement phase compensation with extra circuits, and the large process variation further degrades the problem. Here we denote the difference between actual phase shift and target value as "phase error" and analyze its impact on the SEDFDA power performance.

Recall that to obtain the conclusions in (4) and (5), the phase-shift condition $\beta_d l_d = \beta_g l_g \pm n\pi$ $(n = 0, 1, 2, \ldots)$ must be satisfied, where β_g and β_d are the phase constants for T-lines. The identical phase shift $(\beta_d l_d = \beta_g l_g)$ is relatively easier to achieve and is assumed βl. Since we target a phase shift of $\pm n\pi$, the phase error can then be represented as $mod(\beta l, \pi)$.

Fig. 4 shows the resulted simulation result with the same parameters used as in Fig. 3. The phase error per stage is swept from $-20°$ to $+20°$. As Fig. 4 shows, the power gain degrades as phase error increases. Since phase error is normally proportional to frequency shift, this gain drop determines the BW of the SEDFDA. It also explains the tradeoff of SEDFDA BW over the conventional DA since the conventional topology only requires identical phase shift in gate and drain lines, and therefore has no such BW limitation.

It can be observed that again as the number of stages (N) increases, the power gain degradation by phase error becomes more severe. As a result, phase error on the T-line also limits the maximum number of stages that can be implemented in the SEDFDA.

III. ZPS BY CRLH T-LINE

As discussed in Section II, both loss and phase error of the T-line can degrade SEDFDA performance and also limit the number of stages (N) to be implemented. As will be shown in Section IV, the value of N affects the power-handling capability of the proposed PA topology when using the SEDFDA. A T-line that can achieve phase shift $\pm n\pi$ $(n = 0, 1, 2, \ldots)$ with low loss and small phase error is thereby required. Unfortunately, a 0° phase shift cannot be obtained in nature when using the traditional T-line since its phase shift is proportional to a nonzero length. As a result, a $\lambda/2$ T-line is used instead at the PCB level for SEDFDA design, which achieves a phase shift of 180°. When implemented on chip, this T-line is very bulky and lossy. What is more, its large phase shift (π) means a small percentage

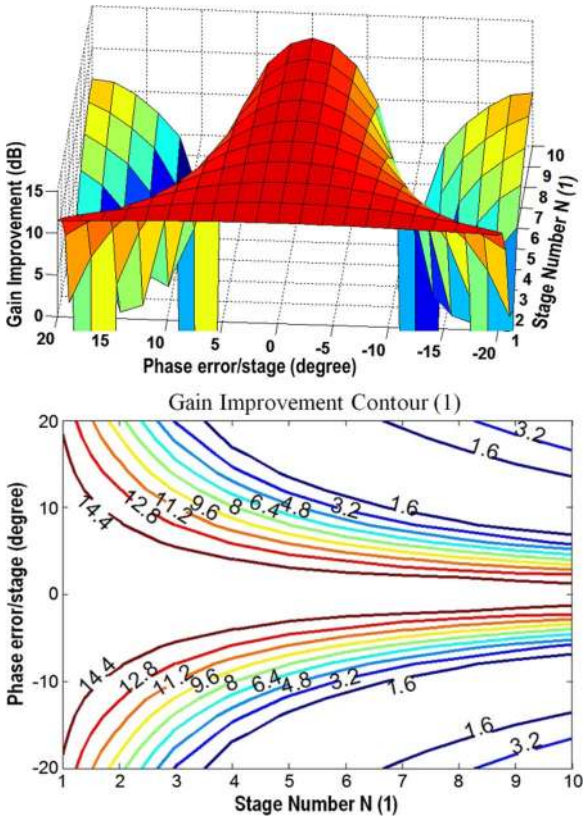

Fig. 4. Effect of T-line phase error on SEDFDA performance.

change can lead to a large phase error, which severely limits the BW. As a result, the traditional T-line approach is impractical for on-chip implementation of the SEDFDA. Alternatively, as frequency pushes to 60 GHz and beyond, those passive devices, which were too bulky to be implemented on chip at lower frequency, can now be designed with smaller value and more compact size for feasible on-chip applications. In Section III-A, a metamaterial-based T-line called the CRLH T-line is shown to be able to achieve a real zero phase shift. Design considerations for low loss and wideband implementation of the CRLH T-line based ZPS are then discussed for the SEDFDA based on chip PA design at 60 GHz.

A. CRLH T-Line Model

Metamaterial can be classified into two types: resonant type [21] and nonresonant type [22]. For applications that require wide BW, nonresonant type metamaterial is preferred [23]. Typically, it is realized as a left-handed T-line with capacitors connected in series (C_s) and inductors connected in parallel (L_p). However, due to the unavoidable parasitic, which are normally serial inductor (L_s) and parallel capacitor (C_p), the resulted T-line is actually a combination of the left-handed T-line and normal right-handed (RH) T-line, and therefore is called the CRLH T-line [22]. Due to the distributive nature of the T-line, the one-unit cell has the equivalent circuit as shown in Fig. 5(a).

The circuit can be viewed as two resonators connected together. L_s and C_s form the serial resonator, while L_p and C_p form the parallel resonator. Their impedance (admittance) can be represented as Z_s and Y_p, respectively. Here, all components (L_s, L_p, C_s, C_p) are normalized to unit cell length. According to T-line theory, the propagation constant (γ) and characteristic impedance (Z_0) can be calculated as

$$\begin{aligned}\gamma &= \alpha + j\beta \\ &= \sqrt{Z_s \times Y_p} \\ &= \sqrt{-\frac{\left[\left(\frac{\omega}{\omega_s}\right)^2 - 1\right] \times \left[\left(\frac{\omega}{\omega_p}\right)^2 - 1\right]}{\omega^2 \times L_p \times C_s}} \end{aligned} \tag{6}$$

$$\begin{aligned} Z_0 &= \sqrt{Z_s \div Y_p} \\ &= \sqrt{\frac{\left(\frac{\omega}{\omega_s}\right)^2 - 1}{\left(\frac{\omega}{\omega_p}\right)^2 - 1}} \times \frac{L_p}{C_s}. \end{aligned} \tag{7}$$

where ω_s and ω_p are resonant frequencies for serial and parallel resonators, respectively. In addition, α and β are the attenuation constant and phase constant.

From (6), we can see that if the signal frequency is between the two resonant frequencies

$$\alpha = \sqrt{-\frac{\left[\left(\frac{\omega}{\omega_s}\right)^2 - 1\right] \times \left[\left(\frac{\omega}{\omega_p}\right)^2 - 1\right]}{\omega^2 \times L_p \times C_s}} > 0, \qquad \beta = 0 \tag{8}$$

the signal does not propagate. The T-line operates in the bandgap region.

The relationship between β and frequency defines the dispersion diagram. Notice here a lossless system is assumed. If lossy components are introduced, β cannot stay 0 in the bandgap region, and α can never become 0.

An example for an ideal CRLH T-line unit cell is plotted in Fig. 5(b) with $L_s = 100$ pH $\cdot$ m^{-1}, $L_p = 100$ pH $\cdot$ m^{-1}, $C_s = 50$ fF $\cdot$ m^{-1}, and $C_p = 70$ fFm^{-1}. The dotted line displays attenuation constant α, and the solid line displays phase constant β. Notice β should be negative below the bandgap region, and is mirrored to the positive side for better observation. A negative (positive) phase constant is obtained in the left-hand (and RH) region, where signal propagates backward (forward). Two additional stopbands appear in the very low- and high-frequency regions due to the CRLH T-line unit cell's nature as a band pass filter.

B. Design of ZPS by CRLH T-Line

For applications in the 60-GHz or millimeter-wave region, the lumped capacitor and inductor to build a CRLH T-line structure are more compact and less lossy, and hence, feasible for on-chip implementation in the CMOS process. More importantly, the CRLH T-line can easily achieve the zero phase shift by combining the two phase shifts in opposite directions for: 1) the traditional RH T-line portion (L_s and C_p) and 2) the left-handed metamaterial portion (L_p and C_s). Since its phase shift does not depend on T-line physical length, a compact ZPS design can be achieved with low loss.

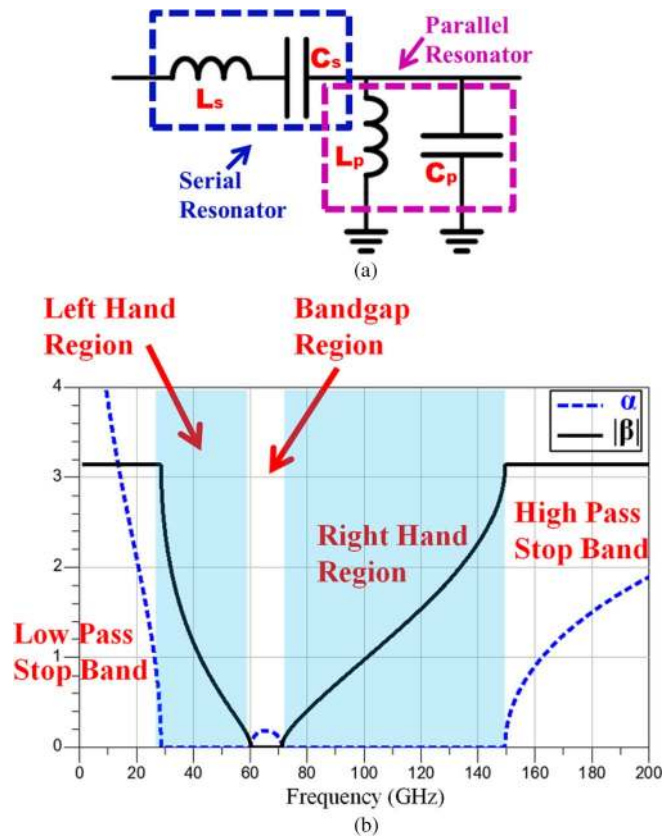

Fig. 5. CRLH T-line. (a) Equivalent circuit for T-line unit cell. (b) Operating regions.

An intuitive method to design a CRLH T-line-based ZPS is to bias the unit cell to operate in its bandgap region. According to (8), when the operating frequency is in the bandgap region ($\omega_s \leq \omega \leq \omega_p$ or $\omega_p \leq \omega \leq \omega_s$) the phase constant is equal to 0 ($\beta = 0$). In this case, signals passing through the CRLH T-line will not have any phase advance or delay. In other words, a zero phase shift is achieved. This condition, however, assumes the impedance matching from the port to T-line is always maintained. As (7) shows, the CRLH T-line's characteristic impedance (Z_0) is normally frequency dependant, which affects the matching for the whole SEDFDA, and therefore limits the actual BW that can be achieved for the zero phase-shift region. A simple solution is to design ω_s equal to ω_p. In this case, Z_0 becomes frequency independent and is only determined by L_p and C_s. Although the bandgap region in this case reduces to one frequency point, according to Fig. 4, as long as a small phase error is maintained, the SEDFDA still shows an advantage over a conventional DA. Actually, the frequency range within which the phase error causes gain degradation less than 3 dB determines the -3-dB BW. The design target thus becomes to maintain a small phase error within a wide frequency range. In other words, a small phase constant β within a wide frequency range is required.

On the other hand, in a practical T-line model, the attenuation constant takes all loss from parasitic into consideration and stays positive ($\alpha > 0$) in all regions. Therefore, to reduce T-line loss as required in Section II, α must be reduced as much as possible.

In summary, for the sake of a low-loss and wideband design of the SEDFDA, both the attenuation constant and phase constant need to be kept small. Equation (6) gives the relation $\alpha, \beta \propto \sqrt{1/L_p \times C_s}$. Although the formula is developed from a lossless system, the relation can be extended into a lossy system. As a result, a large parallel inductor (L_p) and a large serial capacitor (C_s) reduce both T-line loss and phase error. To maintain the same serial and parallel resonant frequencies, and thus the same operating frequency, a small parallel capacitor (C_p) and a small serial inductor (L_s) are required accordingly. In practice, C_p and L_s are realized by parasitic and wire connections to achieve maximized values for L_p and C_s.

IV. ZPS-Based 2-D Distributed Power Combining for PA

Since low output power/PAE and narrow BW are two primary design challenges for the CMOS PA at 60 GHz, this paper introduces a new power-combining topology that can simultaneously improve the PA's power efficiency and BW performance with the minimum implementation expense such as area. One straightforward approach is to merge power combining and distributed amplification together with a distributed topology to improve BW, and with power combining to improve power performance.

A. 2-D Distributed Power-Combining Topology

Since the design target is not for ultra-wideband solution, an SEDFDA topology is selected for distributed amplification with extra BW traded for better power performance. Multiple SEDFDAs are then combined together. 0° power-combining topology is selected for its simple structure and compact size. Moreover, the CRLH T-line-based ZPS is implemented in both the SEDFDA and 0° power combiner. In the SEDFDA, ZPS helps to optimize all transistors' power performance simultaneously, while in the 0° power combiner, the same ZPS provides better control of phase shift, and thus helps to fulfill the stringent phase requirement as mentioned in Section I with no extra layout expense caused.

The resulted topology is shown in Fig. 6. By using the CRLH T-line realized ZPS, a new 2-D distributed power-combining network can be constructed. The CRLH unit cell can replace the traditional $\lambda/2$ T-line for in-phase distributed amplification along the horizontal direction. The 0° power combiner can be also realized by the CRLH unit cell for 0° power combining along the vertical direction, where the distributed PA at last stage is combined. When considering the 0° combiner as a parallel combiner, and the distributed PA as a serial combiner, then the introduced circuit topology can be viewed as a 2-D distributed power-combining network for simultaneous distributed amplification and power combining. Such a topology can be further extended for phased-array applications by replacing the ZPS with an array of tunable phase shifters.

The proposed topology can simultaneously improve power and BW performance of the PA. For example, the PA power performance can be viewed from two aspects: output power per area (P_{out}/area) and output power per power consumption (PAE). The 2-D power-combining network provides a high density of transistor, and therefore improves P_{out}/area. The SEDFDA implemented with the CRLH T-line-based ZPS trades

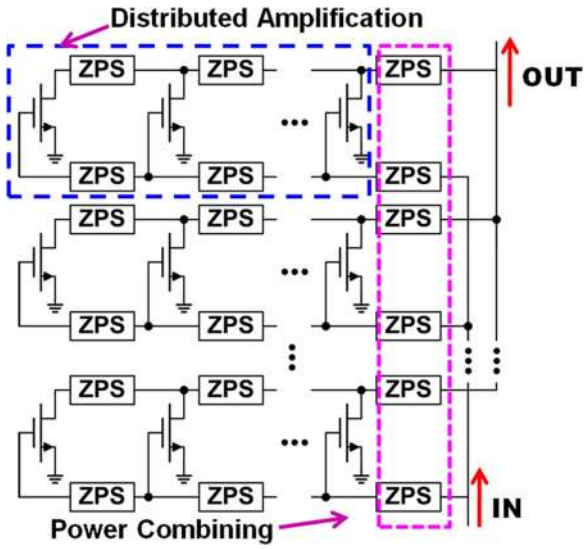

Fig. 6. SEDFDA PA topology based on 2-D distributed power-combining network with the use of CRLH ZPSs. [19].

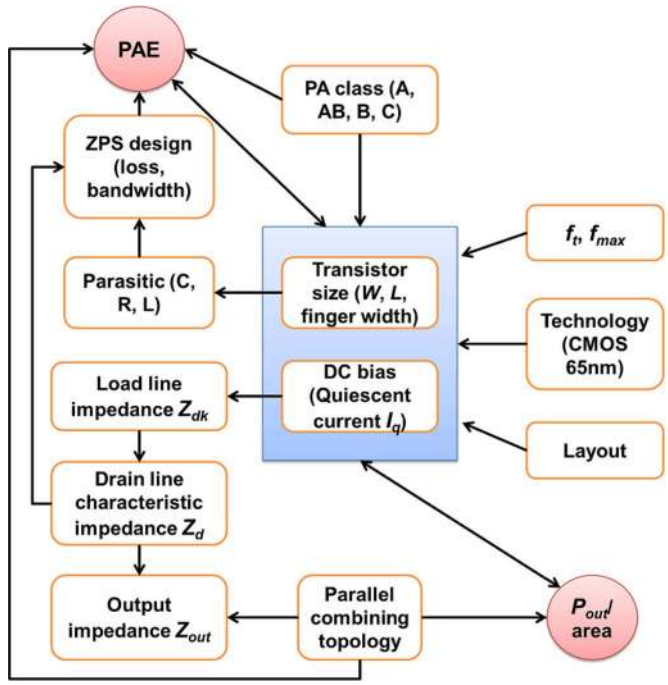

Fig. 7. Design consideration for the proposed 2-D distributed power-combining network.

extra BW with improved efficiency, thus improving PAE. As a result, the power performance can be improved together with BW performance.

Note that for a fixed transistor size, the total output power depends on distributed stages N and parallel combining branches M. Therefore, the power-handling ability of the proposed PA partially depends on distributed stage number N, which is limited by T-line loss and phase error, as mentioned in the Section II.

B. Design Optimization of ZPS-Based Power Combining

A detailed design consideration can be viewed in Fig. 7. With BW performance fulfilled with distributed nature of the proposed topology, the PAE and $P_{\rm out}$/area become two major targets during PA design. By knowing the application for the PA, the proper PA class can then be selected. Together with the selected technology, $f_t/f_{\rm max}$ optimization, PAE and $P_{\rm out}$/area requirement, and layout skills, the sizing and biasing of the transistors can be initially determined.

However, the interdependency between parameters calls for certain design iterations. There are mainly three considerations shown in the diagram that may require design iterations.

1) To improve the power density performance ($P_{\rm out}$/area), large size is preferred for transistors. However, large transistor size brings large parasitic components, which are the major contribution for L_s and C_p in ZPS design. As stated in Section III, this leads to small L_p and C_s to maintain the same operating frequency, which, in turn, causes high loss and narrow BW for the designed ZPS. As a result, the PAE is degraded. A compromise therefore needs to be made between $P_{\rm out}$/area and the PAE.
2) DC bias of transistors determines PA operating class. Both $P_{\rm out}$ and PAE performances for a single transistor is also determined by the bias. However, dc bias of transistors affects ZPS design through its optimized load line impedance. As shown in the diagram, given dc bias, for optimized performance of all transistors, the load line impedance (Z_{dk}) is determined, which, in turn, determines the characteristic impedance of the drain line (Z_d).
   As stated in Section III, $\omega_s = \omega_p$ is preferred for optimized ZPS performance, which leads to a characteristic impedance of $Z_o = \sqrt{L_p/C_s} = \sqrt{L_s/C_p}$ according to (7). However, the actual parasitic reactance from transistors (L_s' and C_p') is unlikely to follow the above relation for L_s and C_p. As a result, the size of L_s or C_p needs to be over-designed to generate wanted Z_d. Again, high loss and narrow BW are caused for the designed ZPS, which degrades the PAE performance. In summary, the PAE is affected by both transistor dc bias and ZPS performance, and a compromise needs to be made between these two parts.
3) The parallel combining topology not only affects $P_{\rm out}$/area and PAE performances directly through its efficiency, but also affects them indirectly through the output matching. As stated in (4), with a fixed load line impedance Z_{dk}, the characteristic impedance for the drain line is $Z_d = Z_{dk}/N$, where N is the distributed stages. Assuming M DAs are combined in parallel, the output impedance can be calculated as $Z_{\rm out} = Z_{dk}/(MN)$ if the Z_d for all DAs are combined in parallel, which is the case for 0° power combiner.
   Though the combiner has the benefit of merging part of the DA design into itself with reduced loss, a large combining network (large MN) may lead to very small output impedance and degrade the whole PA performance. In this case, other combining topologies, which can combine the Z_d for all DAs in serial, may be used, which generates output impedance of $Z_{\rm out} = MZ_{dk}/N$ instead, thus relaxing the stress on output matching. This is the case for DAT combiners.

In summary, selections and design iterations may be made to choose the most suitable power-combining topology. Note that

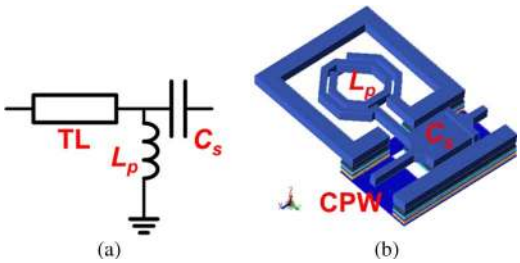

Fig. 8. CRLH T-line-based ZPS unit cell. (a) Schematic. (b) Layout.

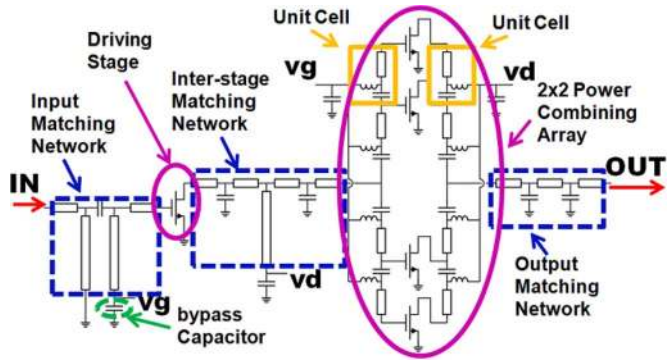

Fig. 9. Schematic of two-stage PA with a 2 × 2 distributed power-combining network [19].

a 0° power combiner is selected in both Fig. 6 and experiments for demonstration with a small 2 × 2 combining network.

V. 60-GHz PA Circuit With 2-D Distributed Power Combining

The ZPS unit cell and 60-GHz PA prototype with proposed 2-D distributed power combining are implemented in a UMC 65-nm logic and mixed-mode low leakage low-K CMOS process with six metal layers (one thick metal layer). The circuit is designed and verified by electromagnetic (EM) simulation (ADS Momentum) before fabrication.

A. ZPS Design

As shown in Fig. 8(a), a unit cell for the CRLH T-line can be constructed by combining a series capacitor (C_s) with a parallel inductor (L_p). The RH part of the CRLH T-line comes from the coplanar waveguide (CPW) T-line that connects unit cells, and parasitic capacitance between the unit cells and ground. Fig. 8(b) shows the layout version of this unit cell, where L_p is a spiral inductor formed by the top metal layer (M6). The thick metal ring around L_p serves as ground to improve isolation between unit cells and to form a better distribution of ground, as described in [24]. C_s is a metal–oxide–metal (MOM) capacitor constructed with multiple metal layers (M4–M6) in an inter-digit manner for better quality factor at 60-GHz range. Notice the two grounds of CPW are connected by metal 1 (M1) below, and the size of M1 can be adjusted to tune the total parallel capacitance to ground.

To characterize the performance of the CRLH T-line-based ZPS, one ZPS unit cell is fabricated along with a open-short-thru de-embedding structure. L_p is implemented with inductance of 220 pH and Q factor of 13.4 at 70 GHz. C_s is implemented with capacitance of 150 fF and Q factor of 19 at 70 GHz.

B. 60-GHz PA Design

With ZPS designed and characterized, the proposed 2-D distributed power-combining network is further implemented in a PA for demonstration. As shown in Fig. 9, a two-stage PA is designed with a single transistor in the first stage as driver; and a 2 × 2 distributed power-combining array in the second stage, which has two power-combining branches and each branch has a two-stage SEDFDA. All transistors are in single-ended common-source topology with transistor size of 64 × 1 μm/60 nm. With a biasing current of 22 mA, the simulated f_t is 172 GHz. The parasitic capacitances from transistor gate and drain are absorbed during the ZPS design to realize the distributed amplification. As a result, the shunt inductor (L_p) in Fig. 8(b) is resized to a single loop. Notice the size of L_s in the gate line is smaller than in the drain line due to a larger parasitic capacitance at the transistor gate.

The two power combiners implemented in the second stage only have two branches, mainly due to the limitation of the tape-out area. More branches can be used to enhance the power performance. Moreover, CPW T-lines are used as parallel inductors for matching and dc biasing at the same time, therefore no additional biasing circuit is required.

VI. Simulation and Measurement Results

Circuit simulation is done in both Cadence and ADS. The chip is measured on a CASCADE Microtech Elite-300 probe station and Agilent PNA-X (N5247A) with frequency sweep up to 110 GHz. Measurement for PA power performance is done at the center frequency (52 GHz) with pads de-embedded.

A. Results of CTLH T-Line-Based ZPS

The simulated and measured S-parameters for the CRLH T-line-based ZPS are shown in Fig. 10, and are compared with the measured results of the conventional $\lambda/2$ T-line. According to Fig. 10(a), the fabricated CRLH unit cell achieves a 30-GHz BW (57 ∼ 87 GHz) for a phase error less than 10°, which is four times wider than the 7-GHz BW (67 ∼ 74 GHz) for the $\lambda/2$ T-line. The measured results agree well with EM simulation with a frequency shift-down of 4 GHz. According to Fig. 10(b), the return loss is greater than 14 dB for the entire near-zero phase-shift region, indicating 50-Ω characteristic impedance. The worst case insertion loss is kept below 1.2 dB, which is three times smaller than the $\lambda/2$ T-line. There is a 0.8-dB deviation from EM simulation for insertion loss, which is due to inaccurate substrate parameters.

Moreover, measurement demonstrated a low-loss (<1.2 dB) wideband (30 GHz) performance for the proposed CRLH T-line-based ZPS, which proves the feasibility for metamaterial application for CMOS designs in the millimeter-wave region. Compared with the traditional $\lambda/2$ T-line, four times wider frequency band and three times less loss are achieved with 11 times reduction of physical length (86 μm).

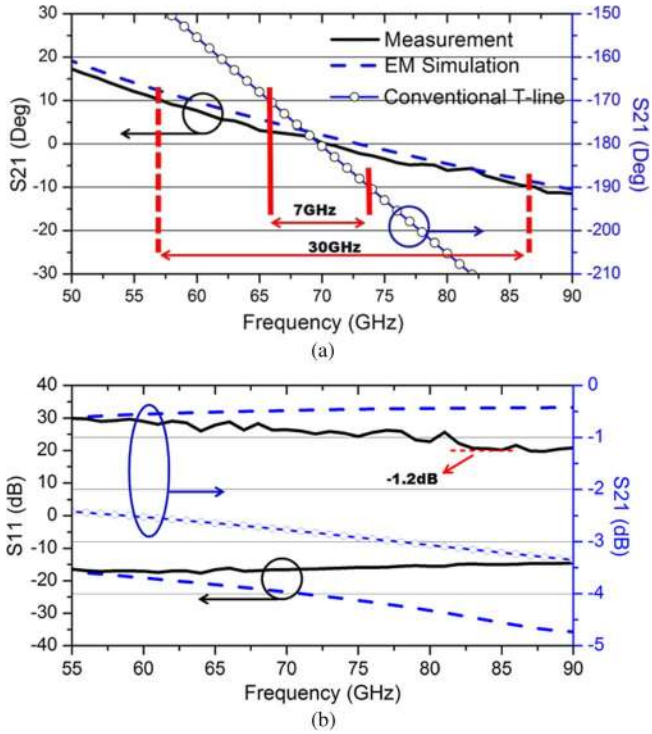

Fig. 10. Simulated and measured S-parameters for unit cell of CRLH T-line-based ZPS. Both: (a) phase and (b) loss performances are compared with measured results for conventional $\lambda/2$ T-line.

Note that to observe the left-handed property, its phase shift and effective phase constant can be obtained from S-parameters [25]. Following is the formula used:

$$\gamma \times p = \cosh^{-1}\left(\frac{1 - S11 \times S22 + S12 \times S21}{2 \times S21}\right) \qquad (9)$$

where p is the physical length of unit cell and $\gamma = \alpha + j\beta$ is the propagation constant. For this design, p is equal to 86 μm.

From Fig. 11(a), we can see $\beta \times p$ and phase of $S21$ overlap with each other, which is justified by that fact that phase shift of the unit cell is approximately equal to the product of phase velocity (β) and unit cell length (p) under impedance match. A small β within a wide frequency range therefore leads to a wideband performance.

The dispersion diagram is plotted in Fig. 11(b), where the phase constant β is obtained by dividing the phase shift $(\beta \times p)$ to unit cell physical length (p). Notice absolute value of β is taken for easier observation. A fall-down curve for $|\beta|$ is observed below the zero phase-shift region, indicating the left-handed region. Above the zero phase-shift region is the RH region, where β becomes positive and keeps rising. The low-pass stopband and high-pass stopband are located around dc and very high frequency, respectively, and are not shown in the plot.

B. Results of 60-GHz PA With 2-D Power Combining

Fig. 12 shows the simulated and measured S-parameters. An open-short de-embedding was performed to obtain the results. From simulation, the maximum gain is at 56.3 GHz with 11.3 dB. A 3-dB BW of 21 GHz is achieved (40.3 GHz

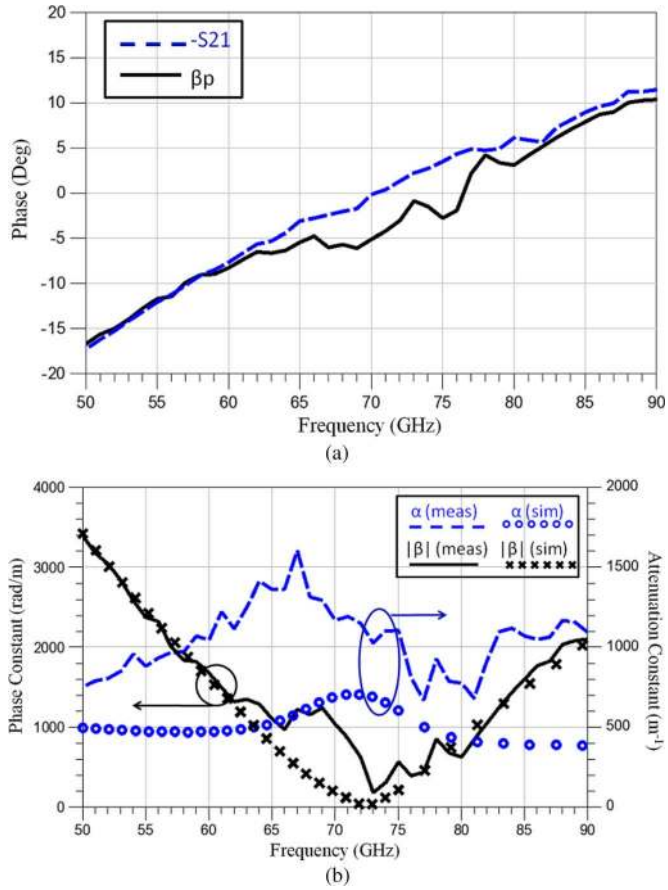

Fig. 11. Characterization of CRLH unit cell. (a) ZPS performance. (b) Propagation constant.

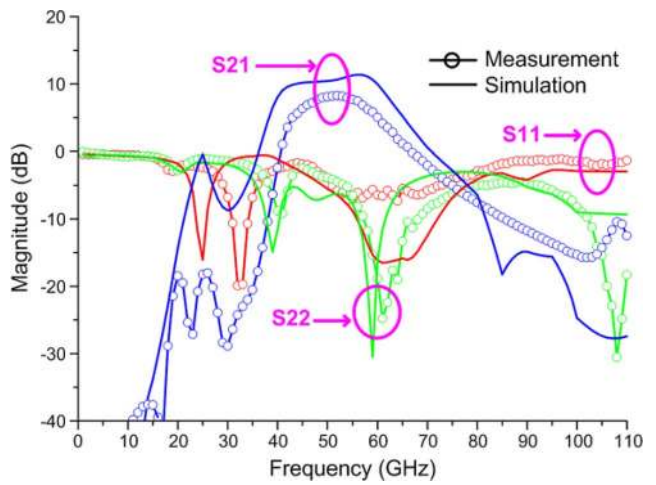

Fig. 12. Simulated and measured S-parameters of PA under 1.2-V supply [19].

$\sim$ 61.7 GHz). At 60 GHz, a 9.8-dB gain is obtained. The measured gain, on the other hand, has a peak value of 8.3 dB at 52 GHz. The 3-dB BW is 16 GHz (44–60 GHz). Compared with simulation, the center frequency is not shifted much, but power gain drops 3 dB and BW shrinks 5 GHz. Output matching confirms with the simulation while degradation occurs at the input matching. This input mismatch may be due to lack of device modeling, and can be used to justify the reduction of power gain.

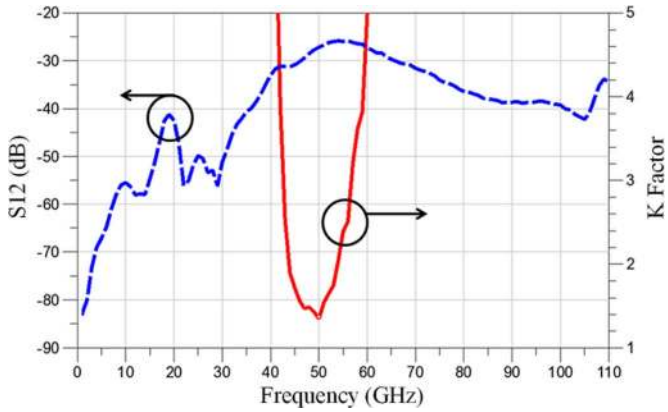

Fig. 13. Reverse isolation and stability of PA under 1.2-V supply.

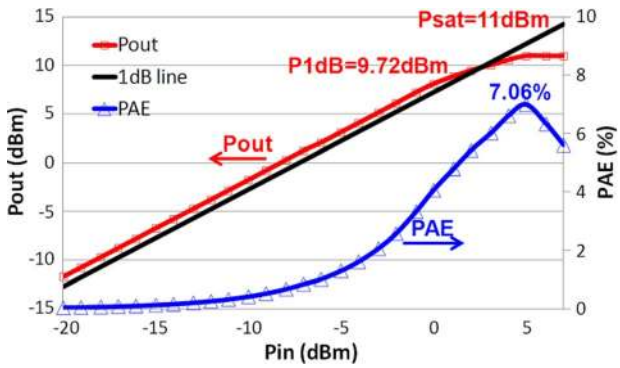

Fig. 14. Measured power and PAE of PA at 52 GHz under 1.2-V supply [19].

TABLE I
COMPARISON OF STATE-OF-ART TWO-STAGE 60-GHz CMOS PAs

	This Work	[3]	[4]	[5]	[6]
Tech. (CMOS)	65nm	65nm	45nm	90nm	90nm
Supply (V)	1.2	1.2	1.1	1	1
Gain (dB)	8.3	14.3	6	8.2	5.6
P1dB (dBm)	9.7	11	11	10.1	9
Psat (dBm)	11	16.6	13.8	11.6	12.3
PAE (%)	7.1	4.6	7	11.5	8.8
BW_{-3dB} (GHz)	16	15	19	13	22
Area (mm^2)	0.39	0.46*	0.06*	1.03	0.25

The measured reverse isolation and stability for the PA are shown in Fig. 13. The circuit is unconditionally stable from dc to 110 GHz, with reverse isolation better than −25 dB over the entire range. In addition, Fig. 14 shows the measured power performance at center frequency (52 GHz). With 1.2-V supply, P1 dB of 9.7 dBm and $P_{\rm sat}$ of 11 dBm are achieved. PAE drops to 7.1%. Note that both PAE and output power are limited by the number of power-combining branches and distributed stages, and can be further improved when a larger 2-D power-combining network is employed. Table I summarizes the presented work with comparison to the state-of-art two-stage CMOS PAs at 60 GHz. Comparison shows that the proposed PA can achieve the state-of-art performance for all figures of merit (FOMs).

Moreover, Fig. 15 shows the chip micrograph. Including pads, the PA occupies an area of 0.39 mm^2, which is quite compact when compared to the traditional design with the use

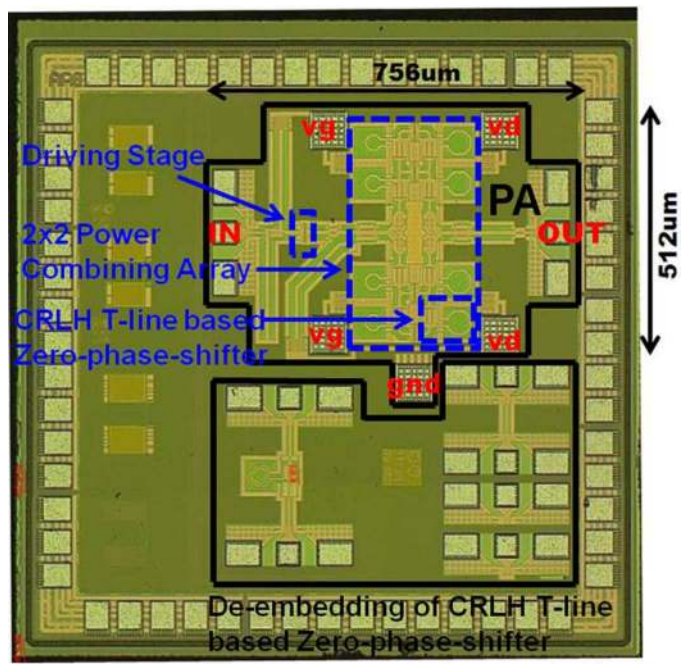

Fig. 15. Die micrograph with block illustrations [19].

of the T-line. Note that the upper part of the photograph is the 60-GHz PA with a 2 × 2 power-combining network. The lower part of the photograph is the de-embedding structures used to characterize the CRLH T-line-based ZPS.

In summary, the presented simulation and measurement results have demonstrated the feasibility of the proposed 2-D distributed power combining as well as the implementation of metamaterial in the millimeter-wave region by a 65-nm CMOS process.

VII. CONCLUSION

In this paper, one type of metamaterial, the CRLH T-line, has been utilized to design ZPS, and is further applied for on-chip PA design at 60 GHz in a 65-nm CMOS. Based on the detailed design consideration of ZPS and its application for distributed amplifier design (SEDFDA), a novel 2-D power-combining topology is introduced to leverage both serial power combining from an SEDFDA and also parallel power combining from a 0° power combiner. The new power-combining topology can provide distributed amplification and power combining simultaneously to improve output power and also to extend BW for a 60-GHz PA with the minimum implementation area. One PA prototype is fabricated in a UMC standard 65-nm CMOS process. Measurement results show 0.39 mm^2 area, 8.3-dB gain, 7.1% PAE, and 9.7-dBm P1 dB with 16-GHz BW (44–60 GHz), which demonstrates the feasibility of the proposed 2-D distributed power combining, as well as the implementation of metamaterial at the millimeter-wave region in a 65-nm CMOS process.

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REFERENCES

[1] A. Komijani and A. Hajimiri, "A wideband 77 GHz, 17.5 dBm power amplifier in silicon," in *Proc. IEEE CICC*, Sep. 2005, pp. 571–574.

[2] J. Chen and A. M. Niknejad, "A stage-scaled distributed power amplifier achieving 110 GHz bandwidth and 17.5 dBm peak output power," in *IEEE RFIC Symp.*, May 2010, pp. 347–350.

[3] B. Martineau, V. Knopik, A. Siligaris, F. Gianesello, and D. Belot, "A 53-to-68 GHz 18 dBm power amplifier with an 8-way combiner in standard 65 nm CMOS," in *Int. Solid-State Circuits Conf. Tech. Dig.*, Feb. 2010, pp. 428–429.

[4] K. Raczkowski, S. Thijs, W. De Raedt, B. Nauwelaers, and P. Wambacq, "50-to-67 GHz ESD-protected power amplifiers in digital 45 nm LP CMOS," in *Int. Solid-State Circuits Conf. Tech. Dig.*, Feb. 2009, vol. 383a, pp. 382–383.

[5] M. Bohsali and A. M. Niknejad, "Current combining 60 GHz CMOS power amplifiers," in *IEEE RFIC Symp.*, Jun. 2009, pp. 31–34.

[6] D. Chowdhury, P. Reynaert, and A. M. Niknejad, "A 60 GHz 1 V + 12.3 dBm transformer-coupled wideband PA in 90 nm CMOS," in *Int. Solid-State Circuits Conf. Tech. Dig.*, Feb. 2008, pp. 560–635.

[7] J. Kim, H. Dabag, P. Asbeck, and J. F. Buckwalter, "Q-band and W-band power amplifiers in 45-nm CMOS SOI," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 6, pp. 1870–1877, Jun. 2012.

[8] C. Y. Law and A. V. Pham, "A high-gain 60 GHz power amplifier with 20 dBm output power in 90 nm CMOS," in *Int. Solid-State Circuits Conf. Tech. Dig.*, Feb. 2010, pp. 426–427.

[9] N. Kurita and H. Kondoh, "60 GHz and 80 GHz wide band power amplifier MMICs in 90 nm CMOS technology," in *IEEE RFIC Symp.*, Jun. 2009, pp. 39–42.

[10] J. Chen and A. M. Niknejad, "A compact 1 V 18.6 dBm 60 GHz power amplifier in 65 nm CMOS," in *Int. Solid-State Circuits Conf. Tech. Dig.*, Feb. 2011, pp. 432–433.

[11] Y. He, L. Li, and P. Reynaert, "60 GHz power amplifier with distributed active transformer and local feedback," in *Proc. ESSCIRC*, Sep. 2010, pp. 314–317.

[12] Q. J. Gu, Z. Xu, and M. C. F. Chang, "Two-way current-combining W-band power amplifier in 65-nm CMOS," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 5, pp. 1365–1374, May 2012.

[13] Y.-N. Jen, J.-H. Tsai, T.-W. Huang, and H. Wang, "Design and analysis of a 55–71-GHz compact and broadband distributed active transformer power amplifier in 90-nm CMOS process," *IEEE Trans. Microw. Theory Techn.*, vol. 57, no. 7, pp. 1637–1646, Jul. 2009.

[14] E. Afshari, H. Bhat, X. Li, and A. Hajimiri, "Electrical funnel: A broadband signal combining method," in *Int. Solid-State Circuits Conf. Tech. Dig.*, Feb. 2006, pp. 751–760.

[15] C. S. Aitchison, N. Bukhari, C. Law, and N. Nazoa-Ruiz, "The dual-fed distributed amplifier," in *IEEE MTT-S Int. Microw. Symp. Dig.*, May 1988, vol. 2, pp. 911–914.

[16] F. Y. Ng-Molina, T. M. Martin-Guerrero, and C. Camacho-Penalosa, "Power and gain considerations in distributed amplifiers based on composite right/lefthanded transmission lines," in *IET Microw., Antennas, Propag.*, 2010, vol. 4, pp. 1000–1006.

[17] M. R. Moazzam and C. S. Aitchison, "A high gain dual-fed single stage distributed amplifier," in *IEEE MTT-S Int. Microw. Symp. Dig.*, May 1994, vol. 3, pp. 1409–1412.

[18] C. T. M. Wu, Y. Dong, J. S. Sun, and T. Itoh, "Ring-resonator-inspired power recycling scheme for gain-enhanced distributed amplifier-based CRLH-transmission line leaky wave antennas," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 4, pp. 1027–1037, Apr. 2012.

[19] W. Fei, H. Yu, K. S. Yeo, X. Liu, and W. M. Lim, "A 44-to-60 GHz, 9.7 dBm P1 dB, 7.1% PAE power amplifier with 2-D distributed power combining by metamaterial-based zero-phase-shifter in 65 nm CMOS," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2012.

[20] K. W. Eccleston, "Multiband power amplifier for multiband wireless applications," in *Proc. 3rd Int. Microw. Millim. Wave Technol. Conf.*, Aug. 2002, pp. 1142–1145.

[21] D. Cai, Y. Shang, H. Yu, and J. Ren, "80 GHz on-chip metamaterial resonator by differential transmission line loaded with split ring resonator," *Electron. Lett.*, vol. 48, pp. 1128–1130, Aug. 2012.

[22] A. Lai, T. Itoh, and C. Caloz, "Composite right/left-handed transmission line metamaterials," *IEEE Microw. Mag.*, vol. 5, pp. 34–50, Sep. 2004.

[23] T. J. Cui, D. R. Smith, and R. Liu, *Metamaterials: Theory, Design, Applications*. Berlin, Germany: Springer, 2009.

[24] M. Boers, "A 60 GHz transformer coupled amplifier in 65 nm digital CMOS," in *IEEE RFIC Symp.*, May 2010, pp. 343–346.

[25] J. Gao and L. Zhu, "Characterization of infinite- and finite-extent coplanar waveguide metamaterials with varied left- and right-handed passbands," *IEEE Microw. Wireless Compon. Lett.*, vol. 15, no. 11, pp. 805–807, Nov. 2005.

Wei Fei (S'10) received the B.S. degree in electrical and electronic engineering from Nanyang Technological University, Singapore, in 2007, and is currently working toward the Ph.D. degree in electrical and electronic engineering at Nanyang Technological University.

His research interest is emerging CMOS IC design at nanotera scale, including both nanoelectronics and terahertz monolithic microwave integrated circuits (MMICs).

Hao Yu (M'06) received the B.S. degree from Fudan University, Shanghai, China, in 1999, and the M.S. and Ph.D. degrees in electrical engineering (with a major in integrated circuit and embedded computing) from the University of California at Los Angeles (UCLA), in 2007.

He was a Senior Research Staff with Berkeley Design Automation (BDA). Since October 2009, he has been an Assistant Professor with the School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore. He has authored or coauthored 80 publications, two books, and four book chapters. His primary research interest is emerging CMOS technologies such as 3-D integrated circuit (3DIC) and RF integrated circuit (RFIC) designs at nanotera scale.

Dr. Yu is an associate editor and Technical Program Committee member of several journals and conferences. He was the recipient of the 2010 Best Paper Award of the *ACM Transactions on Design Automation of Electronic Systems* and the Inventor Award of the Semiconductor Research Cooperation (SRC). He also received Best Paper Award nominations in DAC'06, ICCAD'06, and ASP-DAC'12.

Yang Shang (S'11) received the B.S. and M.S. degrees in electrical and electronic engineering from Nanyang Technological University, Singapore, in 2005 and 2009, respectively, and is currently working toward the Ph.D. degree in electrical and electronics engineering at Nanyang Technological University.

His research interest is emerging CMOS IC design at nanotera scale, including both nanoelectronics and terahertz MMICs.

Kiat Seng Yeo (M'00–SM'09) received the B.Eng. in electrical engineering (with honors) and Ph.D. degree in electrical engineering from Nanyang Technological University (NTU), Singapore, in 1993 and 1996, respectively.

In 1996, he joined the School of Electrical and Electronic Engineering, NTU, as a Lecturer. He is a widely known authority on low-power IC design and a recognized expert in CMOS technology and RF IC design. As a result of his innovative pioneering research in the field of IC design, he has successfully attracted over S$30 million of external research funding from various funding agencies and the industry over the last three years. He is currently a Professor with the School of Electrical and Electronic Engineering and Founding Director

of VIRTUS, a new research centre of excellence jointly setup by NTU and the Singapore Economic Development Board. Since 1996, he has provided consultancy services to statutory boards, local SMEs, and multinational corporations in the areas of IC design. He was Sub-Dean (Student Affairs), Program Manager of the System-on-Chip flagship project, Research Coordinator of the Integrated Circuit Design Group and Principal Investigator of the Integrated Circuit Technology Group, NTU. He has authored or coauthored six books, three book chapters, and over 300 international top-tier refereed journal and conference papers in his area of research. He is Editor of *Advances of Internet of Things* and was one of the guest editors of the *Journal of Circuits, Systems and Computers on Green Integrated Circuits and Systems* (2008–2009). He holds 25 patents.

Dr Yeo is the Associate Chair of Research and a Board Member of the Singapore Semiconductor Industry Association (SSIA). He gave several keynotes and invited talks at various scientific conferences, meetings, workshops, and seminars. He serves in the Editorial Board of the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES. He also hold/held key positions in many international conferences as advisor, general chair, co-general chair and technical chair. He was the recipient of the Public Administration Medal (Bronze) on National Day 2009 by the President of Singapore and the distinguished Nanyang Alumni Award in 2009.