A 200 °C Universal Gate Driver Integrated Circuit for Extreme Environment Applications

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***Abstract*—High-temperature power converters (dc–dc, dc–ac, etc.) have enormous potential in extreme environment applications, including automotive, aerospace, geothermal, nuclear, and well logging. For successful realization of such high-temperature power conversion modules, the associated control electronics also need to perform at high temperature. This paper presents a silicon-on-insulator (SOI) based high-temperature gate driver integrated circuit (IC) incorporating an on-chip low-power temperature sensor and demonstrating an improved peak output current drive over our previously reported work. This driver IC has been primarily designed for automotive applications, where the underhood temperature can reach 200 °C. This new gate driver prototype has been designed and implemented in a 0.8 μm, 2-poly, and 3-metal bipolar CMOS–DMOS (Double-Diffused Metal-Oxide Semiconductor) on SOI process and has been successfully tested for up to 200 °C ambient temperature driving a SiC MOSFET and a SiC normally-ON JFET. The salient feature of the proposed universal gate driver is its ability to drive power switches over a wide range of gate turn-ON voltages such as MOSFET (0 to 20 V), normally-OFF JFET (−7 to 3 V), and normally-ON JFET (−20 to 0 V). The measured peak output current capability of the driver is around 5 A and is thus capable of driving several power switches connected in parallel. An ultralow-power on-chip temperature supervisory circuit has also been integrated into the die to safeguard the driver circuit against excessive die temperature (≥220 °C). This approach utilizes increased diode leakage current at higher temperature to monitor the die temperature. The power consumption of the proposed temperature sensor circuit is below 10 μW for operating temperature up to 200 °C.**

***Index Terms*—Gate driver, high-temperature, silicon-on-insulator (SOI), temperature sensor.**

I. Introduction

HIGH-TEMPERATURE power converters (dc–dc, dc–ac, etc.) have enormous potential in extreme environment applications, including automotive, aerospace, geothermal, nuclear, and well logging. For successful realization of such high-temperature power conversion modules, the associated control electronics also need to perform at high temperature. Operation of most ICs used in consumer electronics and industrial electrical systems is limited to a narrow operating temperature range of −55 °C to 125 °C. Fig. 1 shows the temperature ranges for different classes of commercially available ICs. Operation of electronics outside the traditional temperature range is typically defined as extreme temperature operation. This covers both the very low temperatures down to absolute zero (0 K) and high temperatures such as anything above +125 °C.

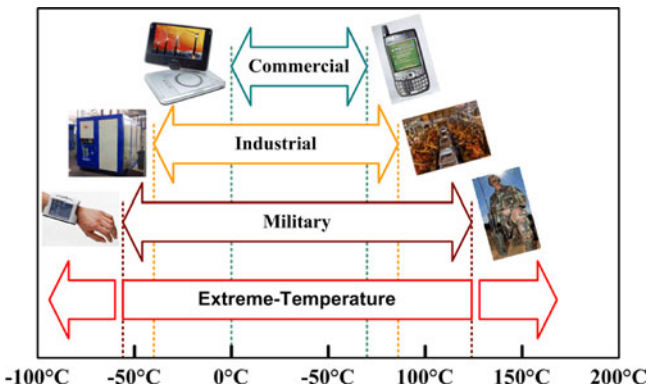

Fig. 1. Operating temperature ranges of semiconductor ICs.

Electronic devices and circuits are exposed to high temperature in a variety of applications under various environmental conditions. Integrated solid-state electronic circuits capable of operating at ambient temperatures higher than 150 °C without external cooling have tremendous potential in automotive, aerospace, and well-logging applications as well as in nuclear and geothermal power plants.

The automotive industry is often considered the primary and the largest near-term market for high-temperature electronics. The volatile nature of gasoline prices and the potential shortage of supply in the future are creating a growing demand for the development of hybrid electric vehicles (HEVs), plug-in HEVs (PHEVs), and all EVs to achieve better fuel efficiency compared to the traditional internal combustion engines [1]. Research and development in electric and HEVs have generated an enormous need for alternative power electronic modules (such as dc–dc converters and dc–ac inverters) for bidirectional power conversion between the energy storage units (battery or ultracapacitor) and the traction system [2]–[7].

Ambient temperature under the hood of an automobile is usually above 150 °C and can even reach 200 °C near the engine [8], [9]. The state-of-art HEV technologies require a separate 70 °C cooling loop for commercially available power

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TABLE I
PHYSICAL PROPERTIES OF TYPICAL SEMICONDUCTOR MATERIALS FOR POWER ELECTRONICS DEVICES

Property	Si	GaAs	4H-SiC	GaN
Bandgap (eV)	1.1	1.43	3.26	3.45
Saturation Electron Velocity (x 10^7 s^{-1})	1.0	1.0	2.0	2.2
Electron Mobility (cm^2/V-s)	1500	8500	1140	1250
Hole Mobility (cm^2/V-s)	600	400	50	850
Breakdown (x 10^5 V cm^{-1})	3	6	30	>10
Dielectric Constant	11.8	12.5	9.6	9
Thermal Conductivity (W cm^{-1} K^{-1})	1.5	0.46	4.9	1.3

electronic circuits which are mostly rated for 85 °C ambient temperature. The future goal of the automotive industry is to use the same 105 °C cooling loop that is used for the engine to cool the electronics under the hood. By removing the extra cooling unit and by reducing the size of the heat sink, an order of magnitude savings in overall mass and volume of the power electronic modules can be achieved. To minimize the cost and to improve the efficiency of HEVs, there is a pressing demand for miniaturization and weight reduction of the power converter modules. To achieve this goal, electronic circuits capable of operating at higher ambient temperatures (175 °C and above) with minimal thermal management are in great demand.

Presently, more than 98% of current electronic devices use silicon (Si) as the semiconductor material [9]. Si-based power devices currently dominate power electronics and power system applications. However, more and more power electronics applications are requiring high voltages, high switching frequencies, and high power densities as well as operating junction temperatures of the power devices in excess of 150 °C. Si-based devices are not capable of meeting these challenging requirements without expensive cooling systems, which increase the weight and volume of the power converters [10].

Table I lists physical properties of typical semiconductor materials [10], [11] for power electronics devices. The superior material properties of the wide bandgap (WBG) semiconductors (SiC and GaN) offer a lower intrinsic carrier concentration (10–35 orders of magnitude), a higher electric breakdown field (4–20 times), a higher thermal conductivity (3–13 times), and a higher saturated electron drift velocity (2–2.5 times) when compared to Si [10]. These properties make WBG semiconductors most effective in high-power and high-temperature applications. Among the WBG materials, SiC has emerged as an alternative semiconductor for overcoming the limitations of Si particularly in extreme environment conditions. SiC device operation at up to 500 °C has been reported in literature [12], whereas Si-based devices can only operate at a maximum junction temperature of 150 °C [12], [13]. Hence, the SiC-based power switches are expected to be the switch of choice for power electronic circuits in harsh environments where the ambient temperature can exceed 200 °C.

In all power electronic circuits including SiC-based power converters, a gate driver is an essential component to control the turning *ON* and *OFF* operations of the power switches. In a typical EV, the power converter modules along with the driver circuits are required to be placed under the hood. Hence, the ambient temperature of the electronics inside the power modules will be 150 °C or higher. Since SiC-based IC design technology is not commercially available, the solution for low or medium power needs and operating temperature up to 300 °C is silicon-on-insulator (SOI), which is commercially available for IC development [14]–[16].

Junction leakage is a major concern for bulk CMOS devices for high-temperature electronics applications which causes higher junction temperature compared to the ambient and can potentially lead to device failure. Si-based CMOS with reduced *OFF*-state leakage current for higher temperature operation can be realized using SOI structure. The buried insulator layer in the SOI structure greatly decreases the leakage path associated with the drain and the source p–n junctions. In SOI technology the leakage area of the junction is decreased by a factor of 100 compared to the bulk-CMOS process [14]. The buried oxide layer also reduces the OFF-state source-to-drain carrier emission leakage that physically occurs deeper in the substrate of the bulk MOSFETs. The threshold voltage variation with temperature is smaller in SOI devices compared to their bulk CMOS counterparts [16]. SOI also provides improved latch-up immunity, which ultimately increases the reliability of the circuit operation at higher temperature [16]. These features make SOI-based circuits capable of operating successfully in the 200–300 °C temperature range. For this paper, a process that combines the advantages of high-voltage DMOS and bipolar devices with SOI technology, known as bipolar CMOS–DMOS (BCD) process, has been chosen for the design and implementation of the high-temperature high-voltage gate driver circuit.

This paper presents an SOI-based high-temperature integrated gate driver circuit with large current drive capability. The proposed universal gate driver circuit demonstrates the capability to drive a SiC MOSFET as well as a normally ON SiC JFET. Circuit topology and operation along with test results of the earlier prototype of this SOI gate driver circuit were presented in [17], [18]. In this paper, an improved version of that gate driver circuit is discussed. The design focus of this iteration was to increase the current drive capability and the robustness of the circuit across a wide temperature range. An on-chip low-power temperature sensor circuit is also incorporated with the core gate driver circuit to safeguard it from excessive die temperature.

II. HIGH-TEMPERATURE HIGH-VOLTAGE GATE DRIVER IC WITH LARGE DRIVE CURRENT

A high-temperature commercial gate driver chipset called Themis & Atlas has been recently introduced by Cissoid (Mont-Saint-Guibert, Belgium), which is rated for −55 to 225 °C junction temperature. However, the peak output current of this driver IC is only 80 mA at 225 °C junction temperature. This paper presents the design of a high-temperature (≥200 °C) high-voltage (10 to 30 V) gate driver IC with high drive current (5 A) for WBG power switches. An earlier prototype of the proposed SOI-based high-temperature high-voltage gate driver circuit was

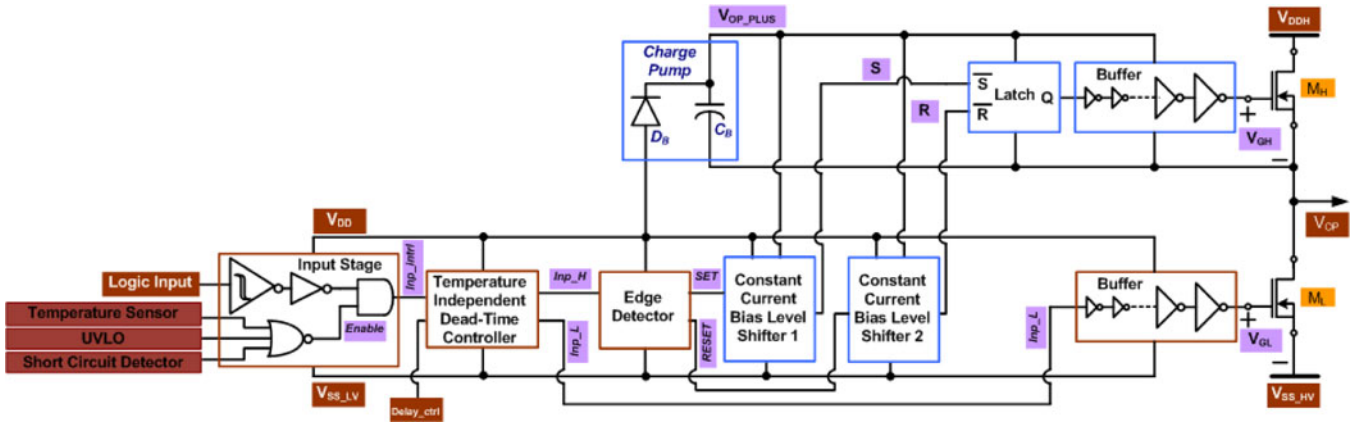

Fig. 2. Schematic of the high-temperature high-voltage gate driver circuit with high output current.

presented in [17] and [18]. The design focus of this iteration was to increase the current drive capability and make the critical functional blocks more robust across a wide temperature range. Several protective features including temperature-sensor-based thermal protection, undervoltage lock out (UVLO), and short-circuit protection have also been incorporated with the core gate driver circuit.

A block diagram level schematic of the gate driver circuit implemented in this design iteration is shown in Fig. 2. This circuit has seven critical building blocks, namely: 1) half-bridge high-voltage output stage (transistor pair M_H and M_L); 2) low- and high-side buffers; 3) on-chip bootstrap capacitor based charge pump; 4) constant current bias low- to high-side level shifters; 5) temperature-independent dead-time controller; 6) edge detection circuit; and 7) input stage. The input stage receives the logic control signal from the external source, which can be a microcontroller or a DSP board. Logic control units are expected to be placed in a relatively cooler space, isolated from the power modules. Often these signals are corrupted by noise.

In the SOI gate driver, a Schmitt trigger buffer in the input stage helps filter out this noise. The Schmitt trigger design used here has a 2.5 V hysteresis across a wide temperature range (−60 to 250 °C). This input stage also generates an *Enable* signal based on the feedback received from the protection circuits. If any one of the three feedback signals indicates a fault in the system, then the *Enable* signal will become zero, which will force the *inp_intrl* signal going to the dead-time controller circuit to a logic low state. This will make the gate driver output low and the power switch will be turned *OFF*.

The all n-type MOS (NMOS) (M_H and M_L) transistor-based half-bridge output stage handles the large drive current requirement of the driver circuit. A large number of 45 V n-type lateral DMOS (LDMOS) devices (each with aspect ratio of 40 μm/1.6 μm) transistors are connected in parallel to form both M_H and M_L switches within the gate driver. The current sourcing and sinking capabilities of this half-bridge stage are higher than 6 and 4 A at −50 °C and 200 °C, respectively. The bootstrap capacitor (C_B) based charge pump establishes a voltage (V_B) above the available highest rail voltage (V_{DDH}) for all the high-side devices and circuits.

The dead-time controller circuit generates two nonoverlapping copies (*inp_L* and *inp_H*) of the incoming logic signal (*inp_intrl*) with temperature-independent dead time injected between them, which ensures the complementary turn *ON* and *OFF* operations of the transistors in the output stage. An edge detector circuit generates two narrow pulses (*SET* and *RESET*) at the rising and the falling edges of the *inp_H* signal.

The level shifter provides conversion of the incoming narrow pulses (*SET* and *RESET*) from the low-side voltage level to the high-side voltage level. The *S* and *R* signals generated by the level shifter circuits are used to generate a voltage-level-shifted copy of *inp_H* using an *SR* latch circuit. The output of the latch circuit and the *inp_L* signals are passed through buffers to drive the relatively large capacitances at the gate terminals of the M_H and M_L transistors. Temperature-independent design of the dead-time controller and the level shifter circuit are discussed in Sections III and IV, respectively.

III. Temperature-Independent Dead-Time Controller

To reduce the power consumption of the chip and to ensure the reliability of the circuit, it is very important to maintain complementary turning *ON* and *OFF* operations of the high-voltage LDMOS transistors in the output stage. Overlapping turn-*ON* of both transistors will create a short circuit between the rail voltages (V_{DDH} and V_{SS}) resulting in large short circuit or crowbar current. This large current will increase the die temperature much above the ambient temperature. To ensure a break-before-make type operation, a temperature-independent dead-time controller circuit has been designed to generate two nonoverlapping copies of the *inp_intrl* logic signal. Fig. 3 shows the schematic of the proposed dead-time controller circuit. By applying logic high or low voltages to the *Delay_ctrl* terminal, the dead time between *inp_H* and *inp_L* can be adjusted.

The main building block of this circuit is the adjustable delay controller circuit that can inject a temperature-independent phase lag to an incoming logic signal. A temperature-independent current bias circuit has been designed to provide constant current biasing to the adjustable delay controller circuit. Fig. 4 shows the schematic of the temperature-independent current bias network developed using the zero-temperature

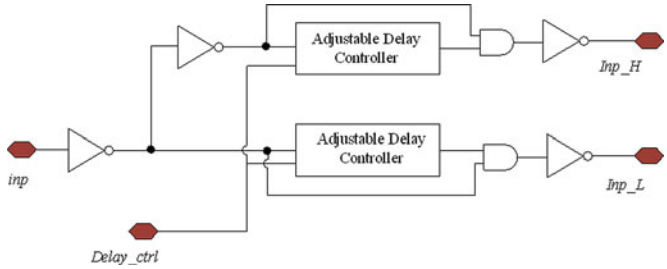

Fig. 3. Temperature-independent dead-time controller circuit.

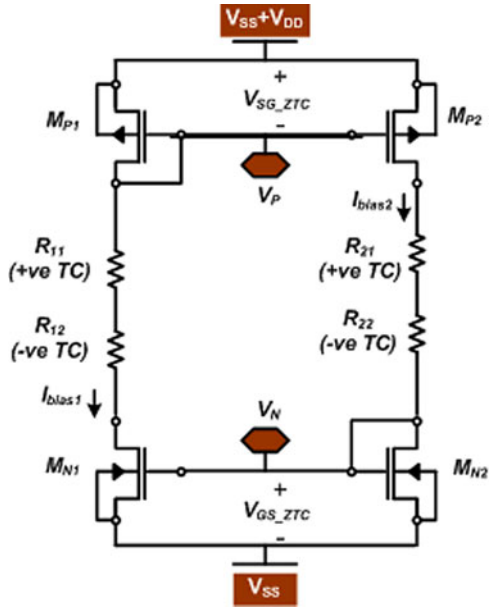

Fig. 4. Schematic of the temperature-independent current bias network.

coefficient (ZTC) [19] bias conditions of the NMOS and the p-type MOS (PMOS) transistors. The sizes of M_{P1} and M_{N1} transistors are selected such that their saturation drain–source currents at ZTC bias voltage $I_{\mathrm{DS\_ZTC}}$ become equal, i.e., $I_{\mathrm{bias1}} = I_{\mathrm{bias2}}$. Since the current through both the PMOS and the NMOS current mirror branches are equal, then the drain voltage of M_{N1} transistor tracks the $V_{\mathrm{GS\_ZTC}}$ voltage of M_{N2}. Similarly, the drain voltage of M_{P2} tracks $V_{\mathrm{SG\_ZTC}}$ of M_{P1}. The resistance value required to keep these transistors operating in saturation with the ZTC bias voltages is calculated by

$$R_{\mathrm{eq}} = R_{11} + R_{12} = R_{21} + R_{22} = \frac{(V_{\mathrm{DD}} - V_{\mathrm{SS}}) - V_{\mathrm{SG\_ZTC}} - V_{\mathrm{GS\_ZTC}}}{I_{\mathrm{DS\_ZTC}}}. \quad (1)$$

To minimize the net resistance variation with temperature, both positive and negative temperature coefficient resistors available in the SOI process were used. Using this circuit, the constant bias voltages V_P for PMOS and V_N for NMOS transistors are generated as shown below

$$V_P = V_{\mathrm{DD}} - V_{\mathrm{SG\_ZTC}} \quad \text{and} \quad V_N = V_{\mathrm{GS\_ZTC}} - V_{\mathrm{SS}}. \quad (2)$$

Fig. 5 shows the dc simulation of this bias network for temperatures ranging from -60 to 250 °C. Bias currents in both

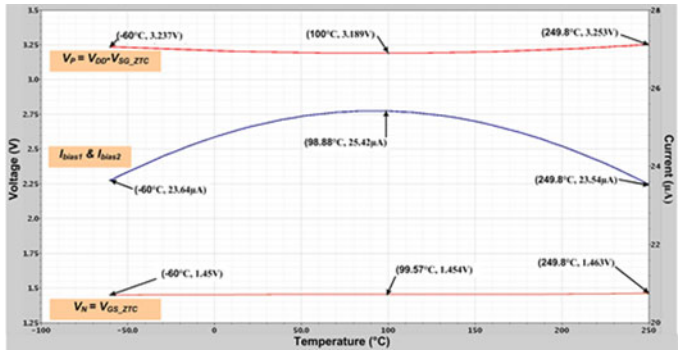

Fig. 5. DC simulation results of the temperature-independent bias network.

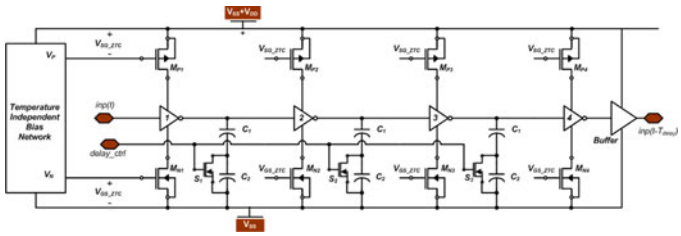

Fig. 6. Schematic of the temperature-independent adjustable delay controller circuit.

TABLE II
SIMULATION RESULTS OF DEAD TIME AT DIFFERENT TEMPERATURES

delay_ctrl	C_{eq} (*fF*)	Dead-time (ns)			
		-60°C	**100°C**	**175°C**	**250°C**
"High"	100	190	180	180	200
"Low"	50	110	110	110	140

branches are exactly the same and vary by less than 2 μA over the 310 °C temperature sweep. V_N and V_P voltages are almost constant across the temperature range. Fig. 6 shows the schematic of the adjustable delay controller circuit with the temperature-independent bias network. The constant bias voltage V_P is supplied to the gates of all the PMOS transistors, which source constant pull-up currents to the inverters, and thus the capacitors get charged by a constant current across the entire temperature range. Similarly, the constant bias voltage V_N is provided to all the NMOS transistors, which sink the constant pull-down current from the inverters. This ensures the same rate of discharge of the capacitors over temperature. The capacitors get charged and discharged by constant currents for the entire temperature range, hence, the phase shift injected by this circuit remains virtually constant over temperature. The dead times achieved between the nonoverlapping copies generated by the dead-time controller at different temperatures are shown in Table II. The aspect ratios of various transistors and the resistor values in the circuits described previously have been selected to accommodate required bias currents and operation modes of the transistors for optimization of the design for high-temperature operation.

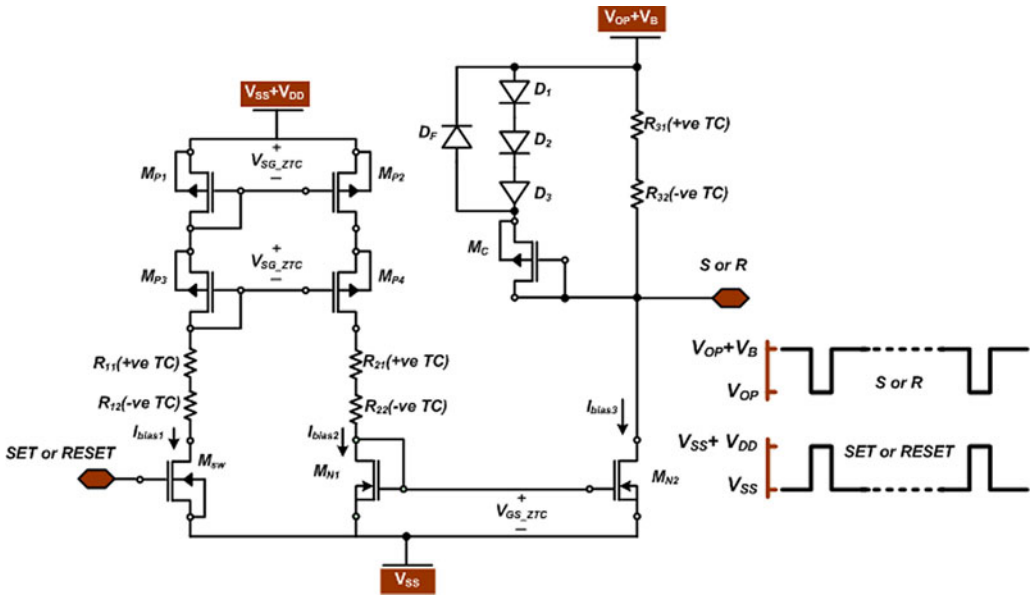

Fig. 7. Schematic of the temperature-independent level shifter circuit.

IV. Constant Current Bias Level Shifter Circuit

The level shifter circuit converts the logic level pulses (*SET* and *RESET*) into currents, and then in the high-voltage side converts this current back into a voltage signal referenced to the high-side voltage. For the all-NMOS LDMOS transistor-based half-bridge implemented in this paper, the level translation is from $(V_{\rm SS} - V_{\rm SS} + V_{\rm DD})$ to $(V_{\rm OP} - V_{\rm OP} + V_B)$. The source terminal of the M_H transistor is connected to the output terminal $(V_{\rm OP})$. Therefore, its gate voltage needs to be either at $V_{\rm OP}$ (to turn it OFF) or at $V_{\rm OP-PLUS} = V_{\rm OP} + V_B$ (to turn it ON). Two constant current bias level shifter circuits are used to generate *S* and *R* signals from the *SET* and *RESET* pulses, respectively, generated by the edge detector circuit.

Fig. 7 shows the schematic of the constant current bias level shifter circuit incorporated in this iteration of the gate driver circuit. The current $I_{\rm bias3}$ in the right-most branch creates a voltage drop across $(R_{31} + R_{32})$ that functions as the active low *SET* or *RESET* signal for the *SR* latch. If $I_{\rm bias3}$ varies with temperature, then the magnitude of the voltage drop will also vary. If the current is too low, then the voltage might not be sufficiently large to trigger the latch, and if it is too large, then this voltage drop may exceed the gate–source breakdown voltage limit of the MOS devices in the latch circuit. Hence, it is critical to maintain a constant current flow through this branch in response to the *SET* or *RESET* pulses.

This constant current bias is guaranteed through the ZTC biasing of the PMOS and the NMOS current mirrors, as shown in Fig. 7. The resistors in all three branches are constructed by a combination of positive and negative temperature coefficient resistors to ensure a fixed voltage drop across them over the entire temperature range of operation. This level shifter circuit consumes power only when the *SET* or *RESET* pulses are applied in the $M_{\rm SW}$ switch. The duty cycle of these pulses is only 0.04%. Therefore, the average power consumption of this circuit is very small. The diodes D_1 to D_3 and the transistor M_C work as a voltage clamping circuit to protect against transient voltage spikes across $(R_{31} + R_{32})$. The diode D_F is the freewheeling diode for the voltage clamp circuit.

V. Ultralow-Power Temperature Supervisory Circuit

An ultra low-power temperature supervisory circuit has been designed to protect the proposed high-temperature gate driver circuit. Most often on-chip temperature sensors use the base-emitter voltage difference between two substrate p–n–p transistors (thermal diode) of the same size, which are forward biased by two different dc currents, usually in the range of hundreds of microamperes [20]–[23]. One drawback of this approach is the continuous power loss even when the die temperature is in the normal operating range. These conventional approaches are also restricted to limited operating temperature range ($\leq$130 °C).

The temperature sensing scheme proposed in this paper utilizes the exponential increase in diode leakage current with the increase of temperature to determine the die temperature. Fig. 8 shows the measured and the simulated leakage current variation versus temperature plots for a p–n junction diode available in the BCD-on-SOI technology used in this paper. As this figure shows, the diode leakage current remains negligibly small until the die temperature reaches 150 °C, and beyond that it increases exponentially. Because of this temperature characteristic, the power consumption of the temperature sensor circuit is very low below 200 °C. The gate driver circuit developed in this paper is intended to operate up to 200 °C. For the typical operating temperature range of the gate driver circuit, the power consumption of the temperature sensor is minimal.

Fig. 9 shows the schematic of the proposed temperature sensor circuit. The core temperature sensing element of this circuit is the reverse-biased diode $D_{\rm sense}$. Several (*M* number) p–n junction diodes are connected in parallel to increase the total leakage current, which depends on the die temperature. The diode leakage current, which is typically in the nanoampere (nA) range,

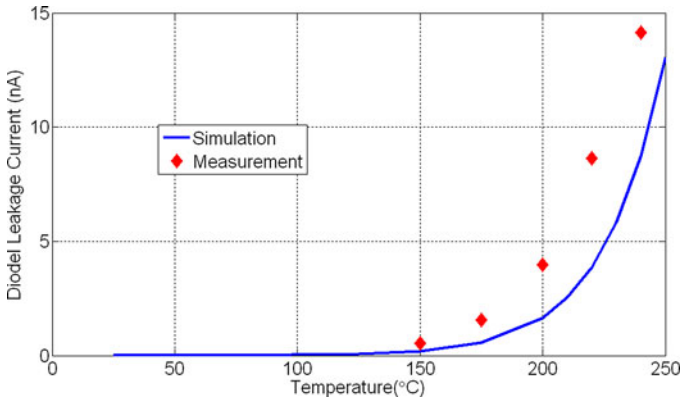

Fig. 8. Measured and simulated p–n junction leakage current as a function of temperature.

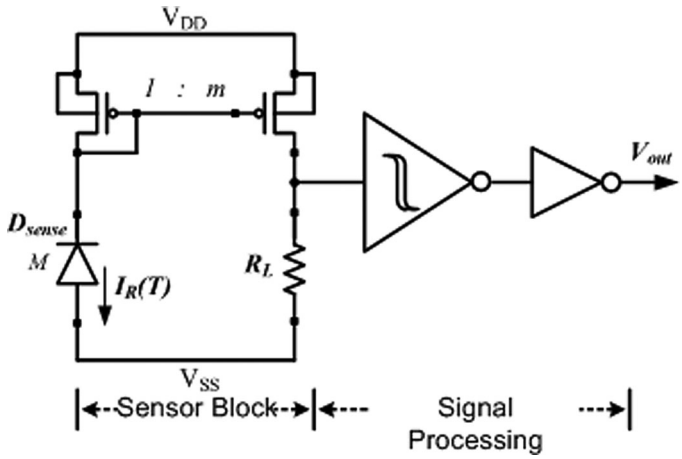

Fig. 9. Schematic of the proposed low-power on-chip temperature sensor circuit.

is first multiplied by the PMOS current mirror with 1:30 ratio and then converted to a voltage signal by the resistor R_L. The voltage drop across the resistor R_L is applied to the input of a Schmitt trigger which is buffered using a digital inverter circuit to drive the output node. With the increase in die temperature, voltage drop across R_L goes high, and once it exceeds the low-to-high threshold voltage of the Schmitt trigger $V_{\rm out}$ transitions to a logic high ($V_{\rm DD}$) indicating a fault condition. This feedback signal is sent to the input stage of the gate driver circuit. The high-to-low threshold voltage of the Schmitt trigger is set at a lower value corresponding to a 15 °C reduction in die temperature. This hysteresis will prevent the circuit from being inappropriately triggered by a temporary recovery of the fault condition.

VI. Experimental Results

The proposed high-temperature gate driver circuit has been designed and implemented in a 0.8 μm BCD on SOI process. The gate driver circuit, including the on-chip temperature sensor, occupies an approximate area of 10 mm^2 (4050 μm $\times$ 2600 μm) including the bonding pads and the electrostatic discharge protection circuits. Fig. 10 shows the layout of the core gate driver

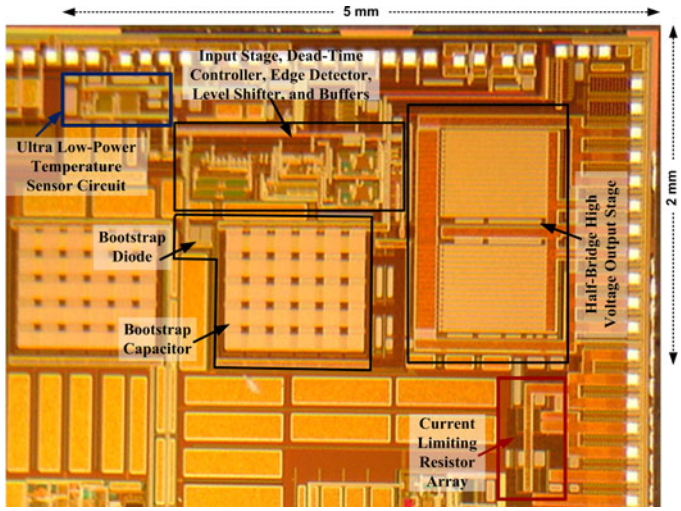

Fig. 10. Microphotograph of the gate driver and temperature sensor circuits.

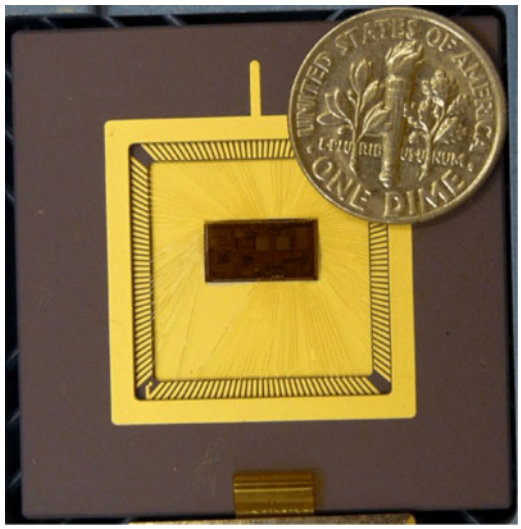

Fig. 11. Packaged high-temperature gate driver IC.

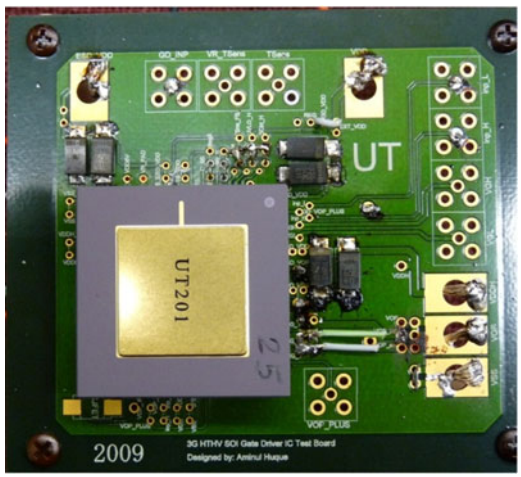

Fig. 12. High-temperature test board made of polyimide.

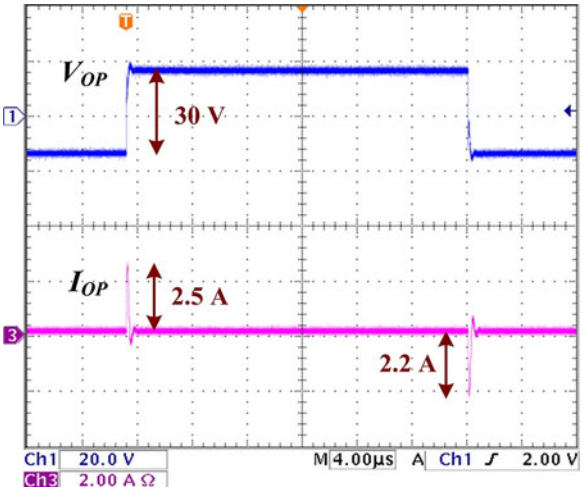

Fig. 13. *RC* load test results at 200 °C.

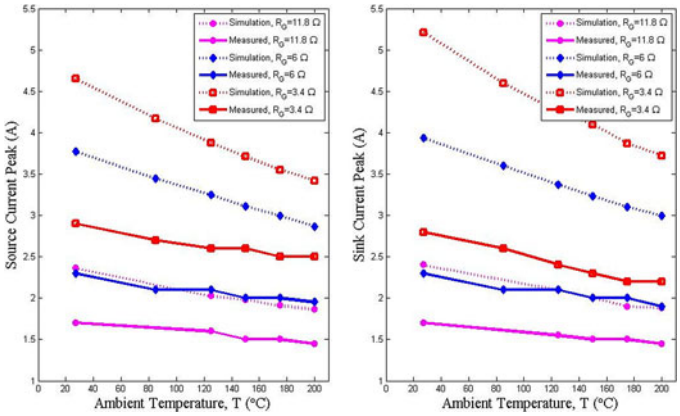

Fig. 14. *RC* load simulation and measured peak drive currents (sourcing and sinking) with three different on-chip current-limiting resistance (R_G) values.

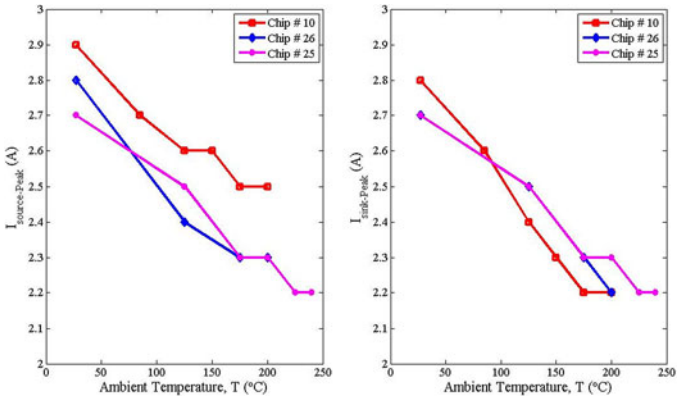

Fig. 15. Measured source and sink current peaks at different ambient temperatures for three different ICs with the same *RC* load (R_G = 3.4 Ω and C = 10 nF).

circuit and the on-chip temperature sensor. This is part of a larger die, which also includes several voltage regulators, UVLO, and short-circuit protection unit. Fig. 11 shows the packaged gate driver IC. A high-temperature test board made using ployimide was developed for testing of the gate driver prototype, as shown in Fig. 12.

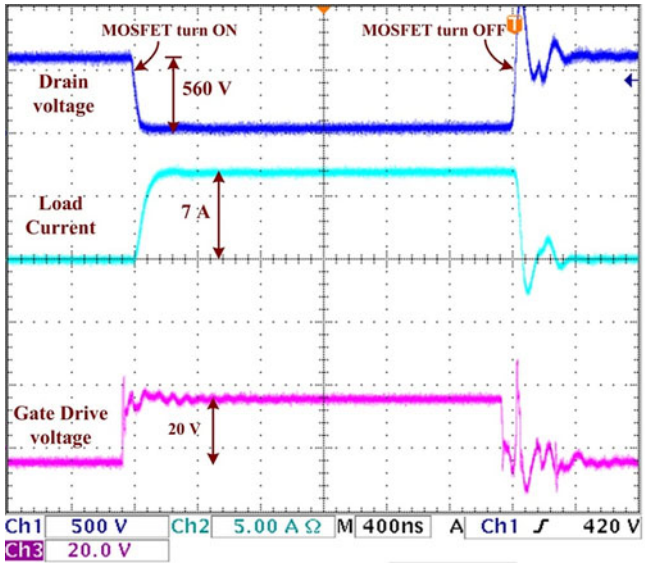

Fig. 16. MOSFET measurement results at 200 °C with 1200 V, 10-A SiC MOSFET operating at a switching frequency of 20 kHz

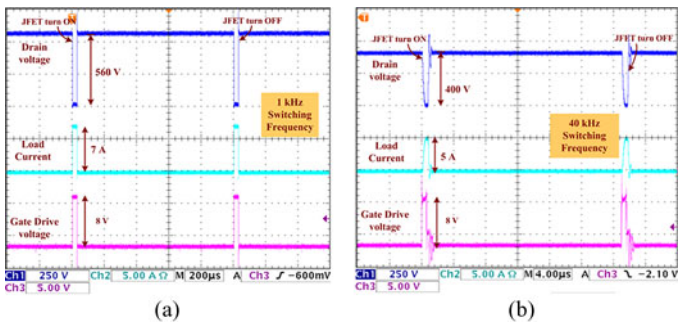

Fig. 17. SiC normally-ON JFET module (1200 V, 50 A) test results at 200 °C ambient temperature: (a) 1 kHz and (b) 40 kHz switching frequency.

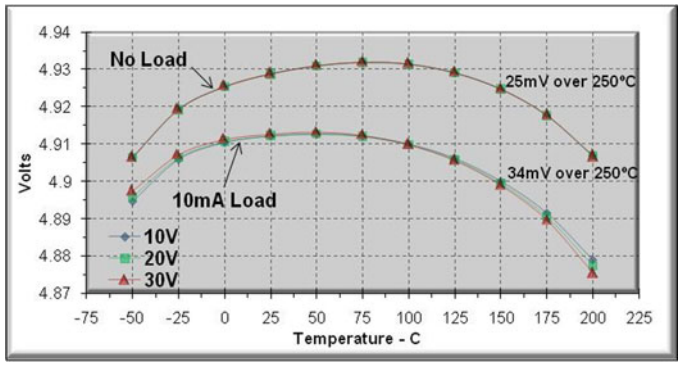

Fig. 18. Temperature characteristics of the 5 V voltage regulator.

Extensive characterization of this improved gate driver circuit has also been carried out with SiC power switches at and above 200 °C. For the first set of measurements, an on-chip current-limiting resistor R_G was connected in series with an external 10-nF capacitive load to model the load presented by a power switch. Fig. 13 shows the 30 V_{p-p} (−15 to +15 V), 20 kHz gate pulse signal generated by the chip at an ambient temperature of 200 °C with a nominal R_G value of 3.4 Ω. At 200 °C, the

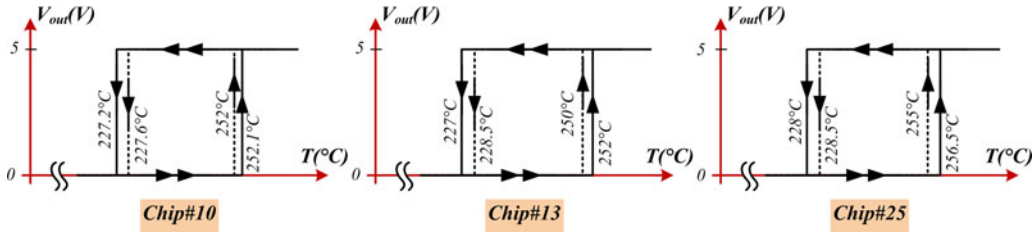

Fig. 19. Output voltages of the temperature sensor circuit in response to several cycles of temperature rise and drop (for $M = 30$).

peak sourcing and sinking currents were measured to be 2.5 and 2.2 A, respectively. A similar *RC* load test was carried out for three different on-chip current-limiting resistance (R_G) values. Fig. 14 presents the change in source and sink current peaks with temperature variation for all three R_G values. Fig. 14 also shows the simulation results for similar load conditions. Differences between the measured and simulated results are still under investigation. Self-heating effects within the on-chip SOI high-voltage transistors of the output stage of the gate driver may be constraining the measured current drive. The modeling of self-heating effects may not be sufficient for simulation. Fig. 15 presents the measured source and sink current peaks at different ambient temperatures for three different ICs with same *RC* load ($R_G = 3.4\ \Omega$ and $C = 10$ nF). Small chip-to-chip variations in drive current were observed.

A SiC power MOSFET (1200 V, 10 A) prototype device was also tested with the gate driver, as shown in Fig. 16. The SiC MOSFET was arranged in a common-source configuration with an 80 Ω, 250 W load resistor in series with the drain terminal. The drain voltage of the MOSFET was set at 560 V using a 600 V, 16 A dc power supply. A 20 V_{p-p} (+15 to −5 V) drive signal was applied to the gate terminal of the SiC MOSFET through the 3.4 Ω, on-chip current-limiting resistor (R_G). The switching frequency was 20 kHz with a duty cycle of 5%. The chip was tested from room temperature up to 200 °C ambient.

The gate driver IC was also tested with a normally-ON SiC JFET (1200 V, 50 A) power module. The gate driver circuit was biased to generate an 8 V_{p-p} (−5 to 3 V) gate signal to control the JFET module that was connected to a 560 V rail voltage through an 80 Ω load resistor. Fig. 17 shows the test result at 200 °C ambient temperature with 1 and 40 kHz switching frequencies. The proposed gate driver featured a 5 V regulator, which requires an external output capacitor to provide a stable output voltage for gate driver circuits. Fig. 18 shows the temperature characteristic test data of the 5 V voltage regulator.

To test the functionality of the newly proposed temperature sensor, the test board was placed inside an environmental chamber. The circuit was properly biased and the output ($V_{\rm out}$) was observed on an oscilloscope. In the beginning of the test, at room temperature, $V_{\rm out}$ was set at logic low (0 V) level. The temperature of the chamber was then raised until a logic transition from low-to-high was observed in the $V_{\rm out}$ signal. The temperature at which this transition took place is the upper limit of the allowed die temperature at which this sensor circuit will send a feedback signal to the input of the gate driver circuit indicating a fault condition. After recording this upper temperature limit, the chamber temperature was reduced until a logic high-to-low transition was observed in the $V_{\rm out}$ wave shape in the oscilloscope. This high-to-low transition took place at much lower temperature than the temperature at which the low-to-high transition was observed. This temperature difference indicates the built-in hysteresis of the sensor circuit. The high-to-low transition in $V_{\rm out}$ indicates the removal of the fault condition, which was causing the excessive rise in the die temperature. Upon receiving this low signal from the sensor circuit, the gate driver will resume its normal operation. Hence, a built-in hysteresis is very critical to ensure proper removal of the fault situation causing the die temperature to rise beyond its normal operating range.

Several temperature rise and drop cycles were carried out to measure the upper and the lower triggering temperatures of the sensor circuit. These tests were repeated for three different chips to observe the repeatability of the circuit performance. Fig. 19 shows the results of these temperature cycle tests for different chips. The worst case spread in fault triggering temperatures (2.5 °C) and the worst case spread in the fault removal temperatures (1.5 °C) were both observed for chip#13. For all three chips, the measured hysteresis was around 25 °C.

VII. Conclusion and Future Work

The proposed SOI gate driver circuit has demonstrated current drive capabilities of 6 and 4 A at −50 °C and 200 °C, respectively. The large current drive is necessary to drive the power switches with large current ratings. Often several power switches are connected in parallel to boost the current handling capability of the system, which also requires large drive current from the gate driver circuit. Simulation results indicate that the proposed driver circuit can drive a 10-nF capacitive load in less than 50 ns and 70 ns at −50 °C and 200 °C, respectively. The switching frequency of the driver can reach 500 kHz, which will help reduce the required size of the power converter modules by reducing the size of the filtering elements.

Monte Carlo simulation across the wide temperature range (−50 to 250 °C) shows very little variation in the circuit performance of the gate driver. The on-chip low-power temperature sensor circuit incorporated in the chip to safeguard the gate driver consumes very little power up to 200 °C temperature. For efficient and effective integration of WBG power devices into power electronic modules, the control circuits need to be interfaced with SOI-based ICs capable of working above the ambient temperature of 200 °C. The improved high-temperature

and high-voltage gate driver circuit presented in this paper is part of an ongoing research effort to design a heatsink-less, air-cooled dc–dc converter and a three-phase inverter that can be placed under the hood of hybrid or plug-in HEVs. Test results involving MOSFET and normally-ON JFET demonstrate the universal driving capability of the proposed gate driver circuit. Although this gate driver circuit has primarily been designed for automotive applications, this could easily be incorporated into any power electronic module developed for harsh environment applications, where conventional bulk Si-based circuits cannot deliver efficient and reliable solutions.

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