

T H E U N I V E R S I T Y O F M I C H I G A N

Memorandum 15

A 201A DATA COMMUNICATION ADAPTOR FOR THE PDP-8:
PRELIMINARY ENGINEERING DESIGN REPORT

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A 201A DATA COMMUNICATION ADAPTOR FOR THE PDP-8:
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INTRODUCTION

This report discusses the design and use of equipment built for data communication to and from the PDP-8 through a 201A data set. The purpose of the data communication interface is to allow a PDP-8 to send and receive digital data through a 201A data set in a half-duplex mode. The 201A data set operates serially at a rate of 2000 bits per second, with the transmit clocks supplied by the data set. In the receive mode, the data set achieves bit synchronization, and provides a receive clocking signal to the interface. The interface provides the character synchronization at the start of a message and then transfers successive characters in parallel to the PDP-8. The interface stores and retrieves characters from the PDP-8 memory through the data-break facility, while achieving control communication with the PDP-8 through the interrupt and programmed data transfer modes.

This report will serve as a progress report for those interested in technical progress on the project, and as a rudimentary maintenance manual for those responsible for system maintenance in the future. Basic design objectives and decisions will be described first. A brief overall system description together with a sketch of a data format scheme and programming considerations will be followed by a detailed description of the interface logic.

DESIGN OBJECTIVES

In order to obtain a flexible interface the following design objectives were set forth:

1. Rigid interrupt discipline.
2. Minimal program interaction required during message transmission.
3. Variable character length and vertical parity calculation under program control.
4. Maximal interface status and control available upon request.
5. Hardware implementation of character synchronization using the ASCII SYN character.

In order to minimize the amount of code in an interrupt processor for the 201A communication interface, the interface was carefully designed to give interrupts only and always when a character was received or transmitted. The desire to give the maximum time between interrupts at the minimal hardware cost led to a decision to use core buffers in the PDP-8 through the use of the data-break facility. This decision was also made in light of the fact that several of these interfaces were to be used on the Data Concentrator. A separate design using a hardware buffer without using the data-break facility is shown in Appendix III.

The expected mode of operation of the interface utilizes an 8-bit character without vertical parity. Experimental evidence during the past year has indicated that vertical parity, at least on local hook-ups, is not needed. The decision to use an 8-bit character was strongly influenced by ASCII conventions and the fact that the central computing facility uses an 8-bit byte IBM/360 model 67 computer.

The interface depends on the PDP-8 only to the extent that characters must be removed or placed in the core buffers,

and the interrupt processed within a character time for error-free transmission. However, complete control and status presentation is available from the interface if desired, to the extent that the 201A data set will allow.

SYSTEM DESCRIPTION

The four sections of the equipment for one end of a data communication link are shown in Figure 1: the PDP-8, the PDP-8/201A line adaptor interface, the 201A line adaptor, and the 201A modem. The PDP-8 and the 201A modem will not be discussed here. This report is concerned with the design of the line adaptor and the line adaptor interface.

The distinction between the line adaptor and its interface is in some instances arbitrary. In general, however, the term line adaptor refers to that portion which is common to the three variations of the 201A data communications adaptor described in this report. The three variations which will be presented are: the basic PDP-8 adaptor, the PDP-8 adaptor which does not use data break, and the 201A line adaptors on the Data Concentrator. The PDP-8/201A line adaptor interface is hence that portion particular to the 201A communication link being considered.

Unless otherwise indicated, the basic PDP-8/201A line adaptor interface will be considered in the main body of the report. Detailed specifications of the 201A interfaces on the Data Concentrator and the 201A interface without data break are given in Appendices II and III respectively.

The subsystem designated by "201A Line Adaptor Control" in Figure 1 is specified in more detail in Figure 2. The basic component of the 201A line adaptor is the serial-deserializer register (SDR). This is a serial-in parallel-out or parallel-in serial-out shift register. It accepts and transmits to the 201A data set a serial data stream at 2000 bits/sec.

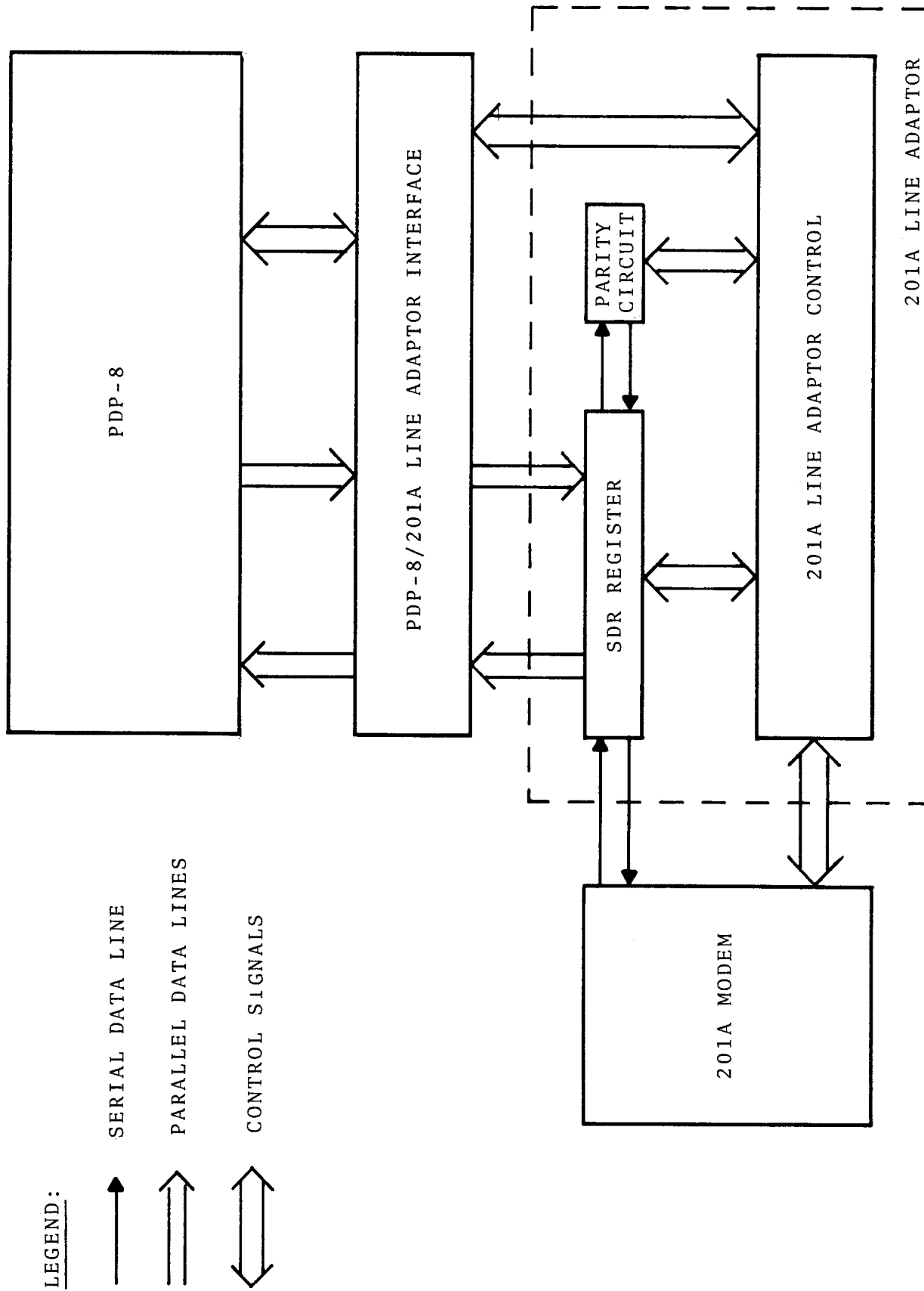


Figure 1. 201A COMMUNICATION LINK

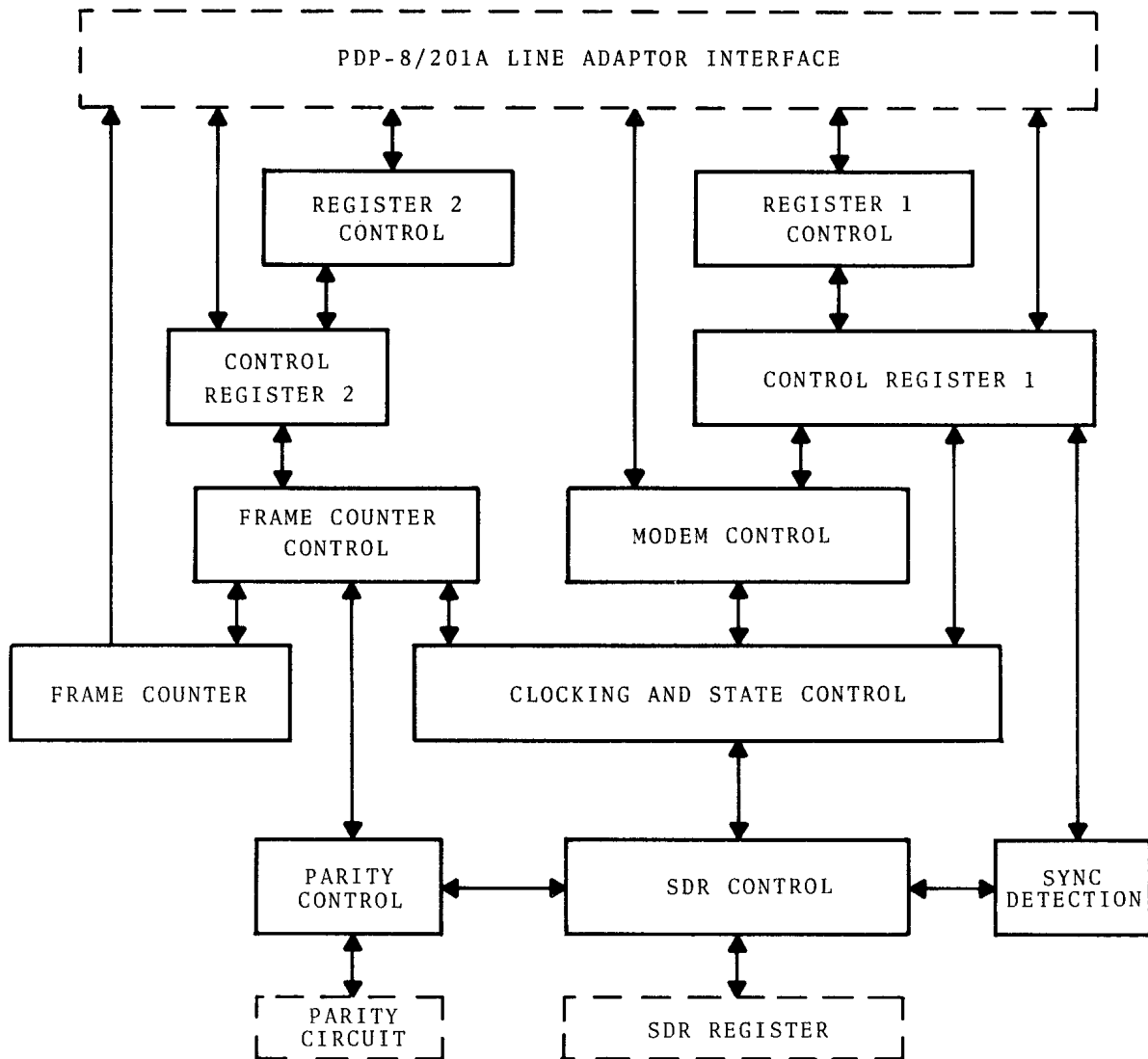


Figure 2. 201A LINE ADAPTOR CONTROL

On the other hand, it accepts from or transmits to the PDP-8 characters (usually 8 bits in length) in parallel. All clocking, with the exception of the data-break timing, is provided by the 201A data set.

The PDP-8 sees the 201A line adaptor (L.A.) as two control or status registers with all interaction being mediated through the manipulation of bits in these 2 registers. A detailed description of these registers as seen by the PDP-8 software is given in the next section. It is sufficient at this point to note that these registers, along with the frame counter, specify to the interface its state and hence the appropriate action to take at any given instant.

The frame counter is that counter in the line adaptor which determines when the correct number of bits have been shifted into or out of the SDR register. When the frame counter overflows, the character is data-brokeed into core, in the case of a receive operation, or a new character is loaded into the SDR register from core in the case of a transmit operation. At the same time, an interrupt flag is set and the frame counter is reloaded. The L.A. then continues to assemble or disassemble the next character while the proceeding interrupt is being processed by the PDP-8. This process is repeated over and over again for each character of the message. If, however, the interrupt flag has not been cleared when the next interrupt is generated, a Data Lost flag is set in addition as an error indication to the PDP-8.

When vertical parity calculation is enabled in the L.A., the frame size is assumed to include a parity bit as the high-order bit. The parity calculation is based on odd parity, and a parity error will cause only the Parity Error flag to be set, with no other abnormal action initiated by the L.A. The remaining function of the L.A. is to achieve character synchronization. This is accomplished by scanning the received data stream for a given bit pattern designated by SYN (026₈).

When this pattern is found, the interface is placed in what is called the text mode state, and the actions described above then take place. At the discretion of the PDP-8 software, the L.A. can be taken out of the text mode state, with the result that the scanning process will be resumed.

The control sequences to transmit and receive data will be described below. The remainder of the L.A. consists of buffers and gates which will be described in detail in the section on logic.

The PDP-8/201A line adaptor interface performs the logical and electrical function of mating the PDP-8 and the 201A line adaptor. This entails the control of the data-break operation between the 201A L.A. and the PDP-8, gating necessary for programmed data transfer, and the logic required for the interrupt control between the two devices. The details of these operations are presented in Appendices I, II, and III since they vary among the three systems.

PROGRAMMING AND CONTROL CONSIDERATIONS

The PDP-8/201A data communication interface in the case of a standard PDP-8 with single-cycle data-break capabilities is controlled by the resident PDP-8 program via three sets of IOT instructions. The device codes for these three sets of IOTs must be consecutive with the first one divisible by 4.* For example, 40, 41, and 42 are not used on most PDP-8 installations and satisfy the requirements. Furthermore, the hardware specifies (at the option of a given installation) two locations in core to be used as receive and transmit buffers. These locations must also be sequential with the convention that: receive $\equiv 0 \pmod{2}$ and transmit $\equiv 1 \pmod{2}$.

After the 201A L.A. transfers a word between the SDR register and the core buffer, the 201A L.A. will generate an interrupt. The first set of IOTs will service the interrupt

* that is, the second octal digit is either a 0 or 4.

as follows:

Identify Transmit Interrupt (6xx1)

This micro-instruction causes a skip if an interrupt caused by a 201A transmit operation is pending.

Identify Receive Interrupt (6xx2)

This micro-instruction causes a skip if an interrupt caused by a 201A receive operation is pending.

Clear 201 Interrupts (6xx4)

This instruction will cause the 201A transmit and receive interrupt flags and the character service flag in the 201A status word to be cleared.

The 201A L.A. has two status or control words associated with it. Control Word 1 is serviced by the second set of IOTs and Control Word 2 by the third. (Figure 3 gives the bit assignment of these control words, and their interpretation is given below.) The IOTs for Control Words 1 and 2 behave identically.

Read (6xx1)

The contents of the specified control word is ORed into the AC.

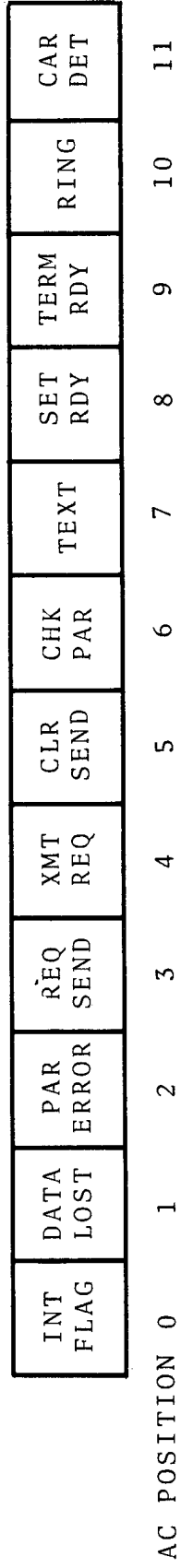
Skip Under Mask (6xx2)

The PDP-8 will skip the next instruction if any position of the AC is a one and the corresponding position in the control word is a zero.

Invert Under Mask (6xx4)

This instruction inverts (complements) each bit of the control word for which there is a one in the AC.

CONTROL WORD 1:



CONTROL WORD 2:

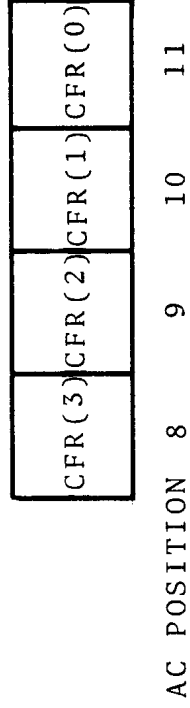


Figure 3. BIT ASSIGNMENT OF CONTROL WORDS

The first status register, called Control Word 1, is the basic 12-bit control register for the 201A L.A. It contains the necessary status information to control the 201A data set and L.A., and to determine its state. The second status register, Control Word 2, is a four-bit register which contains the modulo 16 complement of the character or frame size, not including vertical parity. When vertical parity is enabled, as noted above, the frame size includes a bit position for parity even though it is only detected and used by the hardware. For example, in normal operation, the character size is 8 bits with vertical parity checking and computation disabled; thus Control Word 2 in this instance would contain 10_8 . The restrictions on the frame size from a hardware point of view are that it be greater than 2^* and less than or equal to 12_{10} , including parity.

The following definitions give the name of each bit in Control Word 1 and its position relative to the AC along with the prescribed effect the software should have on each status bit. The operations available to the software (read, clear, and invert) are indicated in parentheses.

INT FLAG—Interrupt Flag (Clear) (ACO)

When receiving, indicates that a character has just been placed in the receive buffer. When transmitting, it indicates that a character has just been taken from the transmit buffer and will be transmitted. An interrupt will occur only and always in these cases.

DATA LOST—(Clear) (AC1)

Indicates that an interrupt has occurred when the INT flag is set. This should indicate, if interrupts are processed correctly, that overrun has occurred and hence a character has been lost (receive) or a duplicate character sent (transmit).

*Note: The SYN character is constrained to be 8 bits.

PAR ERROR—Vertical Parity Error (Clear) (AC2)

Indicates a vertical parity error has occurred on the present character received. This indication will occur only if bit AC6 is set (see description below).

REQ SEND—Request-to-Send (Read) (AC3)

This is a data set control signal which tells the data set to produce a carrier and begin transmitting when the clear-to-send signal comes on. This signal is generated and cleared via transmit request in a manner described below.

XMT REQ—Transmit Request (Invert) (AC4)

By setting this bit, the request-to-send bit is set if the 201A L.A. is not in the receive state. If the 201A L.A. is actively receiving, the receive operation is terminated at the next end-of-character indication and then the request-to-send signal is given. If the 201A L.A. is actively transmitting and XMT REQ is cleared, the 201A L.A. will go into the receive idle state at the next end-of-character indication, that is, waiting for the carrier to be detected from the other end of the line.

CLR SEND—Clear-to-Send (Read) (AC5)

Indicates that sufficient time has elapsed since the request-to-send indication was given and the line is now in a transmit ready state. This indication is not the data set clear-to-send signal, but an indication derived from the data set signal which guarantees proper operation of the interface.

CHK PAR—Check Vertical Parity (Invert) (AC6)

Indicates to the 201A L.A. that in the receive state vertical parity is to be checked, and in the transmit state vertical parity is to be computed and the correct bit appended to the character and transmitted. Vertical parity is always

computed in the 201A L.A., but no action is taken unless the CHK PAR bit is set. This continual computation allows the 201A L.A. to go from non-parity operations to parity operations within one character time.

TEXT—Text Mode (Invert) (AC7)

In the receive state, text mode indicates that character synchronization has been found. If the TEXT bit is cleared while in the receive state, this tells the interface to look for new character synchronization. While looking for character synchronization no interrupts will occur. The first interrupt will occur on the first character received following the establishment of character synchronization.

When in the transmit state, TEXT should normally not be altered. If the TEXT bit is cleared while transmitting, the interface is frozen until the TEXT bit is set again. This has the effect of transmitting continually the bit being presented to the line at the time the TEXT bit was cleared. During this time no interrupts will occur.

The 201A L.A. will always place the TEXT bit in the correct state. It should be changed under program control only if the actions described above are desired.

SET RDY—Set Ready (Read) (AC8)

Indicates that a call has been answered and that there is a data set in the data mode at the other end of the line. This indication drops when either party hangs up.

TERM RDY—Terminal Ready (Invert) (AC9)

Indicates to the data set that it should automatically answer a call.

RING—Ringing (Read) (AC10)

Indicates that the data set is being called. The indication follows the actual bell or ring signal to the hand set.

CAR DET—Carrier Detect (Read) (AC11)

Indicates that carrier is on the line. In most cases of normal operation when CLR SEND is on, it indicates that local carrier is present, and conversely when CLR SEND is off, that carrier is being received from the other end of the line.

Throughout the definitions above, reference was made to the transmit and receive states. These states are defined within the 201A L.A. as the logical conjunction of certain signals. That is, the 201A L.A. is in the transmit state if and only if all the following signals are present:

- a. REQ SEND
- b. CLR SEND
- c. SET RDY
- d. TERM RDY
- e. CAR DET

The 201A L.A. is in the receive state if and only if all the following conditions are true:

- a. REQ SEND is not present
- b. CLR SEND is not present
- c. SET RDY is present
- d. CAR DET is present

The 201A L.A. is in the receive-idle state if and only if all the following conditions are true.

- a. REQ SEND is not present
- b. CLR SEND is not present
- c. SET RDY is present.

A DATA FORMAT SCHEME

For the sake of completeness a brief sketch and discussion of a message format scheme is presented. The only portion of this scheme which is affected by the hardware is the actual SYN character. This particular scheme is presented for exposition purposes only and is not intended to represent the existing 201 software support.

An inbound message has the following format:

<Sync Characters><Text Characters><Terminating Character><Two Block Check Characters>.

These characters are defined as follows:

TABLE I

CONTROL-CHARACTER DEFINITIONS

ASCII NAME	OCTAL	HEX	FUNCTION
ETX	003	03	End of Text
EOT	004	04	End of Transmission
ENQ	005	05	Enquiry
ACK	006	06	Positive Acknowledgment
NAK	025	15	Negative Acknowledgment
SYN	026	16	Synchronous Idle
ETB	027	17	End of Text Block
EOM	031	19	End of Message
PAD	377	FF	Pad for Line Turnaround

A Sync Character is the ASCII SYN character. A minimum of four sync characters will be required to guarantee proper character synchronization by the software. In the case of long distance operation where there is echo suppression on the telephone line a sufficient number of PAD characters must precede the SYN characters to allow the line to settle down.

A Text Character may be any combination of eight bits which is not identical to a terminating character. The positive acknowledgment character, ACK, and the negative acknowledgment character, NAK, are considered message characters for transmission purposes. Likewise SYN is a message character which when received is deleted from the message. The message may be the empty string, that is, no text characters.

A Terminating Character is any member of the following set of characters:

{ETX,ETB,EOT,EOM,ENQ} .

Each of these terminating characters will have the effect of terminating the present message along with other logical implications to the software.

The Block Check Characters are longitudinal parity check characters treated as a code word in a cyclic code whose generating polynomial is

$$x^{16} + x^{15} + x^2 + 1 .$$

Two block check characters must accompany every message.

This format is used in a store and forward mode; that is, the PDP-8 receiving a message across a 201A data communication link will store the incoming message. Concurrently it will forward that message at a rate that the interrupt processing will bear, calculating the cyclic checksum as it proceeds. In general, when the terminating character is finally encountered in this forwarding operation, the two checksums (the one actually received and the one computed) are compared. If the two match, a positive acknowledgment ACK is returned to the sender. If a discrepancy exists, an NAK or negative acknowledgment is returned. The software determines what to do in these cases, and this problem will not be discussed here.

An outbound message has the same format as an inbound message with the addition of at least one PAD character appended to the end of the message to allow for proper "flushing" of the communication link. The PAD characters are always ignored in this context.

A graphical presentation of a message exchange as viewed from the PDP-8 is shown in Figure 4. For exposition purposes the handshake message has the form:

(SYN1)(SYN2)(TEXT CHAR)(ETX)(BCC1)(BCC2)(PAD1)(PAD2) ,

with the acknowledgment taking the form

(SYN1)(SYN2)(ACK)(ETX)(BCC1)(BCC2)(PAD1)(PAD2) .

In Figure 4, the control status is affected either by the program (P.S.-Program Set, P.C.-Program Clear) or by the data set or interface (D.S.-Modem Set, D.C.-Modem Clear).

DETAILED LINE ADAPTOR LOGIC

This section will present in detail the logical design of the 201A line adaptor. The logic diagrams follow standard Digital Equipment Corporation conventions. A working knowledge of D.E.C.'s R and W series logic is assumed throughout this section. The remainder of the logic for the 201A Interface is given in Appendices I, II, and III for each particular version of the interface. For completeness, both the module position and pin assignment for each circuit is indicated. All circuits within this section are in the same D.E.C. 1943 wire-wrap panel. The detailed module utilization is presented with the particular interface in the Appendices. In order to allow for multiple adaptors, as used on the Data Concentrator, the common signal names are prefixed with a # sign. In a single adaptor configuration the # sign is just part of the signal name. The logic will be presented as much as possible within the framework of Figure 2.

Serial-Deserializer Register (Diagram 1)

This is a 12-bit register with high-order position #SR00 and low-order bit #SR11. Serial data are shifted into #SR00 in the receive state from the data set on the clock signal #SHIFT. They are shifted out of #SR11 in the transmit state into a line buffer #SDBF. Characters are strobed into the SDR register in a data-break operation from the buffered memory buffer on the #MBSR signal. This character transfer is simulated in the case of an interface not using data break, and those details are treated in Appendix III. The operation of character transfer to the PDP-8 is treated in the Appendices.

Clock Gating (Diagram 2)

The 201A data set provides two clock signals, #SCRB (receive clock) and #SCTB (transmit clock). The #SCTB clock is always available and is used within the data set for internal control timing. The #SCRB clock is derived from the received data stream and is provided to sample the received data line (#RDB). The interface selects the correct clock on the basis of its state (transmit/receive).

SDR Pulse Gating (Diagram 3)

The control of the SDR register is primarily achieved through the four pulse amplifiers (Diagram 3). To keep all transitions occurring synchronously with the #CLOCK signal it is necessary to separate the clearing of #SR00 from the remainder of the register. By the use of the #FR3+ signal, the register is cleared at the end of a transmitted character before the next character is loaded. It is cleared at the end of a data-break operation in the receive state via #BRKDN; and all but #SR00 is cleared when character synchronization is found in the receive state. In this last case, while the remainder of the register is cleared the first bit is read in from the line. #MBSR loads ones into the register during a data break in the transmit state.

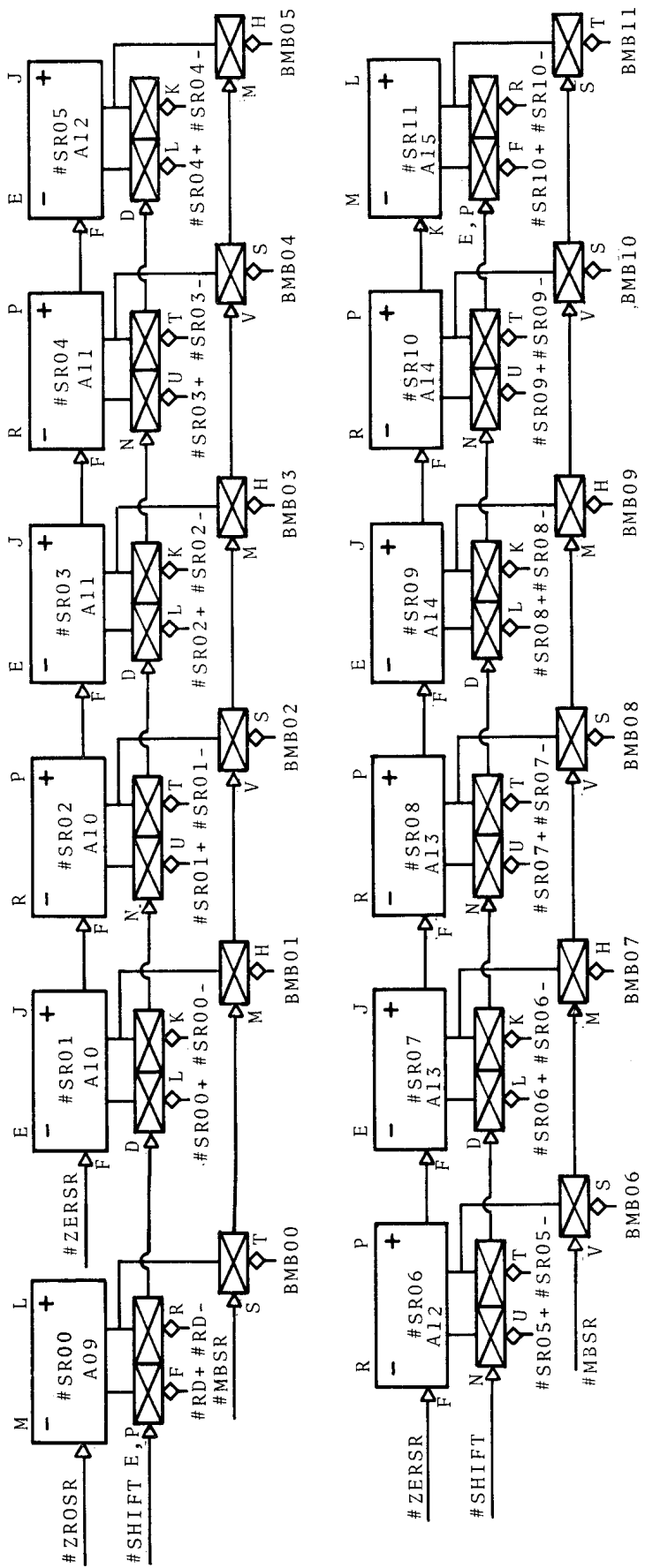


Diagram 1. SDR REGISTER

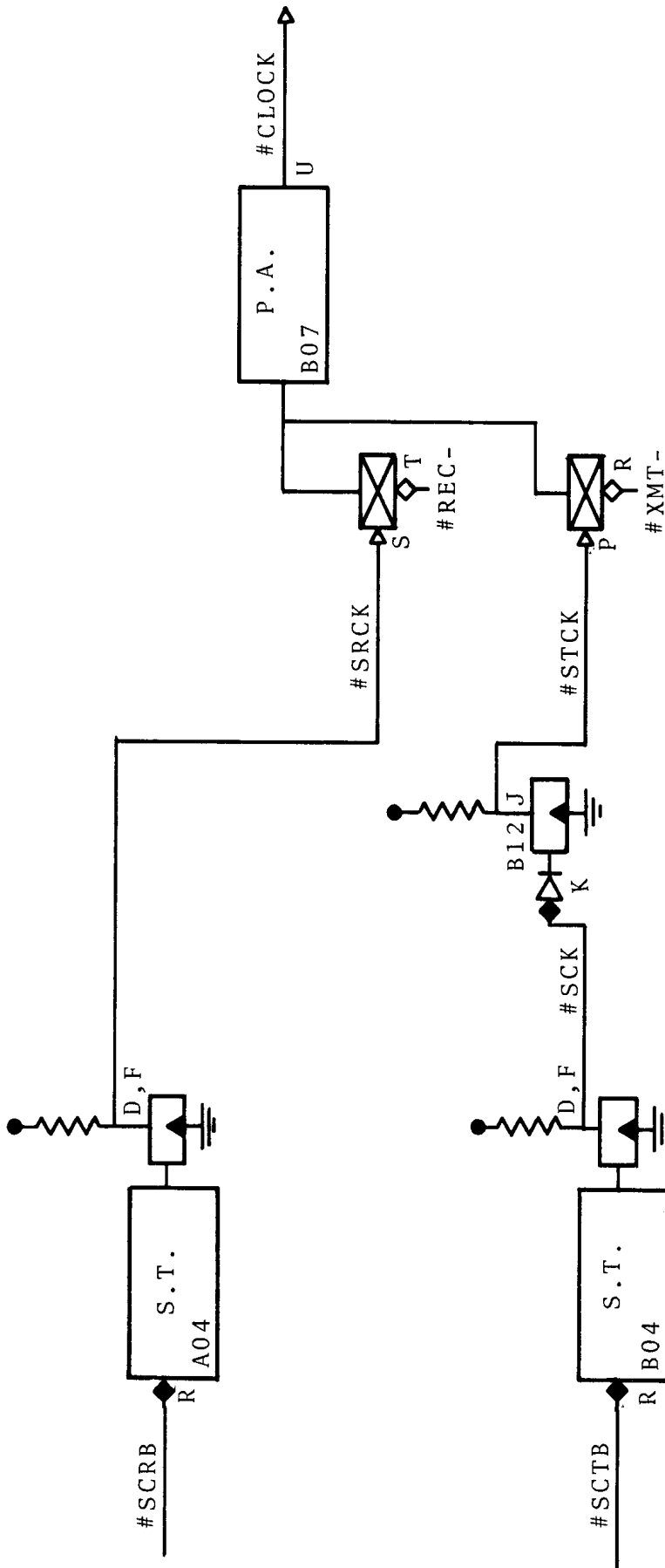


Diagram 2. CLOCK GATING

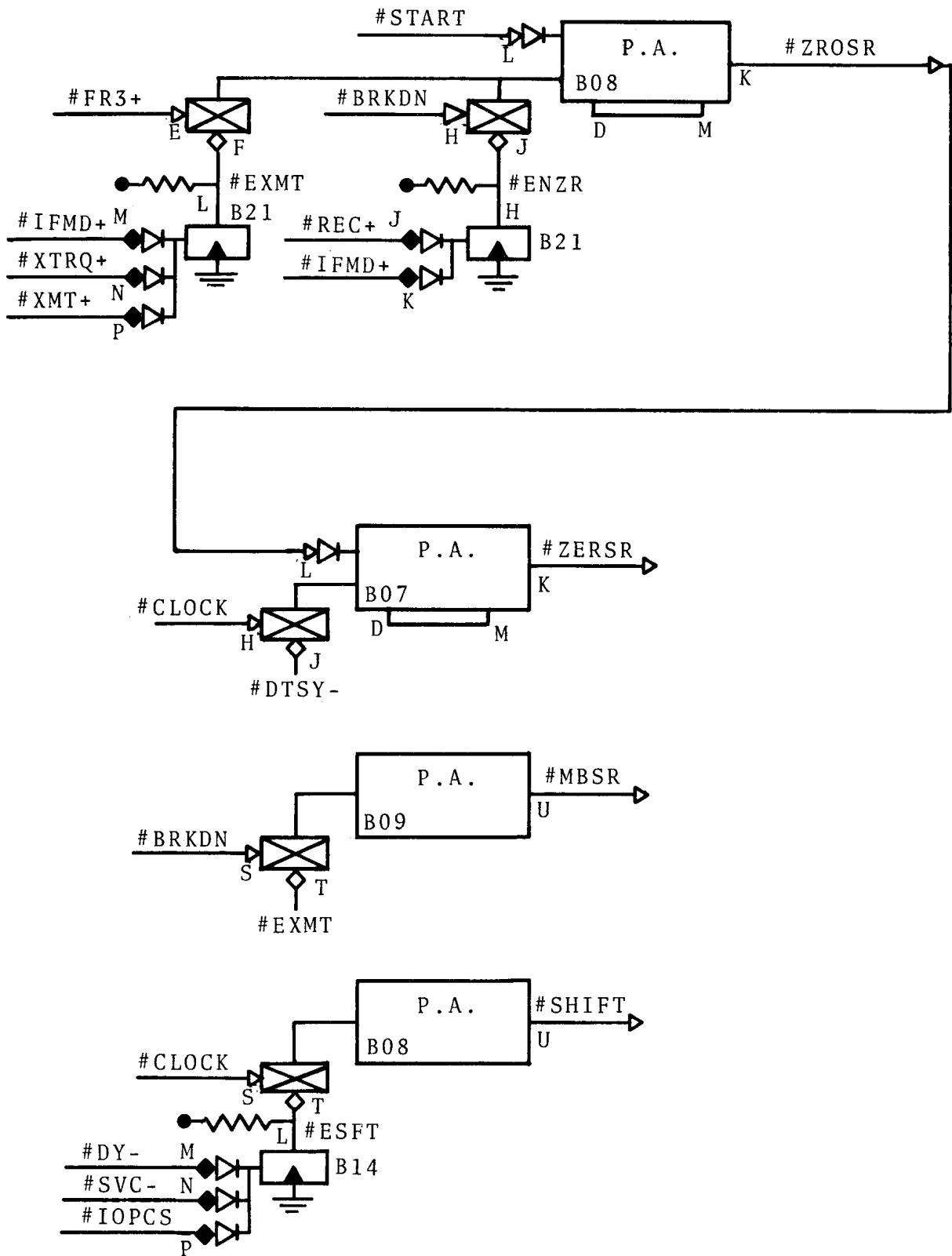


Diagram 3. SDR PULSE GATING

Data Set Signals (Diagram 4)

Diagram 4 shows the correspondence between the 201 data set connector and signal designations of the 201A L.A.

SDR Serial Input/Output Gating (Diagram 5)

The serial input signal #RDB from the 201A data set is converted to standard D.E.C. levels (-3v, 0v) from E.I.A. standard levels (+6v, -6v) (Electronic Industries Association Standard R S 232: Interconnection of Data Terminal Equipment with a Communications Channel). When not in the receive state, the input to the SDR register is conditioned (#RD+) to shift a zero into the SDR register. The #LINE flip-flop determines whether the output from the SDR register buffered via #SDBF or a parity bit (#PTBF) is placed on the transmit data line (#SDB). When the L.A. is in the receive state, zeros are always placed on the #SDB line to minimize possible cross-talk.

Transmit/Receive State Gating (Diagram 6)

The XMT/REC status of the interface is specified by the two flip-flops #XMT and #REC. The definition of these states has been defined above, however, it is important to note that the state changes are synchronized to the clock. The #RSYN latch is used to prevent the loss of the last receive interrupt.

Control Register 2 (Diagram 7)

The second control word as defined above contains the modulo 16 complement of the current character length. This value is referred to throughout the interface as the frame size and is stored in the register #CFRO-#CFR3. The register is loaded via IOT commands described above from the PDP-8 AC, and read into the PDP-8 on an extension to the AC called the EAC. The details of the EAC buss are described in Appendix I.

DIAGRAM 4

DATA SET/INTERFACE CABLE ASSIGNMENT

Interface Signal Name	Data Set Connector (CINCH DB-25-P PLUG)	Signal Name	Interface Connector (W021MJ*)	
	1	AA	Protective Ground	C
	7	AB	Signal Ground	C
#SDB	2	BA	Transmit Data	D
#RDB	3	BB	Receive Data	E
#RSB	4	CA	Request to Send	F
#CSDB	5	CB	Clear to Send	H
#SRDB	6	CC	Set to Ready	J
#TRDYB	20	CD	Terminal Ready	K
#RINGB	22	CE	Ring	L
#CDETB	8	CF	Carrier Detect	M
#SCTEB	24	DA	Terminal Transmit Clock	N
#SCTB	15	DB	Set Transmit Clock	P
#SCRB	17	DD	Set Receive Clock	R

* Special module with all pins available and ground connections for shielding.

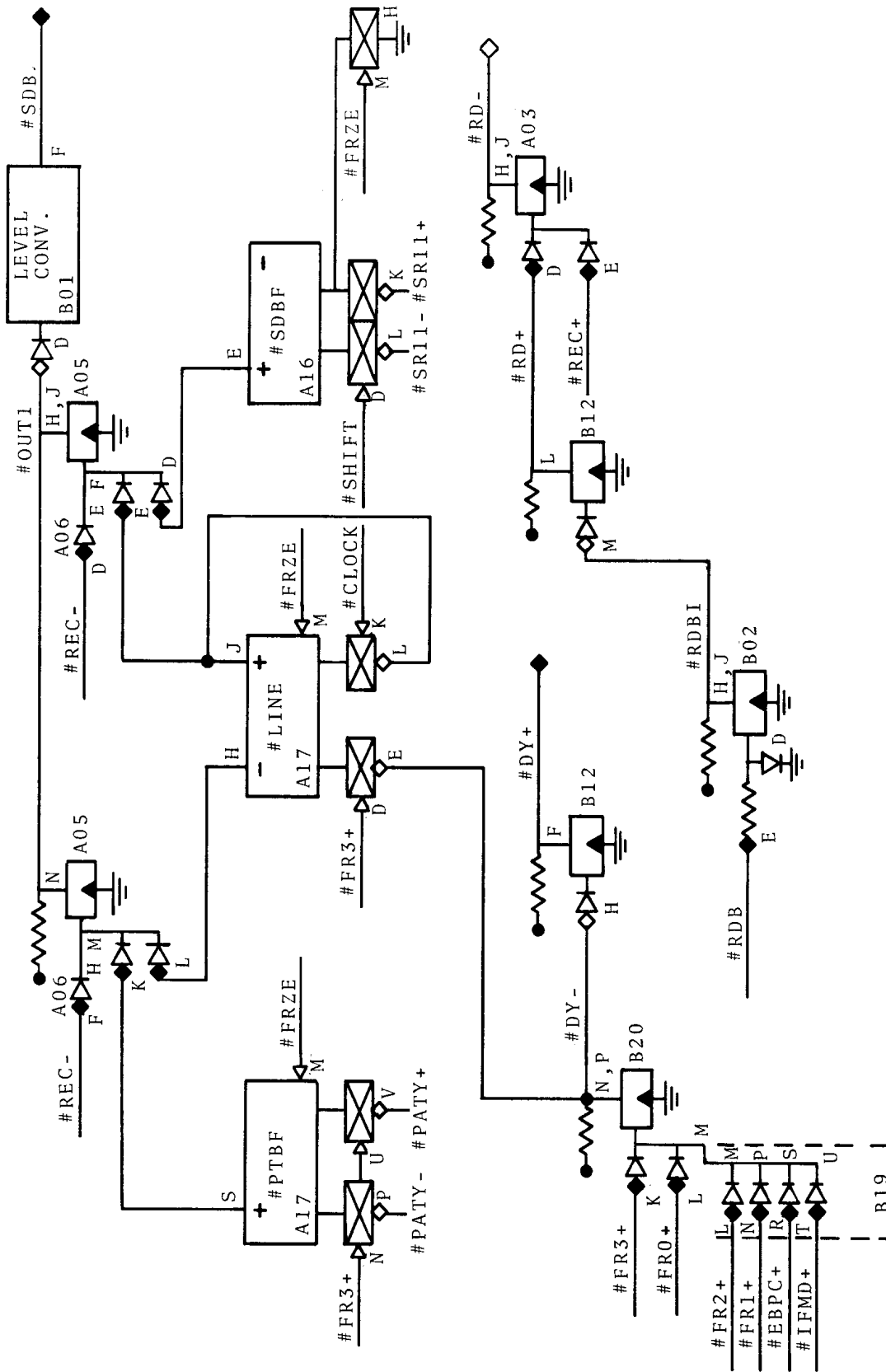


Diagram 5. SDR SERIAL I/O GATING

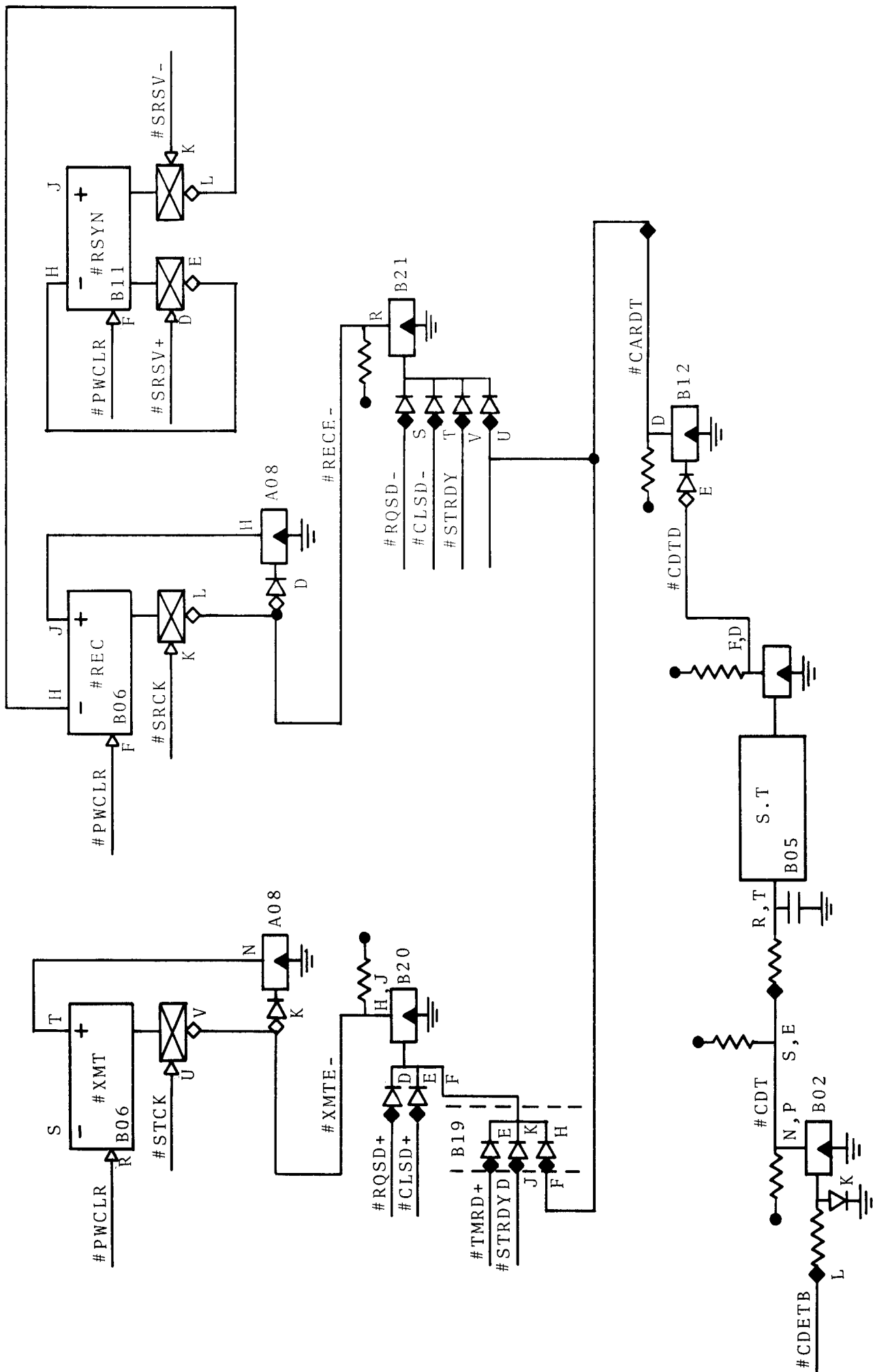


Diagram 6. TRANSMIT/RECEIVE STATE GATING

Frame Counter (Diagram 8)

The frame counter determines by its overflow when a character has been received or transmitted, thus making the positive transition of #FR3+ the character received/transmitted signal. It is reloaded from Control Register 2, each character time making use of the fact that the register is zero at this time. It is thus necessary only to clear the register at the beginning of an operation via the #SVC signal. The frame counter is normally incremented when in the text state and not in a transition state (#SVC+). The #IOPCS signal forces the counter to wait one bit time on character synchronization when parity checking is enabled to take account of the parity bit on the SYN character.

State Synchronization (Diagram 9)

The #SVC state and #SVC-positive transition are used throughout the interface to clear it on a XMT/REC state change or a change in the text state. The remainder of the logic is necessary for its synchronization to the clock signal.

Text State and Sync Detection (Diagram 10)

The text state is embodied in the flip-flop #IFMD. The flip-flop is one bit of Control Word 1 and is therefore accessed through the AC under program control. Two of its other input gates place #IFMD in the correct state when the XMT/REC state is entered. The remaining gate sets #IFMD in the text state when character synchronization is found in the REC state. This transition is conditioned by #DTSY+ and strobed on the clock signal. #DTSY+ is the logical-and gate used to determine whether the first 8 bits of the SDR register contain the SYN character.

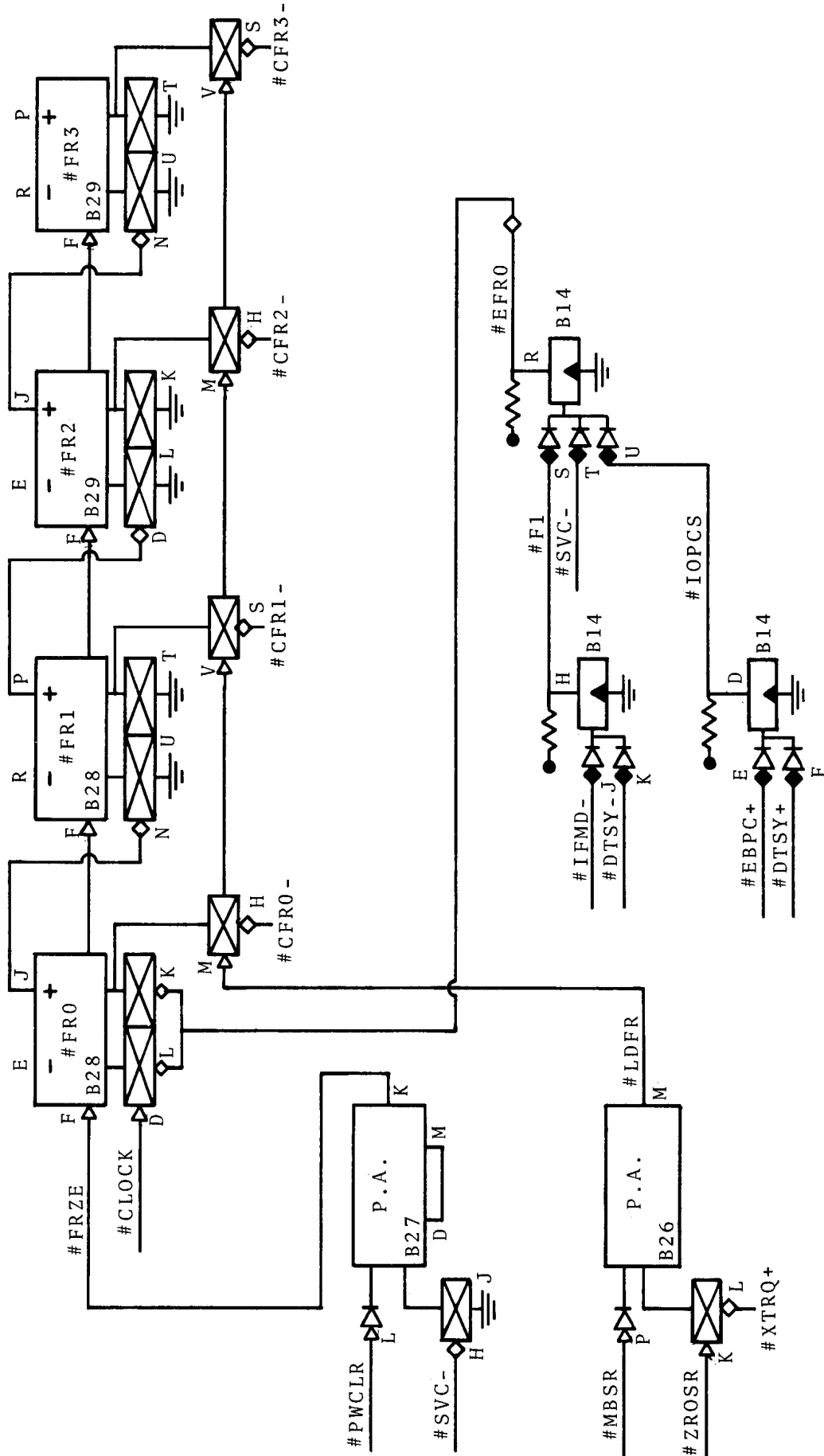


Diagram 8. FRAME COUNTER

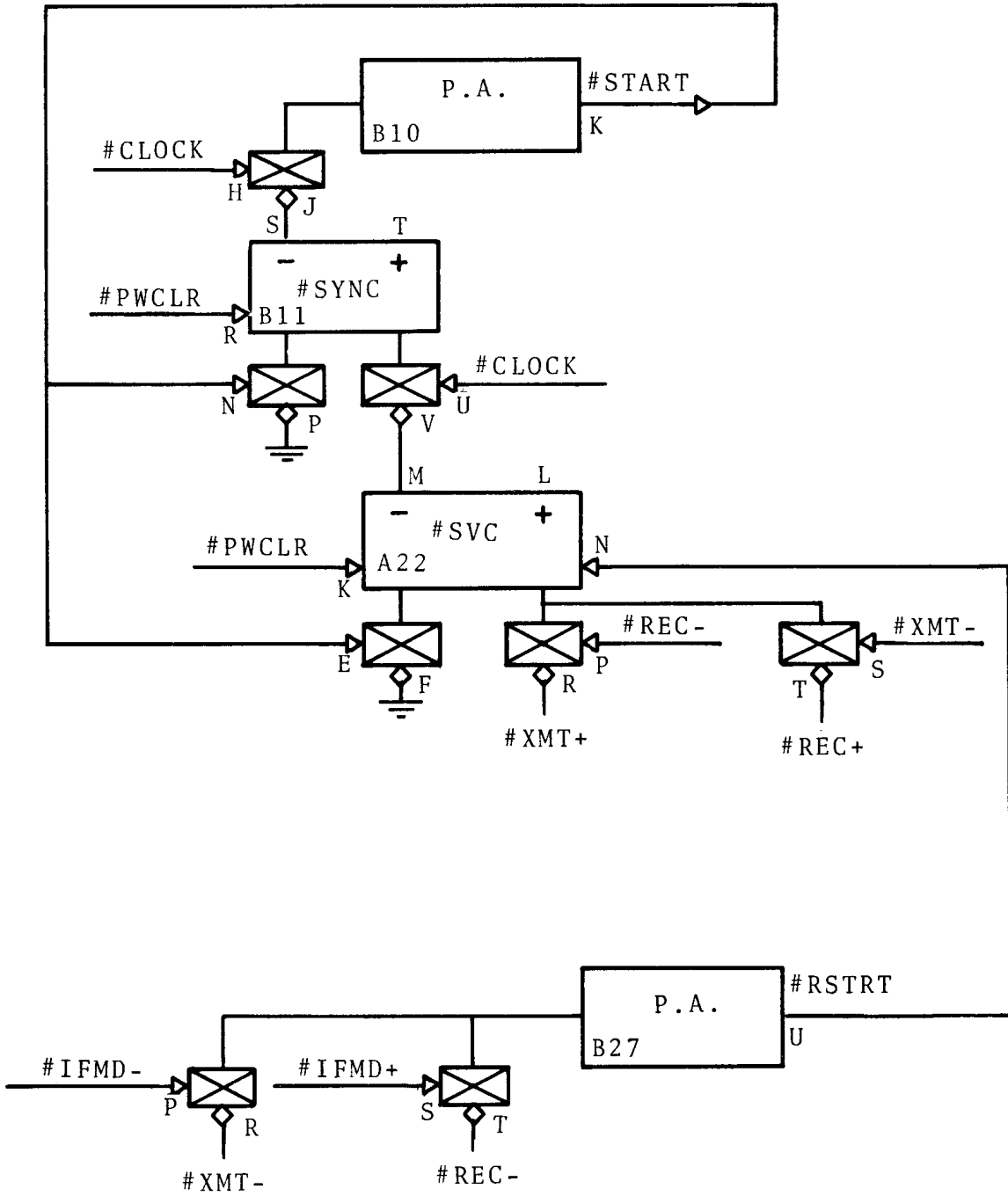


Diagram 9. STATE SYNCHRONIZATION

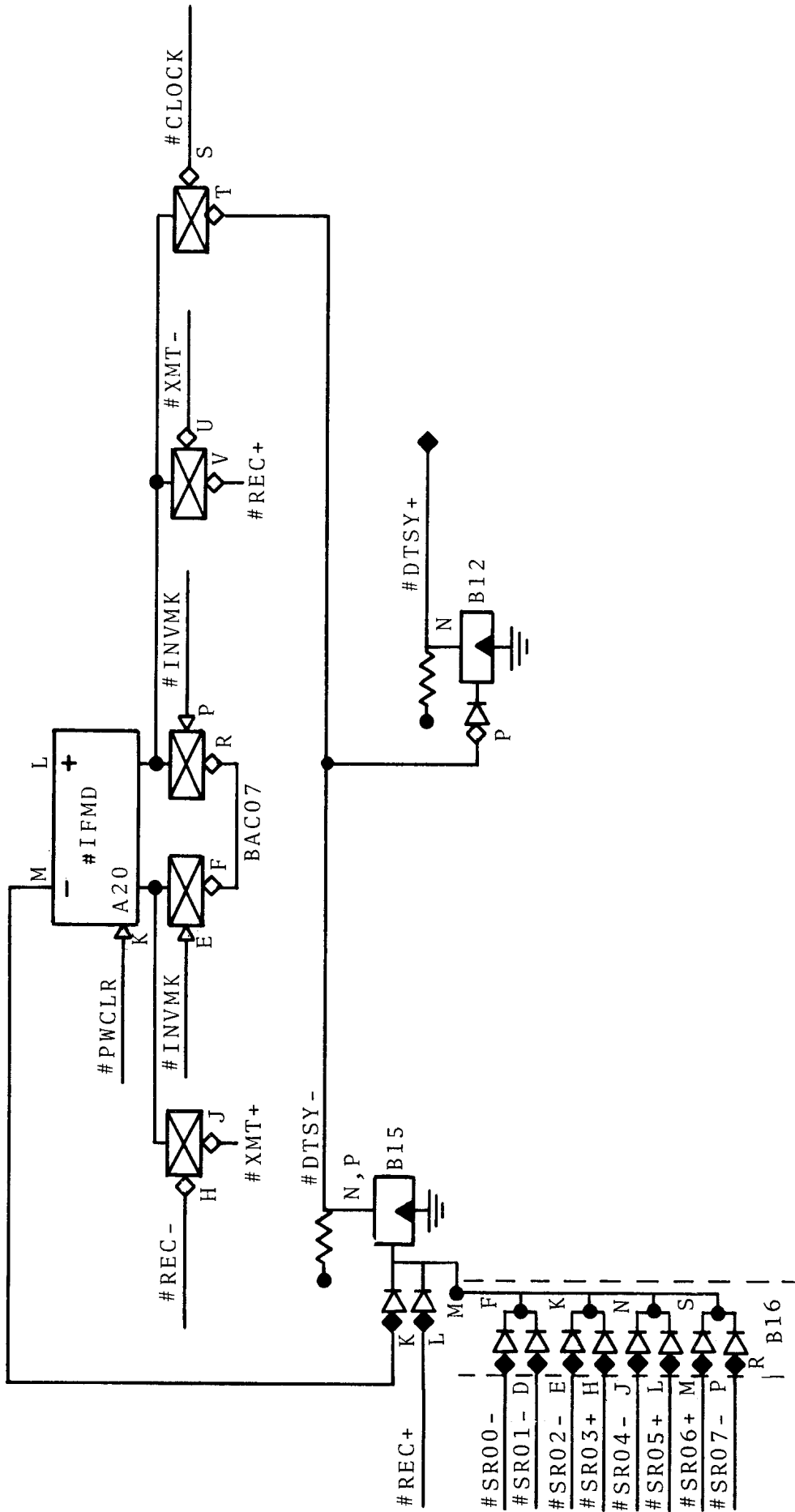


Diagram 10. TEXT STATE AND SYNC DETECTION

Parity Gating (Diagram 11)

The check-vertical-parity-status flip-flop is designated #EBPC in the interface. It is manipulated in the same manner as described above for other bits in Control Word 1. The parity error flip-flop is #PAR and normally is set to zero when #EBPC is not set. When parity checking is enabled, the accumulated parity in #PATY is compared against the last bit of the character when receiving, and #PAR is set if they are not the same.

Clear- and Request-to-Send Gating (Diagram 12)

The contents of the transmit request flip-flop (#XTRQ) is jammed into the request-to-send flip-flop (#RQSD) at the end of each data-break cycle requested by the interface. Since the cleared status of #RQSD is \neg (request-to-transmit) a gate is provided to set #RQSD immediately upon the transition of #XTRQ if the interface is in neither the XMT or REC state. This method of control of request-to-send guarantees that the processing of the current character will be concluded before the XMT/REC state is changed. Furthermore, if #RQSD is set, at least one character must be transmitted before a receive operation can occur.

The clear-to-send indication, #CLSD, is derived from the data set signal #CSDB. In order to avoid a spurious receive state, clear-to-send must be delayed from dropping after request-to-send drops. This delay is necessary because the data set brings up carrier after first dropping it when clear-to-send drops. It appears that this is the result of the data set "flushing" itself after a transmit operation.

Character Service Interrupt Flag (Diagram 13)

The interace's character interrupt flag is #SRSV. This flag is set in the text state on each received character, and in the text state on each character transmitted if there

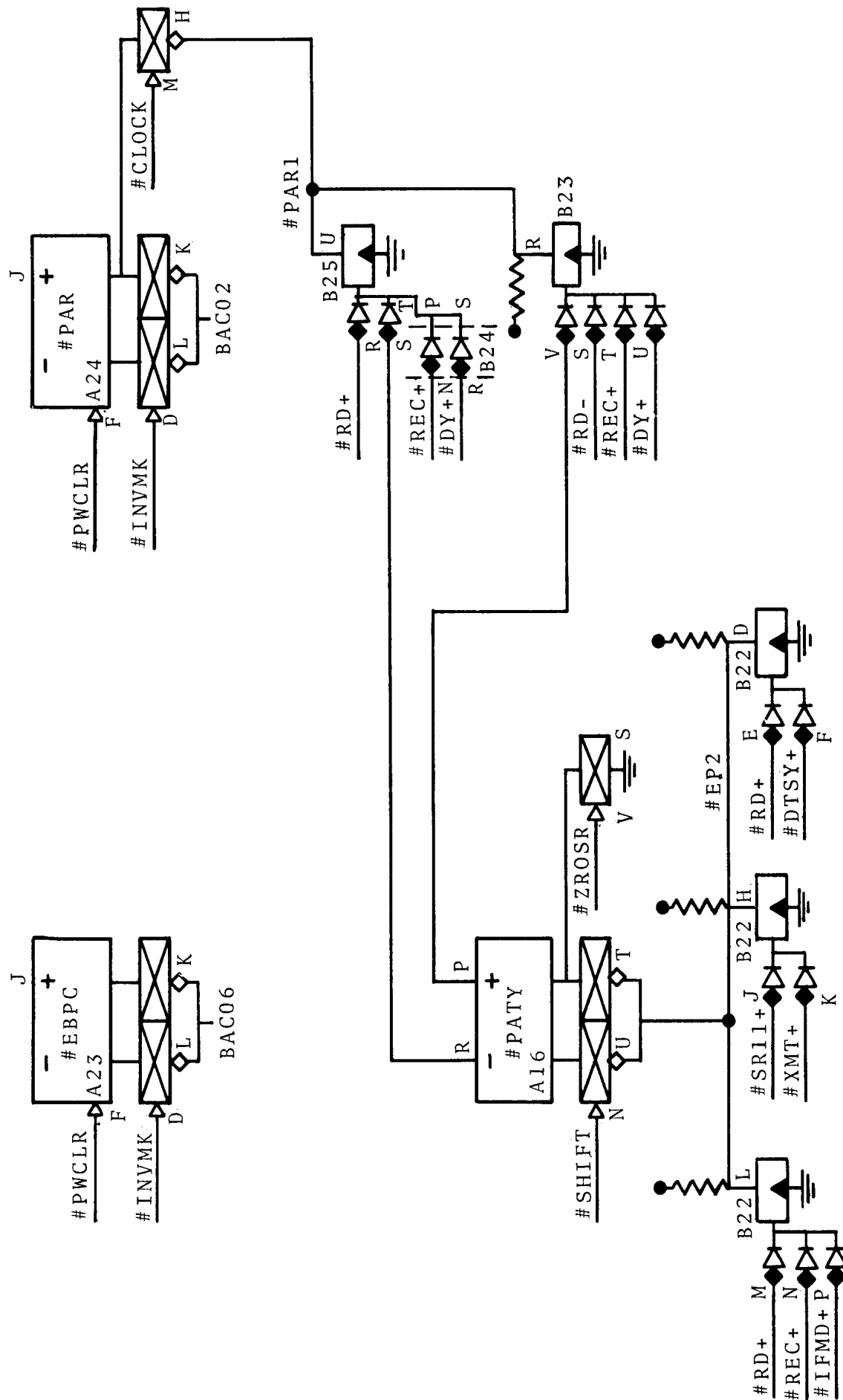


Diagram 11. PARITY GATING

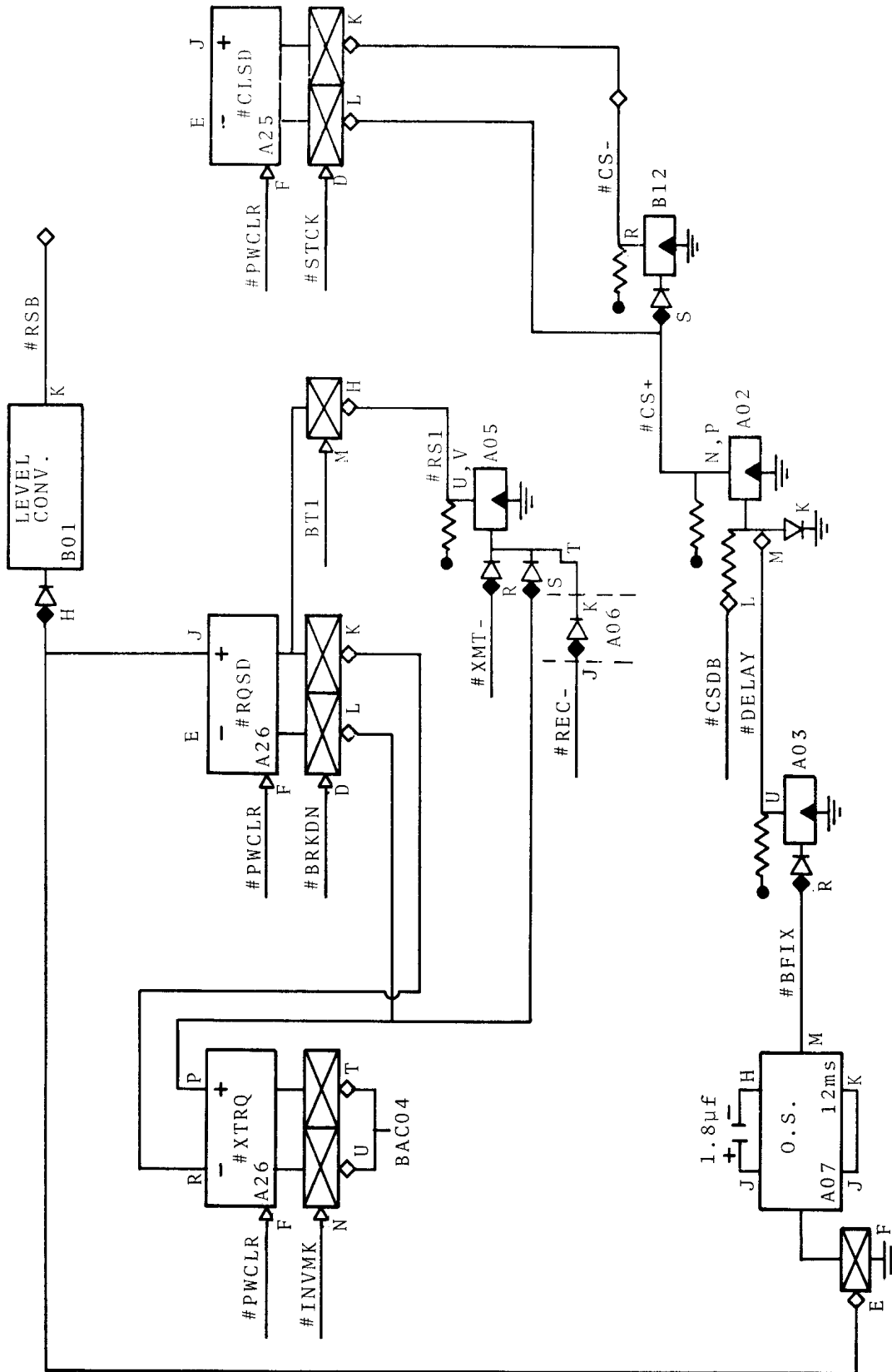


Diagram 12. CLEAR- AND REQUEST-TO-SEND GATING

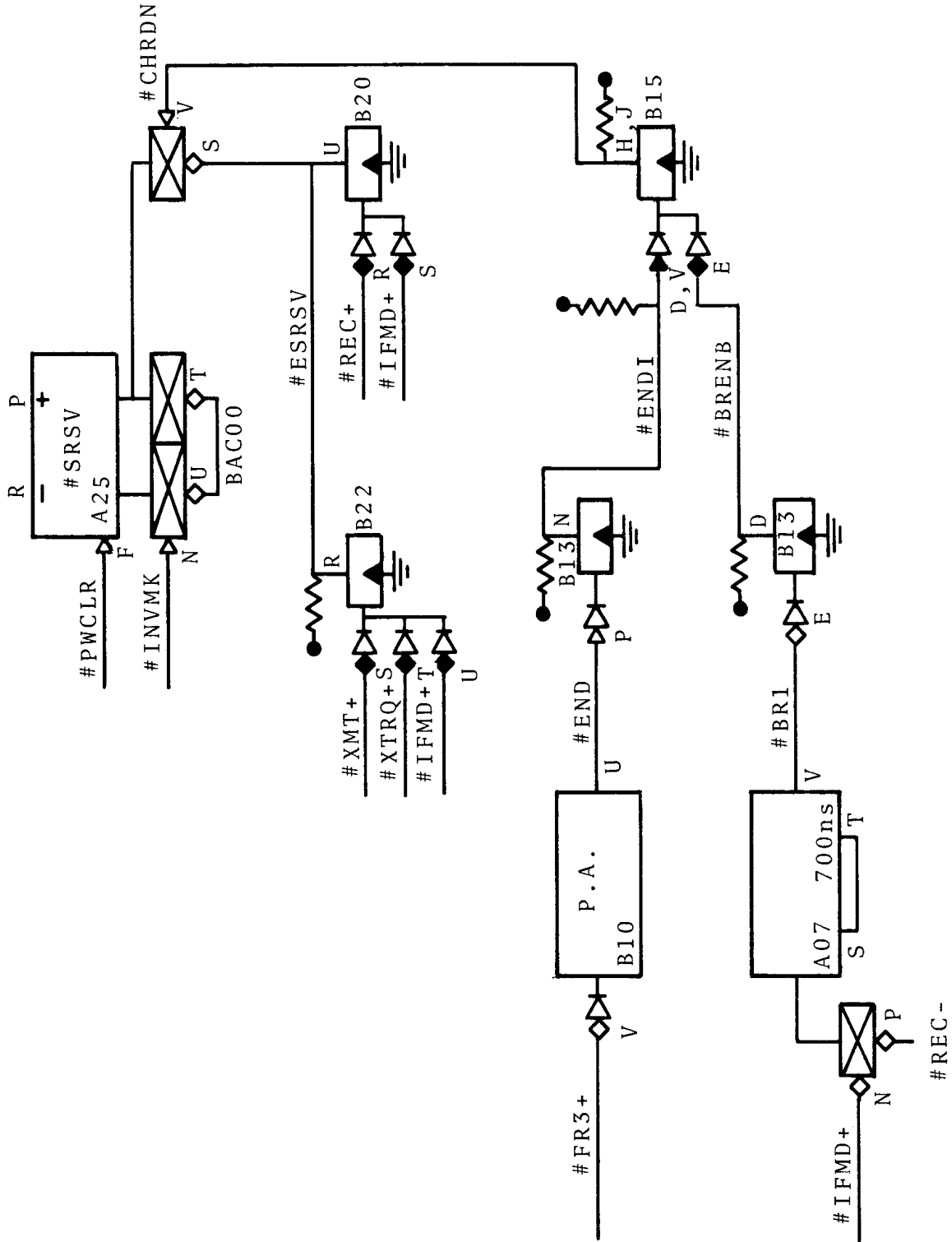


Diagram 13. CHARACTER SERVICE INTERRUPT FLAG

is still a transmit request pending. Every time the frame counter overflows, an #ENDI pulse is generated. This pulse is normally the character service request except when a change in text mode generates a false overflow, thus the need for #BRENB.

Status Indicators (Diagram 14)

Diagram 14 shows the remaining status bits of Control Word 1. Terminal ready (#TMRD) and data lost (#DLST) can be manipulated under program control as described above. Set ready (#STRDY) and (#RING) are only gates since they present static status of the data set.

Control Word 1 EAC Gating (Diagram 15)

Diagram 15 shows the gating necessary to load Control Word 1 on the extended AC buss (EAC).

Miscellaneous Pulses (Diagram 16)

To prevent undue loading of the PDP-8 power clear signal and to allow for reshaping the pulse, #PWCLR is derived. #INVMK is the pulse used to invert under mask the bits in Control Word 1.

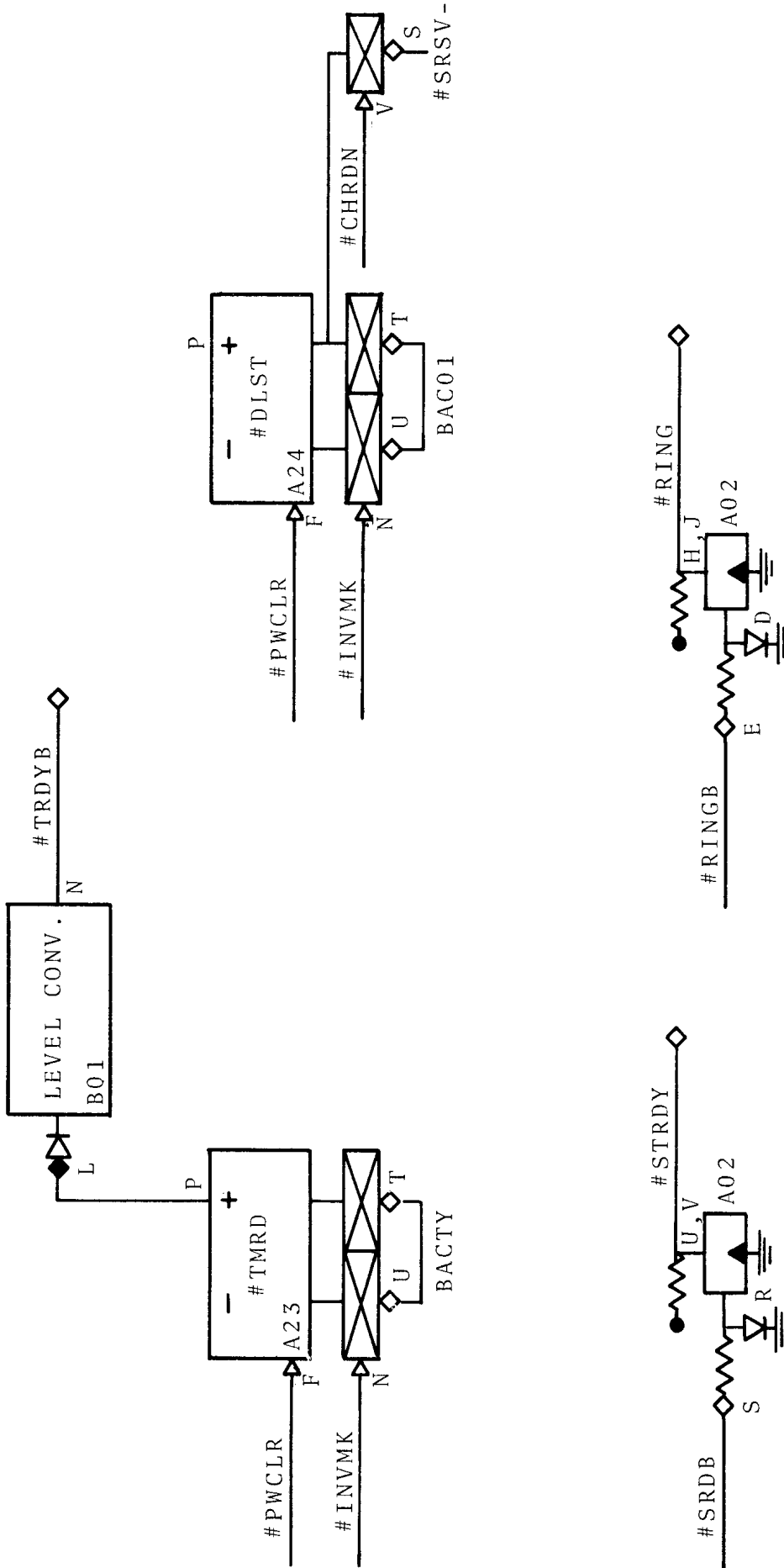


Diagram 14. STATUS INDICATORS

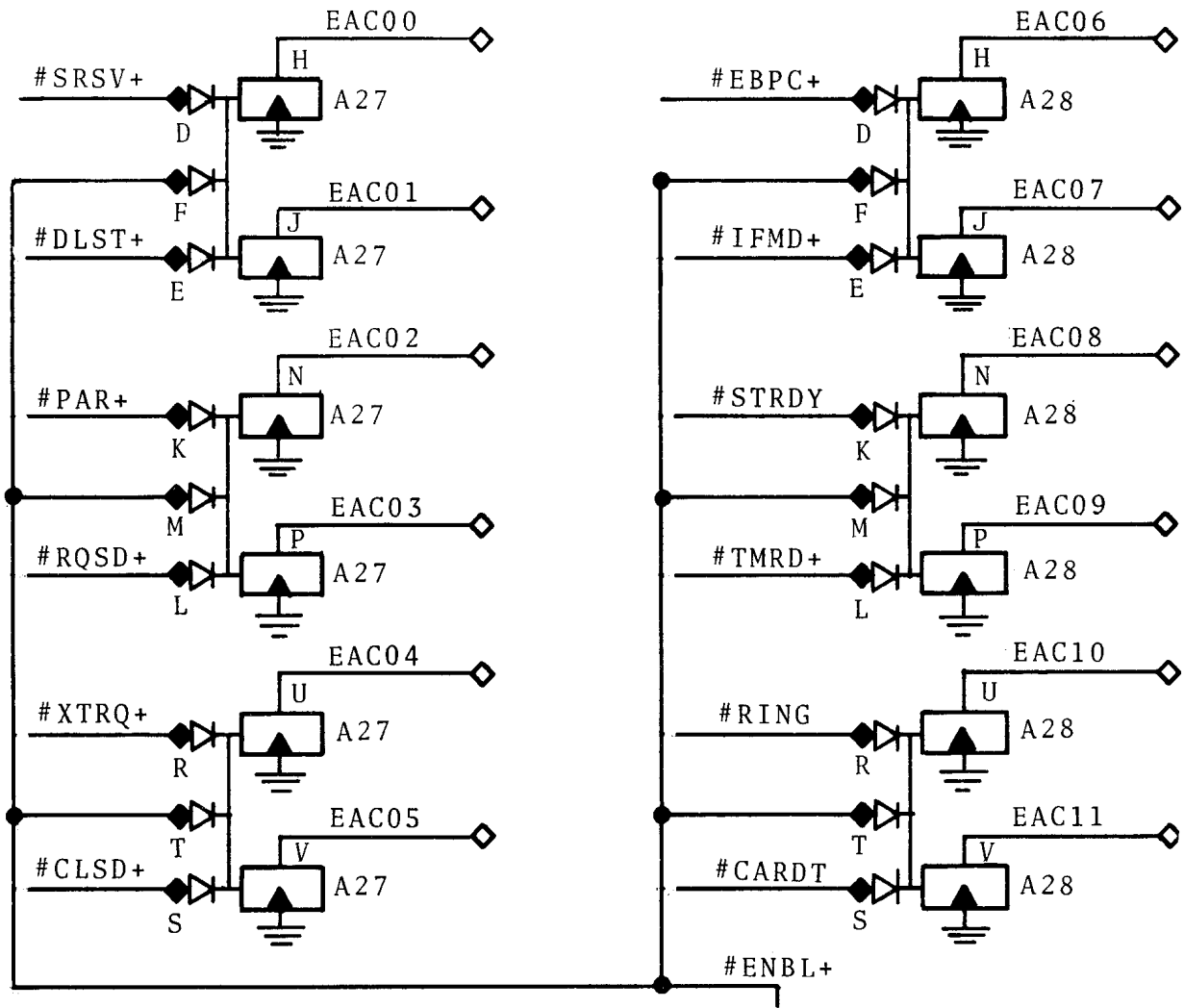


Diagram 15. CONTROL WORD 1 EAC GATING

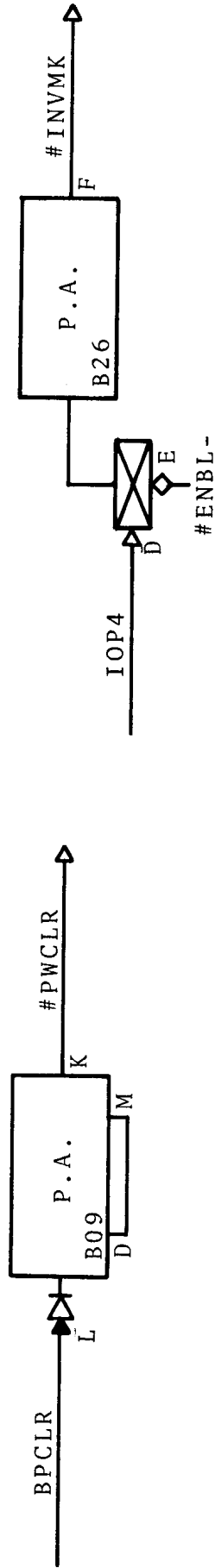


Diagram 16. MISCELLANEOUS PULSES

APPENDIX I

PDP-8/201A LINE ADAPTOR INTERFACE
FOR USE WITH A
PDP-8 WITH THE DATA-BREAK FACILITY

APPENDIX I

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APPENDIX I

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PDP-8/201A LINE ADAPTOR INTERFACE
FOR USE WITH A
PDP-8 WITH THE DATA-BREAK FACILITY

The remainder of the logic and details of the 201A data communication adaptor using the data-break facility is presented in this Appendix. With reference to Figure 1, the body of the logic to be discussed here is considered to make up the PDP-8/201A line adaptor interface.

The total 201A data communications adaptor is realized in two DEC 1943 wire-wrap panels. For the purpose of this report, each panel is called a bay. In this version of the adaptor, for the most part, the PDP-8/201A line adaptor interface is in Bay 1 with the 201A line adaptor in Bay 2. Throughout the remainder of this Appendix, unless noted otherwise, the logic discussed is in Bay 1.

Data Break Control (Diagram I-1)

The line adaptor signals the PDP-8 through the #BKRQ flip-flop that a data transfer is desired to or from PDP-8 core. The address within the PDP-8 memory is read by the PDP-8 from the data address lines. The low-order bit of this address is given by DIAD11. When the break request is given, the direction of the transfer is specified by the DICTL signal. When the PDP-8 enters the break state and the address is loaded into the memory address register, an address accepted pulse is generated by the PDP-8. At this time, the break request signal must be dropped by the interface. During the break state, as defined by the BBREAK signal, the BT1 pulse indicates the end of the break cycle, and is used to strobe the contents of the designated memory location from the buffered memory buffer register into the SDR register. The PDP-8 will also strobe the data-break input lines (DATA BIT) into memory at this time in case the transfer direction is into core. The break request signal is generated each time the frame counter overflows while

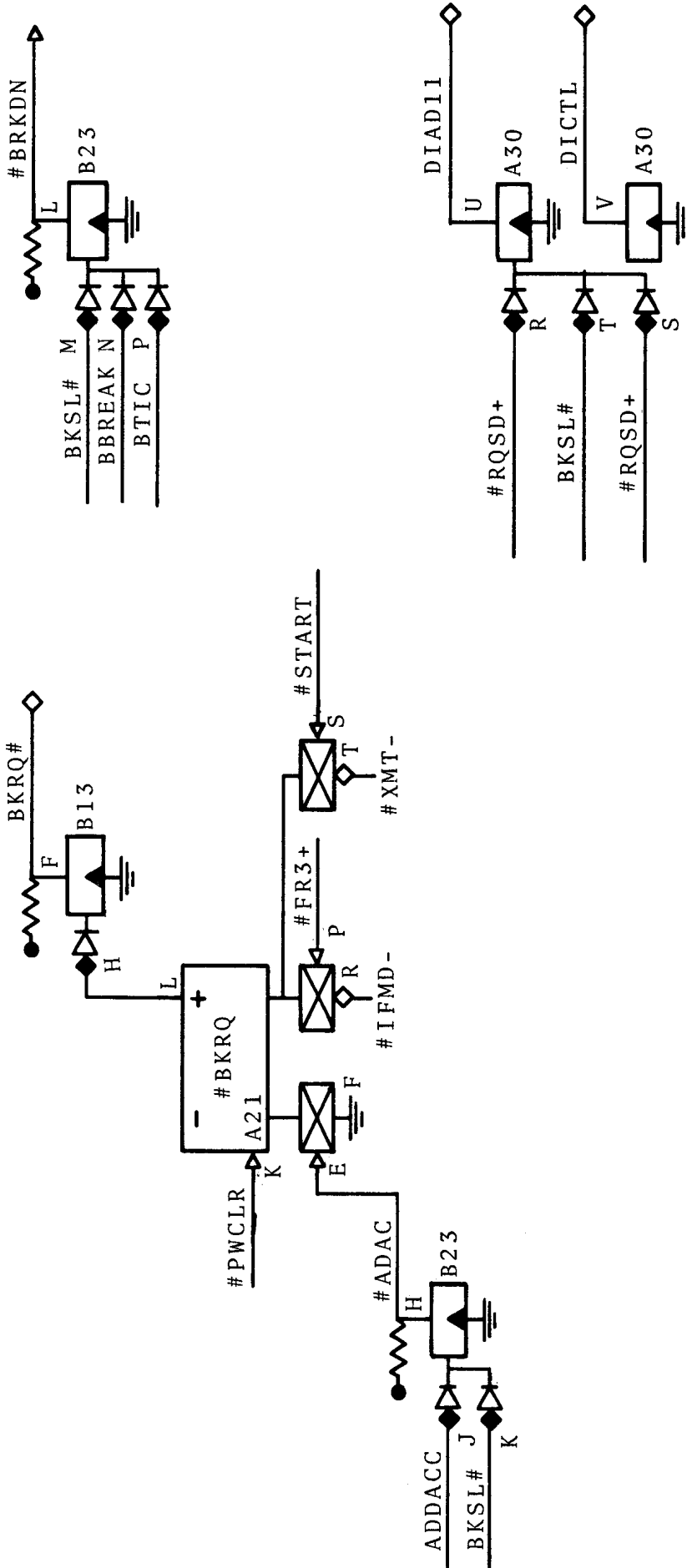


Diagram I-1. DATA-BREAK CONTROL

in the text state, and when the interface first enters the transmit state to fetch the first character to be transmitted. All of the logic shown in this diagram is in Bay 2 of the interface.

Data Break Address (Diagram I-2)

The 201 line adaptor has assigned two sequential locations in PDP-8 core to be used as buffers for incoming (received) and outgoing (transmitted) data. These two locations are specified in the hardware on a W021MG address card. The address is a 14-bit address to allow the buffers to be in any core bank. The 15th or low-order bit is not required because a pair of locations is being specified. By convention, the even location of the pair is the receive buffer and the odd location is the transmit buffer. Using the DEC numbering convention, the address is given by the vector ADDR(0)...ADDR(14). Schematically, the W021MG module is shown in Figure I-1.

These address lines are then buffered as shown in Diagram I-2 and form the inputs for the data break address (DADR); the low-order bit (DIAD11) is generated by the request-to-send signal and is shown in Diagram I-1.

The j -th position ($j=0, \dots, 13$) of the address is a 0 if there is a jumper to ground at that position and is a 1 otherwise. The W021MG address card is located in module position 1B09. If any of the three high-order positions (ADDR(0), ADDR(1), or ADDR(2)) is a 1, there must be extended memory capabilities on the PDP-8, and the eleventh or address extension cable must be provided.

Device Select Code (Diagram I-3)

The device select code is a two octal digit number which selects an external device during an input/output operation. The device code appears in positions 3 through 8 of the memory buffer (M.B.) during an IOT instruction, alerting the external device that it is being selected.

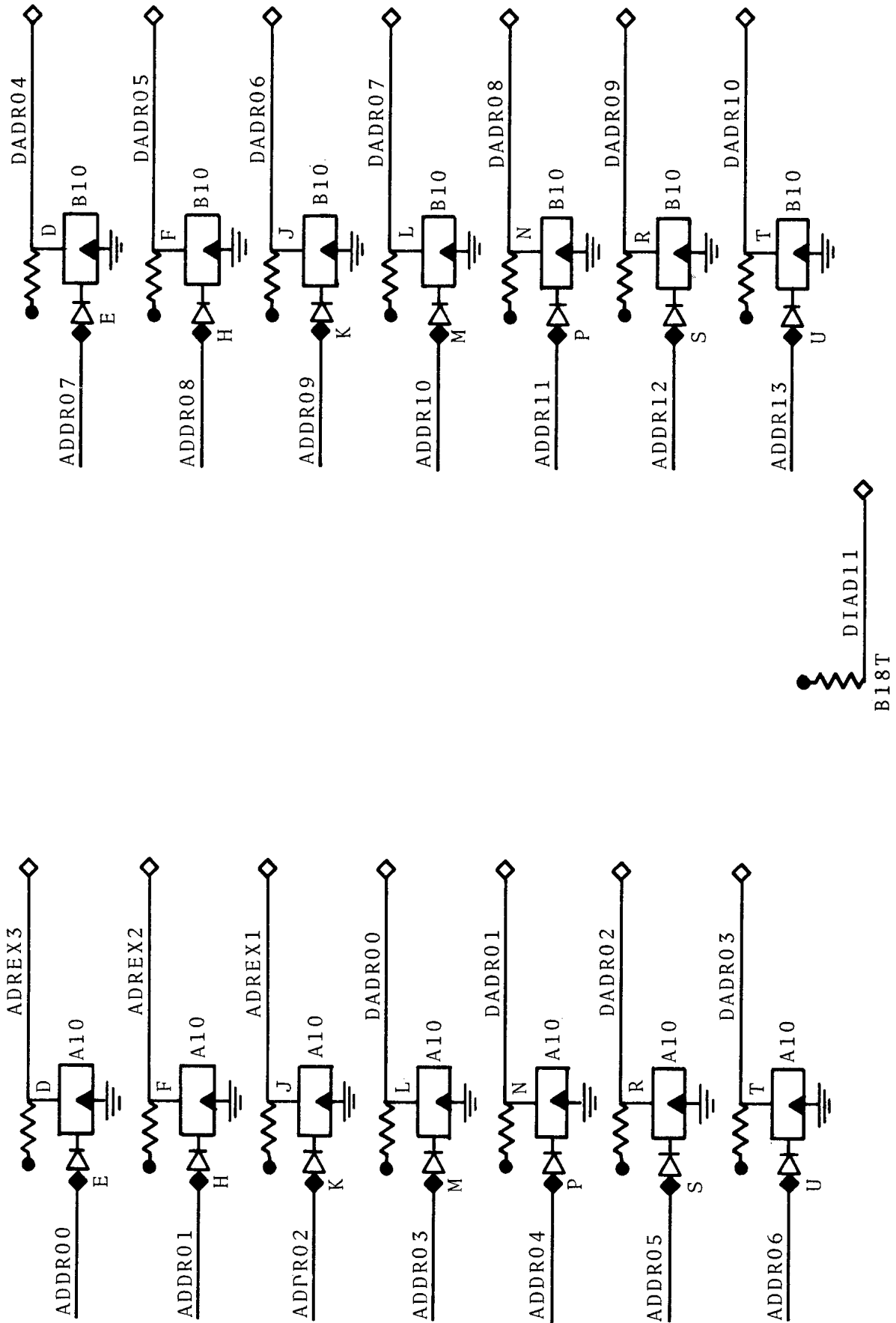


Diagram I-2. DATA-BREAK ADDRESS LINES

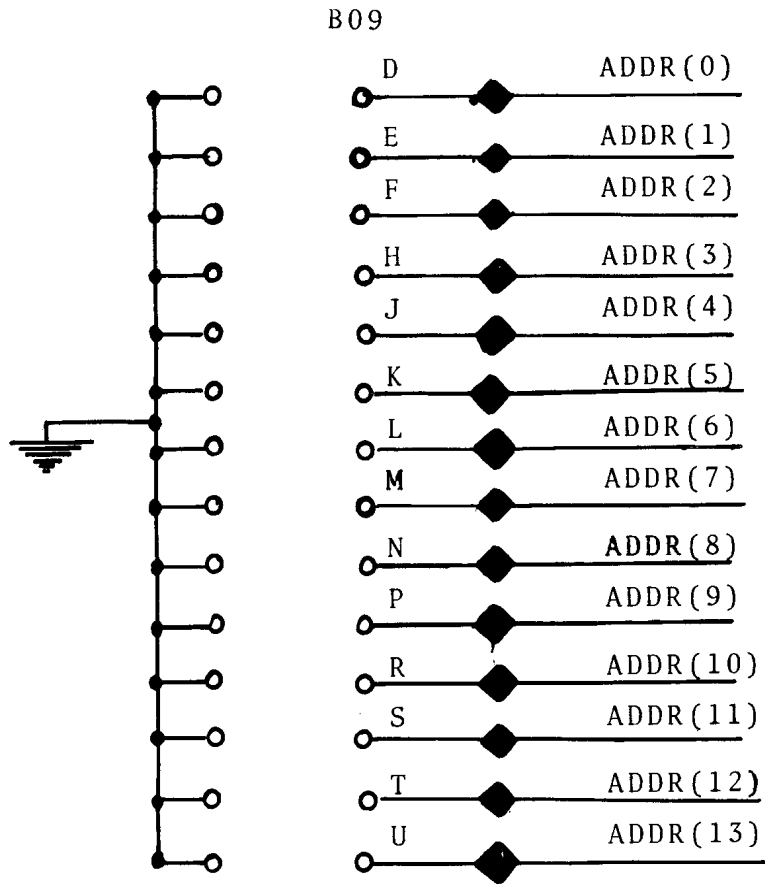


Figure I-1. W021MG Address Card.

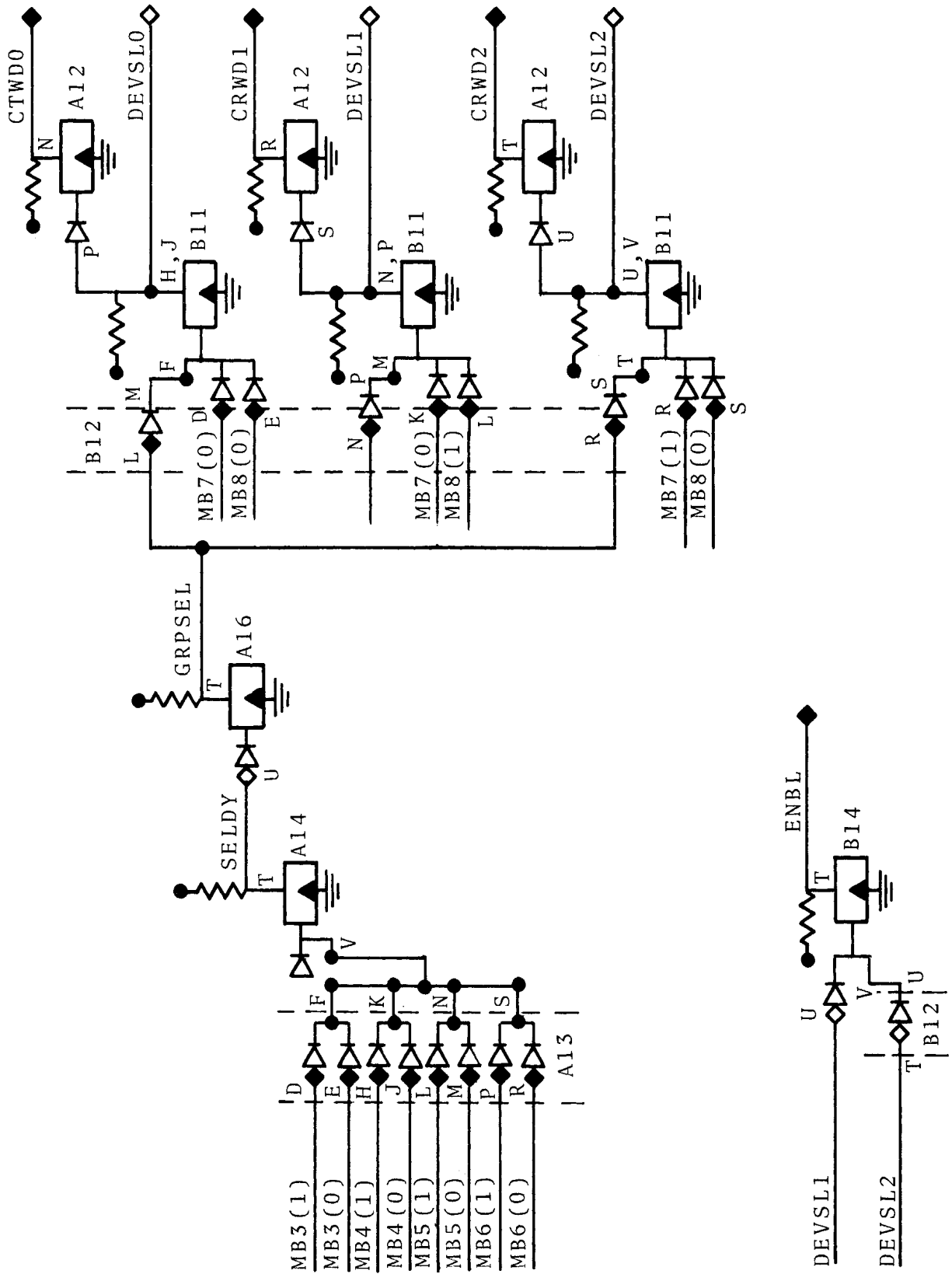


Diagram I-3. DEVICE DECODING

The 201A L.A. has associated with it three separate device codes as discussed above. In order to specify the three devices it is sufficient, because of the aforementioned requirements, to define only a four-bit number, which appears in positions 3-6 of the M.B. during an IOT instruction. This number must also be realized in the hardware, and this is accomplished via an R002 diode module found in position 1A13 and pictured at the far left of Diagram I-3.

Thus to specify the desired set of device codes the appropriate diodes are removed. For example, using the set 40, 41, 42 as before, the diodes connected to pins E, H, L, and P must be removed.

The remainder of Diagram I-3 shows the gating necessary to obtain the signals to identify each of the devices.

Device Selection Gating(Diagram I-4)

The gates shown in Diagram I-4 are located in Bay 2 and provide the signals to differentiate between Control Word 1 and Control Word 2 operation.

Interrupt Control (Diagram I-5)

Every time a character is transferred between the 201A L.A. and the PDP-8's memory, a character service flag (#SRSV) is set as described above.

This flag in turn sets the appropriate interrupt flag, Transmit (XINT) or Receive (RINT), which causes an interrupt request. If interrupts are enabled in the PDP-8, a program interrupt is generated. Via the appropriate IOT micro-instruction, the program can identify the device causing the interrupt. The SKIP signal will be generated, and a program skip forced if this IOT is executed. It is the program's responsibility to clear the interrupt after it is identified, and the remainder of the gates allow for this.

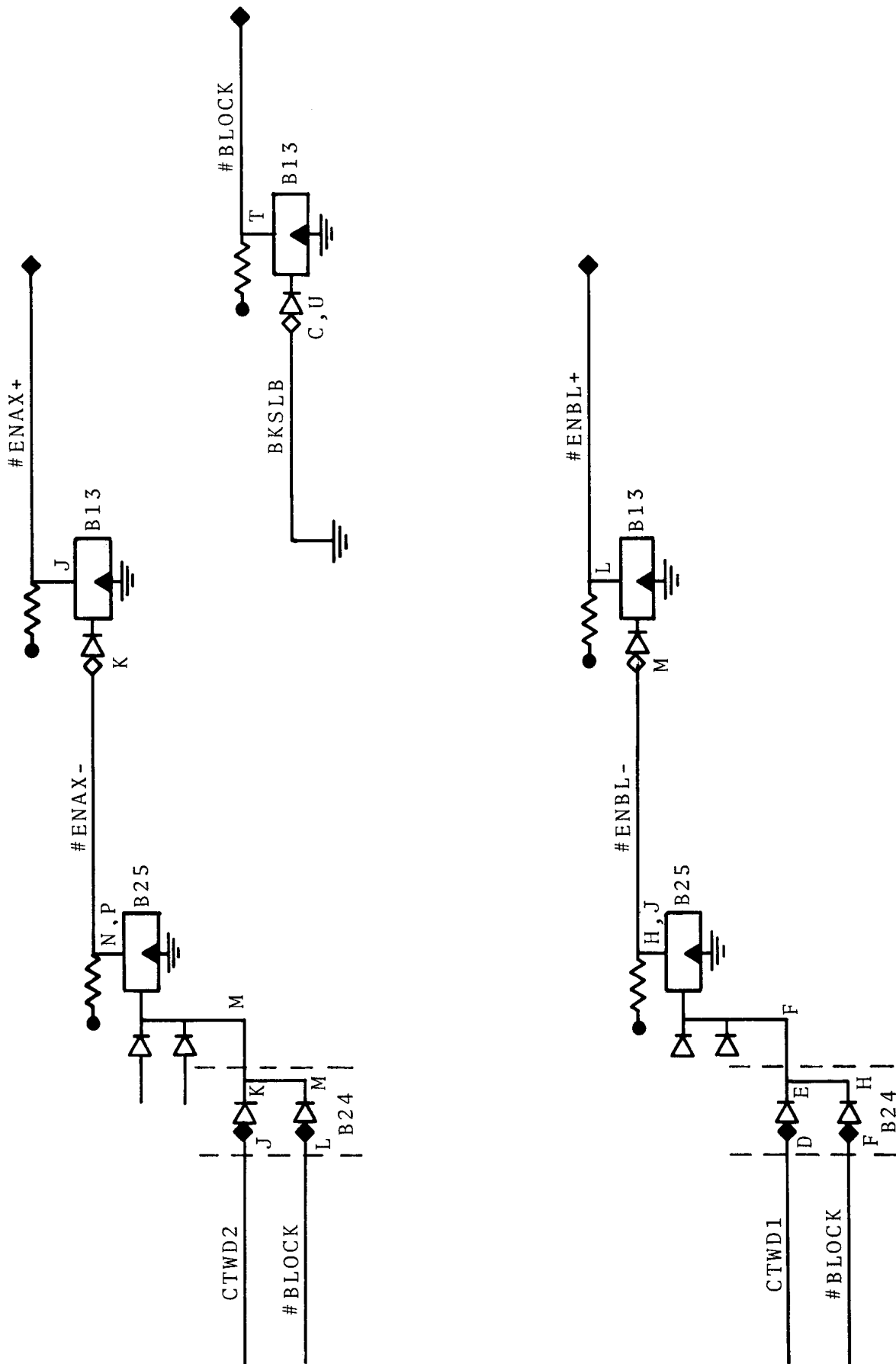


Diagram I-4. DEVICE SELECTION GATING

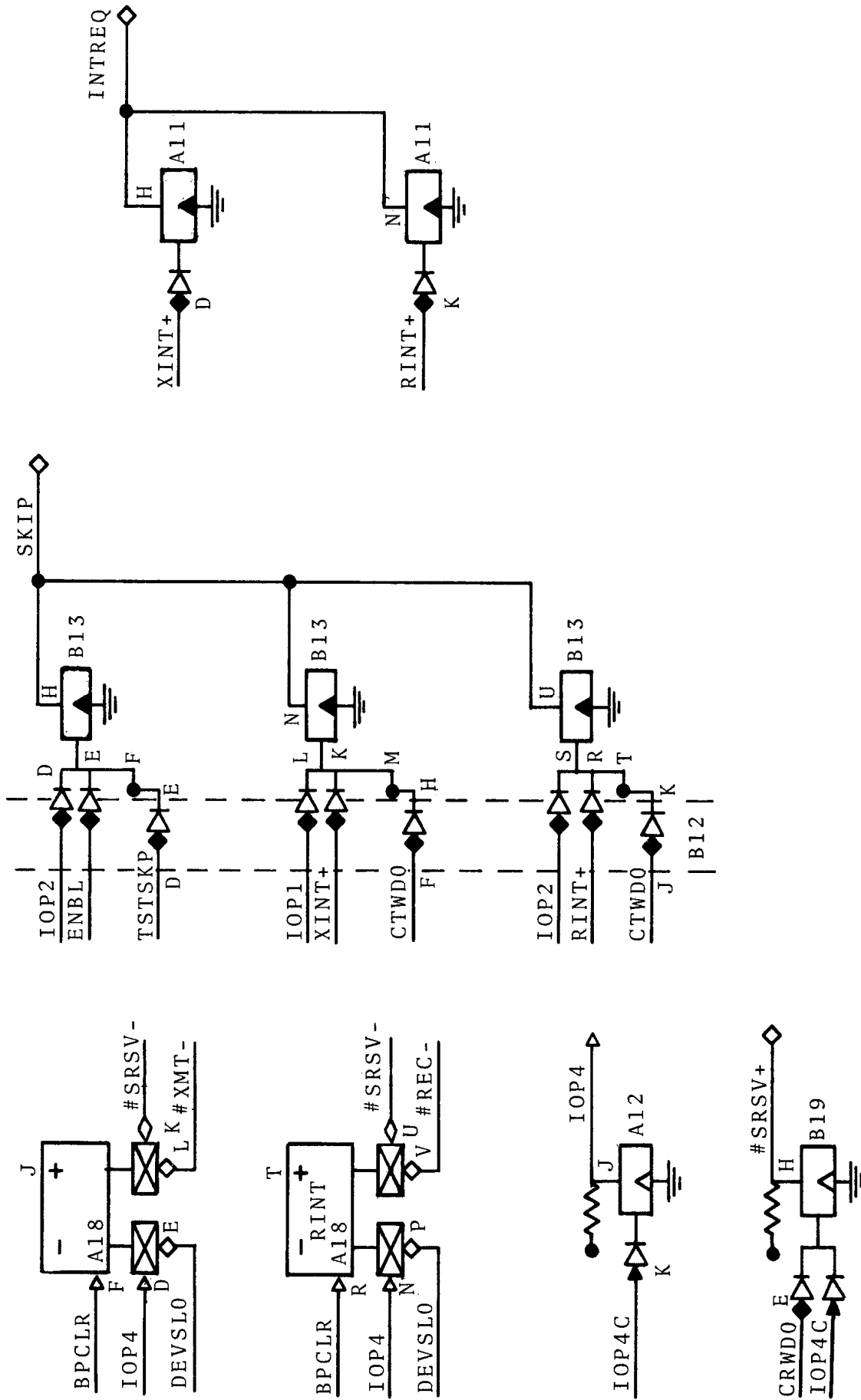


Diagram I-5. INTERRUPT CONTROL

Extended Accumulator Control (Diagram I-6)

In order to provide the IOT structure described in the Programming and Control Considerations section, the Extended Accumulator (EAC) buss was implemented. The full power of the EAC is not realized until multiple devices are using the buss, since it provides the mechanism for multiple inputs to the PDP-8 AC. Diagram I-6 shows the gating necessary to generate the SKIP signal when a skip under mask IOT is executed.

Accumulator Input Gating (Diagram I-7)

Diagram I-7 shows the buffers which gate the EAC buss onto the AC buss. For other devices to use the EAC buss they need only provide the appropriate input to the ENBL gate and the gates for the EAC buss.

Extended Accumulator Buffers (Diagram I-8)

Diagram I-8 shows a set of buffers necessary to accomplish the inversion to gate the EAC onto the AC. The clamped loads for the EAC buss are also indicated.

Data Bit Buffers (Diagram I-9)

Diagram I-9 shows the buffers used to provide isolation between the SDR register outputs and the data inputs on a data break into the PDP-8. There is no gating signal provided on these buffers since this is the only device using the data bit lines.

Miscellaneous Circuits (Diagram I-10)

Diagram I-10 is best described as the left-over circuits without a logical home.

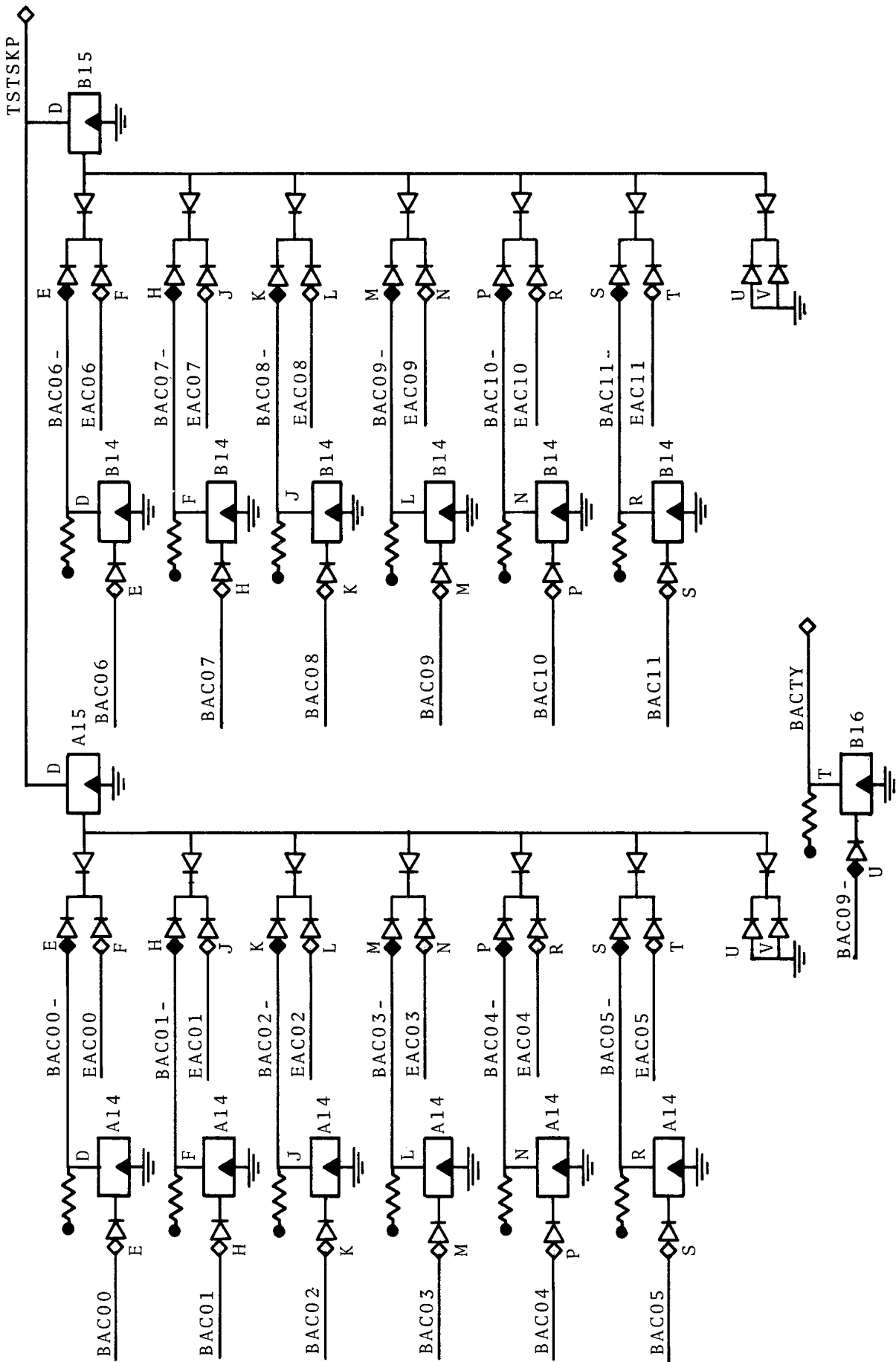


Diagram I-6. EXTENDED ACCUMULATOR CONTROL

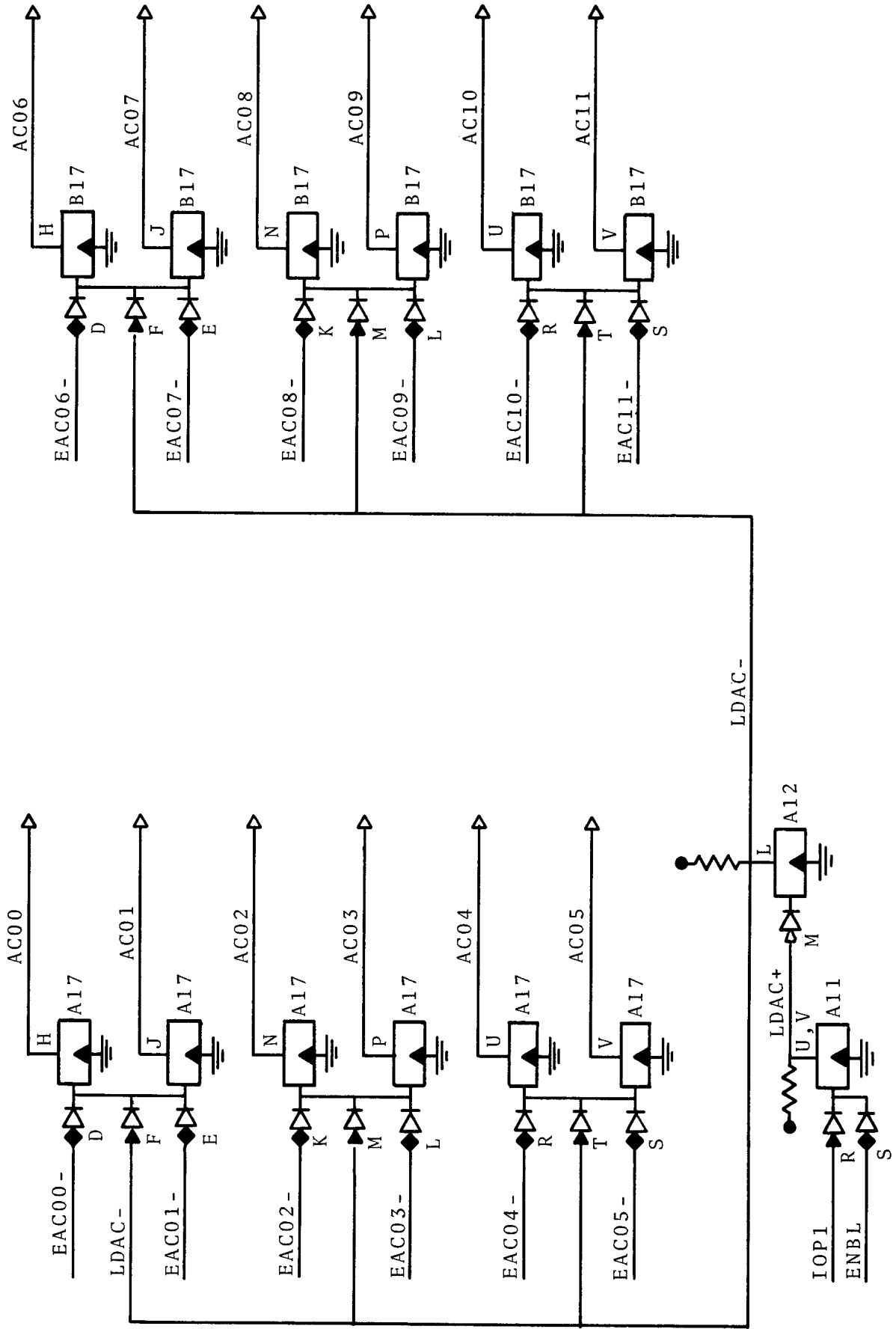


Diagram I-7. ACCUMULATOR INPUT GATING

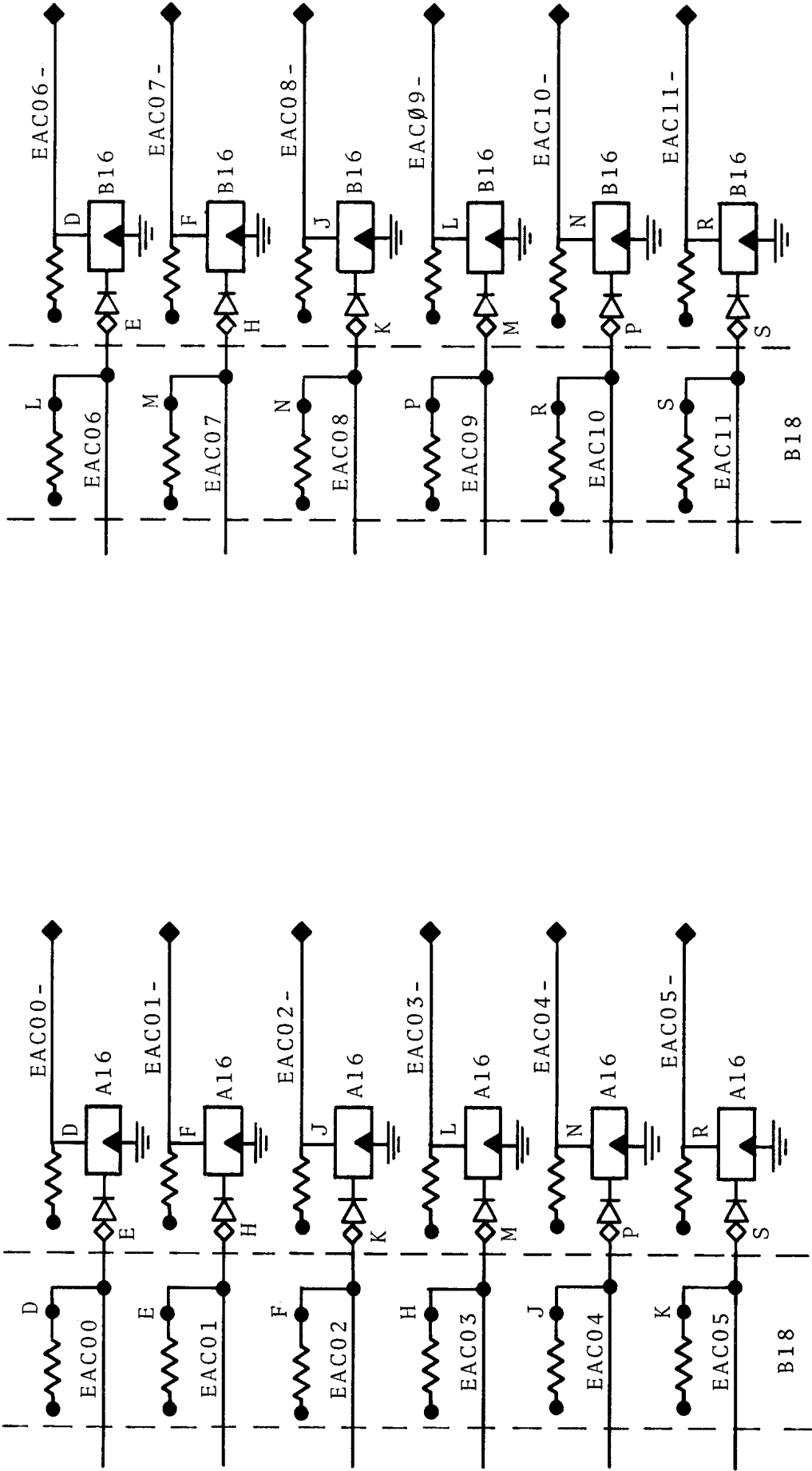


Diagram I-8. EXTENDED ACCUMULATOR BUFFERS

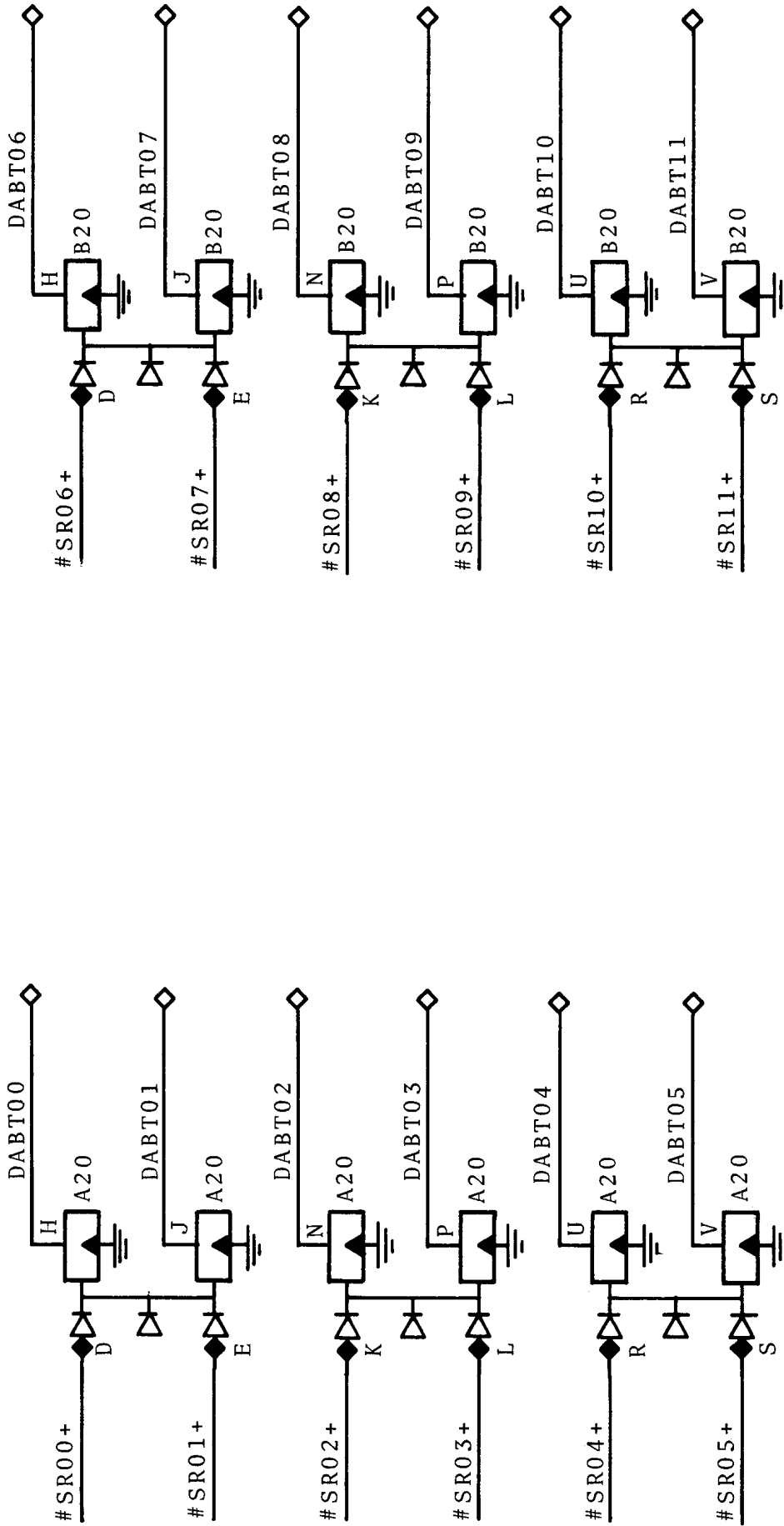


Diagram I-9. DATA BIT BUFFERS

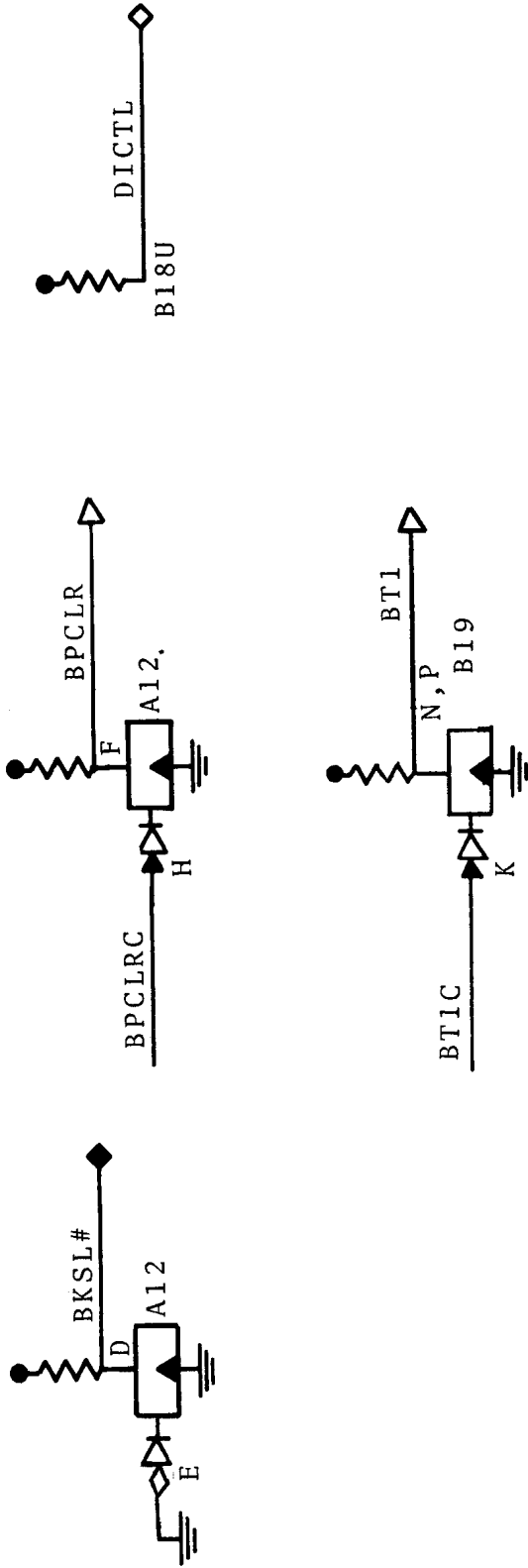


Diagram I-10. MISCELLANEOUS CIRCUITS

Cable Layout (Diagram I-11)

The input/output cables for the 201A L.A. are shown in Diagram I-11. The correspondences between the signal names, module positions, and pin connections for the 201A L.A. and the PDP-8 are given in Tables I-1 through I-7.

Module Utilization (Tables I-8 through I-11)

Tables I-8 through I-11 give the module utilization for a 201A L.A. In addition to the module utilization, a complete signal name map is also shown.

TABLE I-1

BUFFERED ACCUMULATOR OUTPUTS















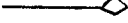









201A LINE ADAPTOR			PDP-8		
INTERFACE CONNECTION	SIGNAL NAME	LOGIC SYMBOL	LOGIC SYMBOL	SIGNAL NAME	INTERFACE CONNECTION
A01D, A02D	BAC00			BAC0	ME34D
A01E, A02E	BAC01			BAC1	ME34E
A01H, A02H	BAC02			BAC2	ME34H
A01K, A02K	BAC03			BAC3	ME34K
A01M, A02M	BAC04			BAC4	ME34M
A01P, A02P	BAC05			BAC5	ME34P
A01S, A02S	BAC06			BAC6	ME34S
A01T, A02T	BAC07			BAC7	ME34T
A01V, A02V	BAC08			BAC8	ME34V
B01D, B02D	BAC09			BAC9	MF34D
B01E, B02E	BAC10			BAC10	MF34E
B01H, B02H	BAC11			BAC11	MF34H

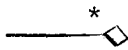
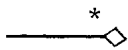
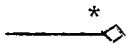
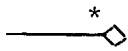
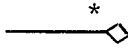
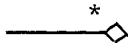
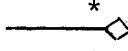
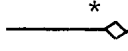
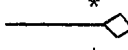
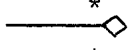
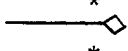
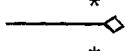


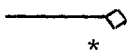
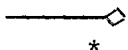
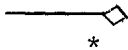
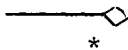
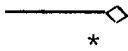
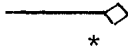
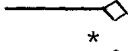
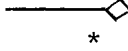
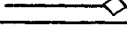
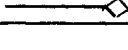
TABLE I-2

BUFFERED MEMORY BUFFER OUTPUT LINES

201A LINE ADAPTOR			PDP-8		
INTERFACE CONNECTION	SIGNAL NAME	LOGIC SYMBOL	LOGIC SYMBOL	SIGNAL NAME	INTERFACE CONNECTION
A03D, A04D	BMB00	—◇	—◇	BMB0(1)	ME35D
A03E, A04E	BMB01	—◇	—◇	BMB1(1)	ME35E
A03H, A04H	BMB02	—◇	—◇	BMB2(1)	ME35H
A03K, A04K	BMB03-	—◇	—◇	BMB3(0)	ME35K
A03M, A04M	BMB03	—◇	—◇	BMB3(1)	ME35M
A03P, A04P	BMB04-	—◇	—◇	BMB4(0)	ME35P
A03S, A04S	BMB04	—◇	—◇	BMB4(1)	ME35S
A03T, A04T	BMB05-	—◇	—◇	BMB5(0)	ME35T
A03V, A04V	BMB05	—◇	—◇	BMB5(1)	ME35V
B03D, B04D	BMB06-	—◇	—◇	BMB6(0)	MF35D
B03E, B04E	BMB06	—◇	—◇	BMB6(1)	MF35E
B03H, B04H	BMB07-	—◇	—◇	BMB7(0)	MF35H
B03K, B04K	BMB07	—◇	—◇	BMB7(1)	MF35K
B03M, B04M	BMB08-	—◇	—◇	BMB8(0)	MF35M
B03P, B04P	BMB08	—◇	—◇	BMB8(1)	MF35P
B03S, B04S	BMB09	—◇	—◇	BMB9(1)	MF35S
B03T, B04T	BMB10	—◇	—◇	BMB10(1)	MF35T
B03V, B04V	BMB11	—◇	—◇	BMB11(1)	MF35V

TABLE I-3

ACCUMULATOR INPUTS

201A LINE ADAPTOR			PDP-8		
INTERFACE CONNECTION	SIGNAL NAME	LOGIC SYMBOL	LOGIC SYMBOL	SIGNAL NAME	INTERFACE CONNECTION
A05D, A06D	AC00			AC0	PE2D
A05E, A06E	AC01			AC1	PE2E
A05H, A06H	AC02			AC2	PE2H
A05K, A06K	AC03			AC3	PE2K
A05M, A06M	AC04			AC4	PE2M
A05P, A06P	AC05			AC5	PE2P
A05S, A06S	AC06			AC6	PE2S
A05T, A06T	AC07			AC7	PE2T
A05V, A06V	AC08			AC8	PE2V
B05D, B06D	AC09			AC9	PF2D
B05E, B06E	AC10			AC10	PF2E
B05H, B06H	AC11			AC11	PF2H

*Note: Collector of Grounded-Emitter Transistor

TABLE I-4
PROGRAMMED INPUT/OUTPUT CONTROL

201A LINE ADAPTOR			PDP-8		
INTERFACE CONNECTION	SIGNAL NAME	LOGIC SYMBOL	LOGIC SYMBOL	SIGNAL NAME	INTERFACE CONNECTION
B05M, B06M	INTREQ	*1 —◇	*1 —◇	INTERRUPT REQUEST	PF2M
B05K, B06K	SKIP	*1 —◇	*1 —◇	SKIP	PF2K
B01K, B02K	IOP1	—▶	—▶	IOP1	MF34K
B01M, B02M	IOP2	—▶	—▶	IOP2	MF34M
B01P, B02P	IOP4C	—▶	—▶	IOP4	MF34P

*Note: Collector of Grounded-Emitter Transistor

TABLE I - 5
DATA-BREAK ADDRESS LINES































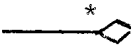
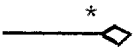

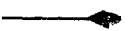


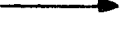




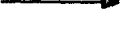


201A LINE ADAPTOR			PDP-8		
INTERFACE CONNECTION	SIGNAL NAME	LOGIC SYMBOL	LOGIC SYMBOL	SIGNAL NAME	INTERFACE CONNECTION
A09H	ADREX3			ADDR EXT 3	ME30H
A09E	ADREX2			ADDR EXT 2	ME30E
A09D	ADREX1			ADDR EXT 1	ME30D
A07D	DADR00			DATA ADDR 0 (1)	PE3D
A07E	DADR01			DATA ADDR 1 (1)	PE3E
A07H	DADR02			DATA ADDR 2 (1)	PE3H
A07K	DADR03			DATA ADDR 3 (1)	PE3K
A07M	DADR04			DATA ADDR 4 (1)	PE3M
A07P	DADR05			DATA ADDR 5 (1)	PE3P
A07S	DADR06			DATA ADDR 6 (1)	PE3S
A07T	DADR07			DATA ADDR 7 (1)	PE3T
A07V	DADR08			DATA ADDR 8 (1)	PE3V
B07D	DADR09			DATA ADDR 9 (1)	PF3D
B07E	DADR10			DATA ADDR 10 (1)	PF3E
B07H	DADR11			DATA ADDR 11 (1)	PF3H

TABLE I - 6
DATA-BREAK INPUT LINES

201A LINE ADAPTOR				PDP - 8	
INTERFACE CONNECTION	SIGNAL NAME	LOGIC SYMBOL	LOGIC SYMBOL	SIGNAL NAME	INTERFACE CONNECTION
A08D	DABT00			DATA - BIT 0	PE4D
A08E	DABT01			DATA - BIT 1	PE4E
A08H	DABT02			DATA - BIT 2	PE4H
A08K	DABT03			DATA - BIT 3	PE4K
A08M	DABT04			DATA - BIT 4	PE4M
A08P	DABT05			DATA - BIT 5	PE4P
A08S	DABT06			DATA - BIT 6	PE4S
A08T	DABT07			DATA - BIT 7	PE4T
A08V	DABT08			DATA - BIT 8	PE4V
B08D	DABT09			DATA - BIT 9	PF4D
B08E	DABT10			DATA - BIT 10	PF4E
B08H	DABT11			DATA - BIT 11	PF4H

TABLE I-7
DATA-BREAK CONTROL SIGNALS

201A LINE ADAPTOR			PDP-8		
INTERFACE CONNECTION	SIGNAL NAME	LOGIC SYMBOL	LOGIC SYMBOL	SIGNAL NAME	INTERFACE CONNECTION
B07K	BKRQ#			BREAK REQUEST	PF3K
B07M	DICTL			TRANSFER DIRECTION	PF3M
B07P	BBREAK			B BREAK	PF3P
B07S	ADDACC			ADDRESS ACCEPTED	PF3S
B01S, B02S	BT1C			BT1	MF34S
B01T, B02T	BR2A			BT2A	MF34T
B01V, B02V	BPCLRC			B POWER CLEAR	MF34V

*Note: Collector of a Grounded-Emitter Transistor.

PANEL 1 . . . COMMON SECTION

	A01	A02	A03	A04	AC5	AC6	A07	AC8	AC9	A10	A11	A12	A13	A14	A15	A16
A	W021	W021	W021	W021	W021	W021	W021	W021	W021	W021	R107	R111	R107	R107	R141	R107
B																
C																
D	BAC00	BAC00	BMB00	BMB00	ACC0	ACC0	DADRC0	CABTC0	ADREX1	ADREX3	XINT+	GNDAL12	BMSL#	BAC00-	BAC00-	TSTSKP
E	BAC01	BAC01	BMB01	BMB01	ACC1	ACC1	DADRC1	CABTC1	ADREX2	ADREX0		GNDAL12	BMSL#	BAC00	BAC00-	EAC00-
F	BAC02	BAC02	BMB02	BMB02	ACC2	ACC2	DADRC2	CABTC2	ADREX1	ADREX0		BPCLK	SELNC	BAC01-	EAC00	EAC01-
G	BAC03	BAC03	BMB03-	BMB03-	ACC3	ACC3	DADRC3	CABTC3	ADREX1	ADREX0		BPCLRC	BAC04-	BAC01	BAC01-	EAC01
H	BAC04	BAC04	BMB04	BMB04	ACC4	ACC4	DADRC4	CABTC4	ADREX2	ADREX0		TOP4	BAC04-	BAC01	BAC01-	EAC01
I	BAC05	BAC05	BMB05-	BMB05-	ACC5	ACC5	DADRC5	CABTC5	ADREX2	ADREX0		LDAC-	BAC05-	BAC02	BAC02-	EAC02-
J	BAC06	BAC06	BMB06	BMB06	ACC6	ACC6	DADRC6	CABTC6	ADREX3	ADREX0		LDAC-	BAC05-	BAC03-	EAC02	EAC03-
K	BAC07	BAC07	BMB07-	BMB07-	ACC7	ACC7	DADRC7	CABTC7	ADREX3	ADREX0		LDAC+	BAC05	BAC03-	EAC03-	EAC03-
L	BAC08	BAC08	BMB08	BMB08	ACC8	ACC8	DADRC8	CABTC8	ADREX3	ADREX0		LDAC+	BAC05	BAC03-	EAC03-	EAC03-
M																
N																
O																
P																
Q																
R																
S																
T																
U																
V																

	B01	B02	B03	B04	B05	B06	B07	B08	B09	B10	B11	B12	B13	B14	B15	B16
A	W021	W021	W021	W021	W021	W021	W021	W021	W021	W021	R107	R001	R111	R107	R141	R107
B																
C																
D	BAC09	BAC09	BMB06-	BMB06-	ACC9	ACC9	DADRC9	CABTC9	ADDR00	DADR04	BMB07	TSTSKP	TOP2	BAC06-	BAC06-	EAC06-
E	BAC10	BAC10	BMB06	BMB06	ACC10	ACC10	DADRC10	CABTC10	ADDR01	ADDR07	BMB08	SKIP1	ENBL	BAC06	BAC06-	EAC06
F	BAC11	BAC11	BMB07-	BMB07-	ACC11	ACC11	DIADR11	CABTC11	ADDR02	DADR05	DEVND0	CTWDO	SKIPI	BAC07-	EAC06	EAC07-
G	BAC12	BAC12	BMB07	BMB07	ACC12	ACC12	DIADR12	CABTC12	ADDR03	ADDR08	DEVSL0	CTWDO	SKIPI	BAC07	BAC07-	EAC07
H	BAC13	BAC13	BMB08	BMB08	ACC13	ACC13	DIADR13	CABTC13	ADDR04	DADR06	DEVSL0	CTWDO	SKIPI	BAC08-	EAC07	EAC08-
I	BAC14	BAC14	BMB08	BMB08	ACC14	ACC14	DIADR14	CABTC14	ADDR05	DADR09	BMB07	SKIP3	XINT+	BAC08	BAC08-	EAC08
J	BAC15	BAC15	BMB09	BMB09	ACC15	ACC15	DIADR15	CABTC15	ADDR06	DADR07	BMB08-	GRPSEL	TOP1	BAC05-	EAC08	EAC09-
K	BAC16	BAC16	BMB09	BMB09	ACC16	ACC16	DIADR16	CABTC16	ADDR07	ADDR10	DEVND1	DEVND0	SKIP2	BAC09	BAC09-	EAC09
L	BAC17	BAC17	BMB10	BMB10	ACC17	ACC17	DIADR17	CABTC17	ADDR08	DADR08	DEVSL1	GRPSEL	SKIPI	BAC09	BAC09-	EAC09
M																
N																
O																
P																
Q																
R																
S																
T																
U																
V																

TABLE I-8 .

PANEL 1 . . . COMMON SECTION

	A17	A18	A19	A20	A21	A22	A23	A24	A25	A26	A27	A28	A29	A30	A31	A32
	R123	R202			R123							W050S				
A																
B																
C																
D	EAC00-	IOP4		#SR00+								#XMT+				
E	EAC01-	DEVSLC		#SR01+								#REC+				
F	LDAC-	BPCLR										#SRSV+				
H	AC00			DABT00								#DLST+				
J	AC01	XINT+		DABT01								#PAR+				
K	EAC02-	#SRSV-		#SR02+								#EBPC+				
L	EAC03-	#XMT-		#SR03+								#IFMD+				
M	LDAC-											#STRDY				
N	AC02	IOP4		DABT02								#TMRD+				
P	AC03	DEVSLC		DABT03								#RING				
R	EAC04-	BPCLR		#SR04+								#CARDT				
S	EAC05-			#SR05+												
T	LDAC-	RINT+														
U	AC04	#SRSV-		DABT04												
V	AC05	#REC-		DABT05												
	B17	B18	B19	B20	B21	B22	B23	B24	B25	B26	B27	B28	B29	B30	B31	B32
	R123	W002	R111	R123												
A																
B																
C																
D	EAC06-	EAC00	IOP4C	#SR06+												
E	EAC07-	EAC01	GTWDC	#SR07+												
F	LDAC-	EAC02														
H	AC06	EAC03	#SRSV+	DABT06												
J	AC07	EAC04		DABT07												
K	EAC08-	EAC05	BTIC	#SR08+												
L	EAC09-	EAC06		#SR09+												
M	LDAC-	EAC07														
N	AC08	EAC08	BTI	DABT08												
P	AC09	EAC09	BTI	DABT09												
R	EAC10-	EAC10		#SR10+												
S	EAC11-	EAC11		#SR11+												
T	LDAC-	DIAC11														
U	AC10	DICTL		DABT10												
V	AC11			DABT11												

TABLE I-9

PANEL 2 ... PORT 0/LINE ADAPTOR 1

	A01	A02	A03	A04	A05	A06	A07	A08	A09	A10	A11	A12	A13	A14	A15	A16
A	W201C	E1AR	R111	W501	R111	R001	R302	R111	R201	R205	R205	R205	R205	R205	R201	R205
B																
C																
D	#GND02	#GND02	#RD+	#SRCK	#SRCK	#REC-	#RECE-	#GND06	#SR00+	#SR02+	#SR02+	#SR04+	#SR06+	#SR08+	#SR11+	#GND14
E	#RDR	#RINGE	#PEC+	#LINE+	#DTND1	#REC-	#QSC+	#GND06	#SR00-	#MBSR	#MBSR	#MBSR	#MBSR	#MBSR	#SK11-	#SHIFT
F	#RSB	#CTND1	#REC-	#CTND1	#REC-	#GND06	#REC+	#RD+	#SR01-	#SR03-	#SR05-	#SR07-	#SR09-	#SR10+	#SR10+	#SDBF+
G	#CSDR	#RING	#RD-	#CTND2	#REC-	#GND06	#REC+	#RD+	#SR01-	#SR03-	#SR05-	#SR07-	#SR09-	#SR10+	#SR10+	#GND14
H	#SPDB	#RING	#RD-	#CTND2	#REC-	#GND06	#REC+	#RD+	#SR01-	#SR03-	#SR05-	#SR07-	#SR09-	#SR10+	#SR10+	#GND14
I	#TRDY3	#GND02	#RD-	#CTND2	#REC-	#GND06	#REC+	#RD+	#SR01-	#SR03-	#SR05-	#SR07-	#SR09-	#SR10+	#SR10+	#GND14
J	#TRDY3	#GND02	#RD-	#CTND2	#REC-	#GND06	#REC+	#RD+	#SR01-	#SR03-	#SR05-	#SR07-	#SR09-	#SR10+	#SR10+	#GND14
K	#TRDY3	#GND02	#RD-	#CTND2	#REC-	#GND06	#REC+	#RD+	#SR01-	#SR03-	#SR05-	#SR07-	#SR09-	#SR10+	#SR10+	#GND14
L	#TRDY3	#GND02	#RD-	#CTND2	#REC-	#GND06	#REC+	#RD+	#SR01-	#SR03-	#SR05-	#SR07-	#SR09-	#SR10+	#SR10+	#GND14
M	#CDETB	#CS+	#XTM+	#LINE-	#XTM+	#REC-	#XMT+	#RFX	#SR00-	#MBSR	#MBSR	#MBSR	#MBSR	#MBSR	#SK11-	#FRZE
N	#CDETB	#CS+	#XTM+	#LINE-	#XTM+	#REC-	#XMT+	#RFX	#SR00-	#MBSR	#MBSR	#MBSR	#MBSR	#MBSR	#SK11-	#FRZE
O	#CDETB	#CS+	#XTM+	#LINE-	#XTM+	#REC-	#XMT+	#RFX	#SR00-	#MBSR	#MBSR	#MBSR	#MBSR	#MBSR	#SK11-	#FRZE
P	#CDETB	#CS+	#XTM+	#LINE-	#XTM+	#REC-	#XMT+	#RFX	#SR00-	#MBSR	#MBSR	#MBSR	#MBSR	#MBSR	#SK11-	#FRZE
Q	#CDETB	#CS+	#XTM+	#LINE-	#XTM+	#REC-	#XMT+	#RFX	#SR00-	#MBSR	#MBSR	#MBSR	#MBSR	#MBSR	#SK11-	#FRZE
R	#CDETB	#CS+	#XTM+	#LINE-	#XTM+	#REC-	#XMT+	#RFX	#SR00-	#MBSR	#MBSR	#MBSR	#MBSR	#MBSR	#SK11-	#FRZE
S	#CDETB	#CS+	#XTM+	#LINE-	#XTM+	#REC-	#XMT+	#RFX	#SR00-	#MBSR	#MBSR	#MBSR	#MBSR	#MBSR	#SK11-	#FRZE
T	#CDETB	#CS+	#XTM+	#LINE-	#XTM+	#REC-	#XMT+	#RFX	#SR00-	#MBSR	#MBSR	#MBSR	#MBSR	#MBSR	#SK11-	#FRZE
U	#STRDY	#DELAY	#RS1	#RSND	#RSND	#REC-	#XMT+	#RFX	#SR01-	#SR03-	#SR05-	#SR07-	#SR09-	#SR10+	#SR10+	#EP2
V	#STRDY	#DELAY	#RS1	#RSND	#RSND	#REC-	#XMT+	#RFX	#SR01-	#SR03-	#SR05-	#SR07-	#SR09-	#SR10+	#SR10+	#ZROSR

	B01	B02	B03	B04	B05	B06	B07	B08	B09	B10	B11	B12	B13	B14	B15	B16
A	W502	E1AR	B03	W501	B04	B05	B06	B07	B08	B09	B10	B11	B12	B13	B14	B15
B																
C																
D																
E																
F																
G																
H																
I																
J																
K																
L																
M																
N																
O																
P																
Q																
R																
S																
T																
U																
V																

	W502 <th>E1AR <th>B03 <th>W501 <th>B04 <th>B05 <th>B06 <th>B07 <th>B08 <th>B09 <th>B10 <th>B11 <th>B12 <th>B13 <th>B14 <th>B15 <th>B16</th> </th></th></th></th></th></th></th></th></th></th></th></th></th></th></th>	E1AR <th>B03 <th>W501 <th>B04 <th>B05 <th>B06 <th>B07 <th>B08 <th>B09 <th>B10 <th>B11 <th>B12 <th>B13 <th>B14 <th>B15 <th>B16</th> </th></th></th></th></th></th></th></th></th></th></th></th></th></th>	B03 <th>W501 <th>B04 <th>B05 <th>B06 <th>B07 <th>B08 <th>B09 <th>B10 <th>B11 <th>B12 <th>B13 <th>B14 <th>B15 <th>B16</th> </th></th></th></th></th></th></th></th></th></th></th></th></th>	W501 <th>B04 <th>B05 <th>B06 <th>B07 <th>B08 <th>B09 <th>B10 <th>B11 <th>B12 <th>B13 <th>B14 <th>B15 <th>B16</th> </th></th></th></th></th></th></th></th></th></th></th></th>	B04 <th>B05 <th>B06 <th>B07 <th>B08 <th>B09 <th>B10 <th>B11 <th>B12 <th>B13 <th>B14 <th>B15 <th>B16</th> </th></th></th></th></th></th></th></th></th></th></th>	B05 <th>B06 <th>B07 <th>B08 <th>B09 <th>B10 <th>B11 <th>B12 <th>B13 <th>B14 <th>B15 <th>B16</th> </th></th></th></th></th></th></th></th></th></th>	B06 <th>B07 <th>B08 <th>B09 <th>B10 <th>B11 <th>B12 <th>B13 <th>B14 <th>B15 <th>B16</th> </th></th></th></th></th></th></th></th></th>	B07 <th>B08 <th>B09 <th>B10 <th>B11 <th>B12 <th>B13 <th>B14 <th>B15 <th>B16</th> </th></th></th></th></th></th></th></th>	B08 <th>B09 <th>B10 <th>B11 <th>B12 <th>B13 <th>B14 <th>B15 <th>B16</th> </th></th></th></th></th></th></th>	B09 <th>B10 <th>B11 <th>B12 <th>B13 <th>B14 <th>B15 <th>B16</th> </th></th></th></th></th></th>	B10 <th>B11 <th>B12 <th>B13 <th>B14 <th>B15 <th>B16</th> </th></th></th></th></th>	B11 <th>B12 <th>B13 <th>B14 <th>B15 <th>B16</th> </th></th></th></th>	B12 <th>B13 <th>B14 <th>B15 <th>B16</th> </th></th></th>	B13 <th>B14 <th>B15 <th>B16</th> </th></th>	B14 <th>B15 <th>B16</th> </th>	B15 <th>B16</th>	B16
A																	
B																	
C																	
D																	
E																	
F																	
G																	
H																	
I																	
J																	
K																	
L																	
M																	
N																	
O																	
P																	
Q																	
R																	
S																	
T																	
U																	
V																	

TABLE I-10.

PANEL 2 ... PORT O/LINE ADAPICK 1

	A17	A18	A19	A20	A21	A22	A23	A24	A25	A26	A27	A28	A29	A30	A31	A32
A	R202															
B																
C																
D	#FR3+	#INVMK	#ALAC	#START	#GND19	#GND20	#INVMK	#INVMK	#STCK	#BRKDN	#SRV+	#EBPC+		#CFR3+		
E	#DY-	BAC07	#GND19	#GND20	#PWCLR	#PWCLR	#PWCLR	#PWCLR	#CLSD-	#RQSD-	#DLST+	#IFMD+		#CFR2+		
F	#REC-	#XMT+	#XMT+	#XMT+	#PAR+	#EBPC+	#PAR+	#PAR+	#PAR+	#RSI	EAC06	EAC06		#ENAX+		
H	#LINE+	#PWCLR	#PWCLR	#PWCLR	BAC06	BAC06	BAC06	BAC06	#CS-	#RQSD+	EAC01	EAC07		EAC08		
J	#CLUCK	#IFMD+	#PKRC+	#SVC-	#REC-	#XMT+	#XMT+	#XMT+	#XMT+	#XTRC-	#PAR+	#STRCY		EAC09		
K	#LINE+	#IFMD-	#IFMD-	#SVC-	#REC-	#XMT+	#XMT+	#XMT+	#XMT+	#XTRC+	#PAR+	#STRCY		EAC10		
L	#FRZF	#INVMK	#FR3+	#REC-	#XMT+	#XMT+	#XMT+	#XMT+	#XMT+	#XTRC+	#PAR+	#STRCY		EAC11		
M	#FR3+	BAC07	#IFMD-	#XMT+	#XMT+	#XMT+	#XMT+	#XMT+	#XMT+	#XTRC+	#PAR+	#STRCY		#RQSD+		
N	#PATY-	#CLUCK	#START	#XMT+	#XMT+	#XMT+	#XMT+	#XMT+	#XMT+	#XTRC-	#PAR+	#STRCY		#RQSD+		
P	#PATY+	#DTSY-	#XMT-	#REC+	BACTY	BACTY	BACTY	BACTY	BACTY	BACTY	BACTY	BACTY		#RQSD+		
R														HKSL#		
S														DIAD11		
T	#FR3+													DICTL		
U	#PATY+															
V																

	B17	B18	B19	B20	B21	B22	B23	B24	B25	B26	B27	B28	B29	B30	B31	B32
A																
B																
C																
D																
E																
F																
H																
J																
K																
L																
M																
N																
P																
R																
S																
T																
U																
V																

TABLE I-11.

APPENDIX II

201A LINE ADAPTOR INTERFACE
FOR USE ON
THE DATA CONCENTRATOR

APPENDIX II

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APPENDIX II

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201A LINE ADAPTOR INTERFACE
FOR USE ON
THE DATA CONCENTRATOR

The remainder of the logic and details of the 201A communication adaptors used on the Data Concentrator are presented in this Appendix. Figure II-1 shows in block form the general organization of the Data Concentrator, to the extent that it concerns the 201A line adaptors. The control of AC transfers and interrupts for the PDP-8 is handled by the scanner. In order to address a line adaptor (for the purposes here, a 201A line adaptor) the scan address register must be loaded with what corresponds to the line adaptor's logical address. This logical address, in reality, is the core address of its receive or transmit buffer. When the scanner is interrupted by a line adaptor, it in turn interrupts the PDP-8 with the scan address register set to the receive or transmit buffer address depending on the type of interrupt. The IOT structure is the same as described for the basic 201A line adaptor once the scan address register is pointed to the line adaptor.

The normal operation for the scanner is to scan, in turn, each of the 64 full-duplex lines looking for an interrupt. When an interrupt is found, the scanner is stopped and a PDP-8 interrupt is generated. After servicing the scanner interrupt (indirectly a line adaptor interrupt), the scanner is restarted.

The multiplexor is a buss-type multiplexor where the device presently selected gates its address and data information onto common busses. A device requests a data-break cycle by pulling to ground its break request line, and the data break is granted when its select line goes to -3v. In order to realize this buss concept, certain of the normal PDP-8 signals are electrically inverted at the multiplexor interface.

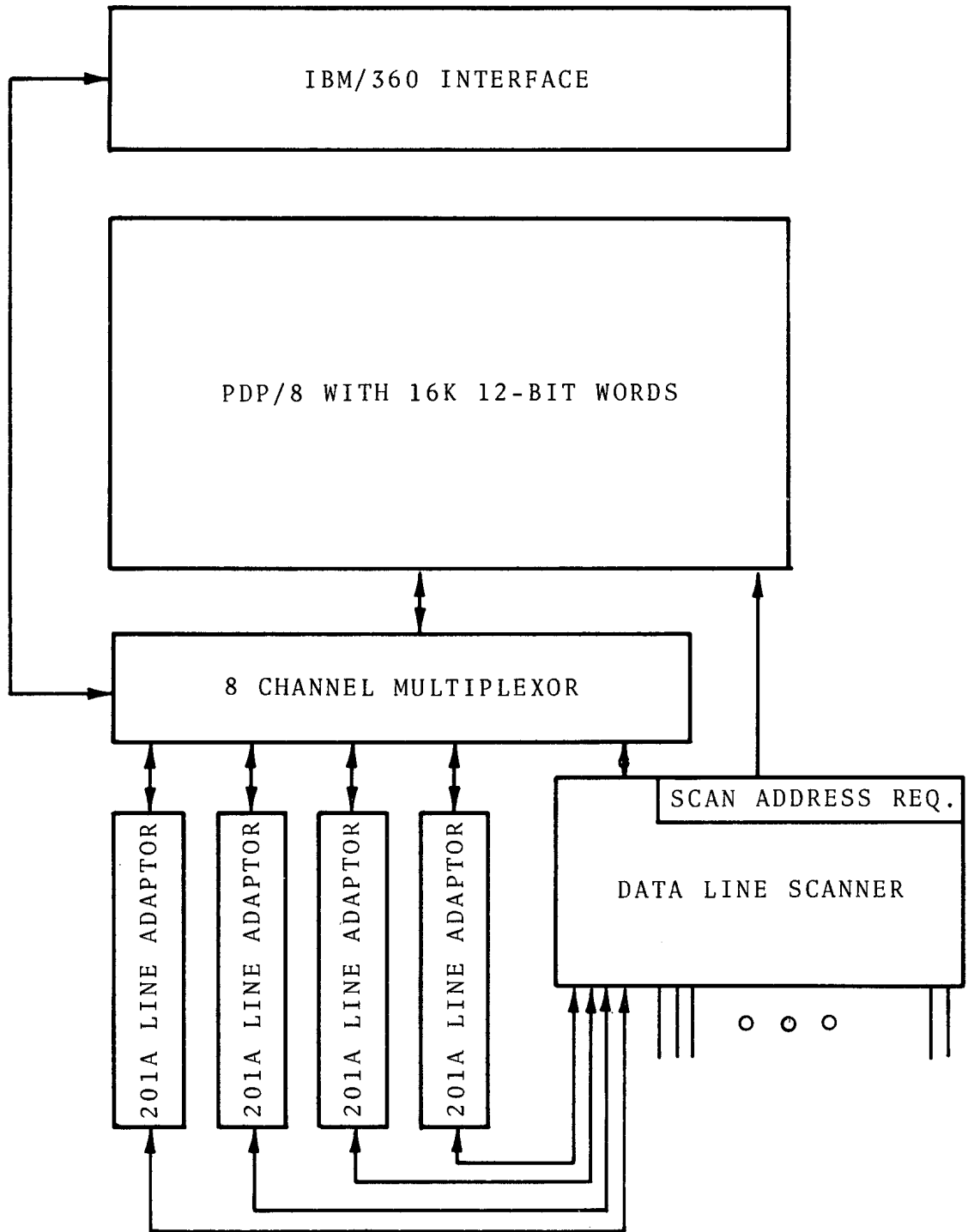


Figure II-1. ORGANIZATION OF THE DATA CONCENTRATOR

There are four 201A line adaptors on the Data Concentrator. They all have a common control section which, in the context of Figure 1, is the PDP-8/201A line adaptor interface. The common section is Bay 1 of the complex with Bays 2-5, representing the four 201A line adaptors. The individual signal names in the 201A line adaptor contain a # sign which is replaced by a 1, 2, 3, or 4 in the particular line adaptor. The common signals are distinguished by the absence of a # sign. Unless otherwise noted, the logic shown in the diagrams in this Appendix is realized in Bay 1.

Data-Break Control (Diagram II-1)

By setting the #BKRQ flip-flop, the line adaptor signals the PDP-8 (through the multiplexor) that a data transfer is desired to or from PDP-8 core. The multiplexor responds with the BKAC# signal when the data-break cycle is granted. The direction of the transfer is specified by the DICTL signal. When the PDP-8 enters the break state, the address is loaded into the memory address register and an address accepted pulse is generated by the PDP-8. At this time, the break request signal must be dropped by the interface. During the break state, as indicated by the logical-and of BBREAK and BKSL#, the BT1 pulse is used to generate a #BRKDN pulse which strobes the contents of the designated memory location from the buffered memory buffer register into the SDR register. The PDP-8 will also strobe the data-break input lines (DABT) into memory at this time in the case that the transfer direction is into core. The break request signal is generated each time the frame counter overflows when in the text state, and when the interface first enters the transmit state to fetch the first character to be transmitted. All of the logic shown in Diagram II-1 is in the individual line adaptor bay.

Data-Break Address and Data Gating (Diagram II-2)

Each 201A line adaptor has assigned two sequential locations in PDP-8 core to be used as buffers for incoming (received) and outgoing (transmitted) data. The low-order four bits, except for the lowest order bit, are specified by an address card shown in Diagram II-5. The high-order five bits (page address) are specified by the Scanner and are gated onto the data address lines when the PGENB signal is given, as derived in Diagram II-3. The remainder of the address bits are specified in Diagram II-3.

The contents of the SDR register are gated onto the data break input lines when the BKSL# signal is present, as shown in Diagram II-2. All of the logic shown in Diagram II-2 is in the individual line adaptor bay.

Common Data Address Gating (Diagram II-3)

There are a total of 128 scanner data lines (64 full-duplex pairs). This corresponds to one full PDP-8 page of buffers. In the twelve-bit PDP-8 address, the high-order five bits specify the page; the low-order bit specifies whether the address is a receive or transmit buffer as the bit is respectively zero or one. The remaining six bits specify which of the 64 line pairs is being referenced. These 64 line pairs are further broken down into eight blocks of eight lines each. Positions 5, 6, and 7 in the address thus specify the block address. A separate cable connects the scanner to each block of line adaptors and in turn provides the block address for those line adaptors, and a common buss (PGENB) to tell the scanner to load the page address on to the data address lines. Diagram II-3 indicates the gating necessary to gate the block address onto the data address lines and pull down the PGENB buss.

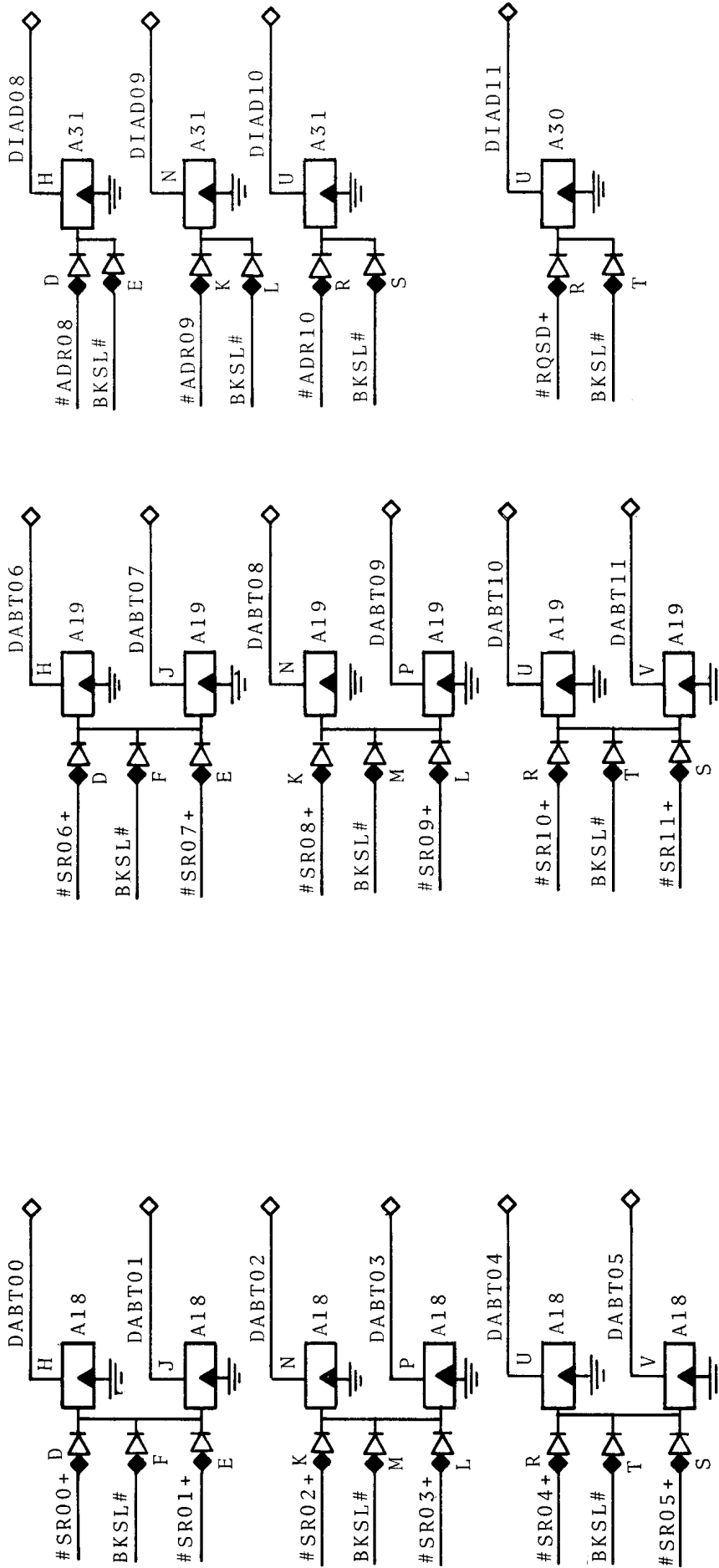


Diagram II-2. DATA BREAK ADDRESS AND DATA GATING

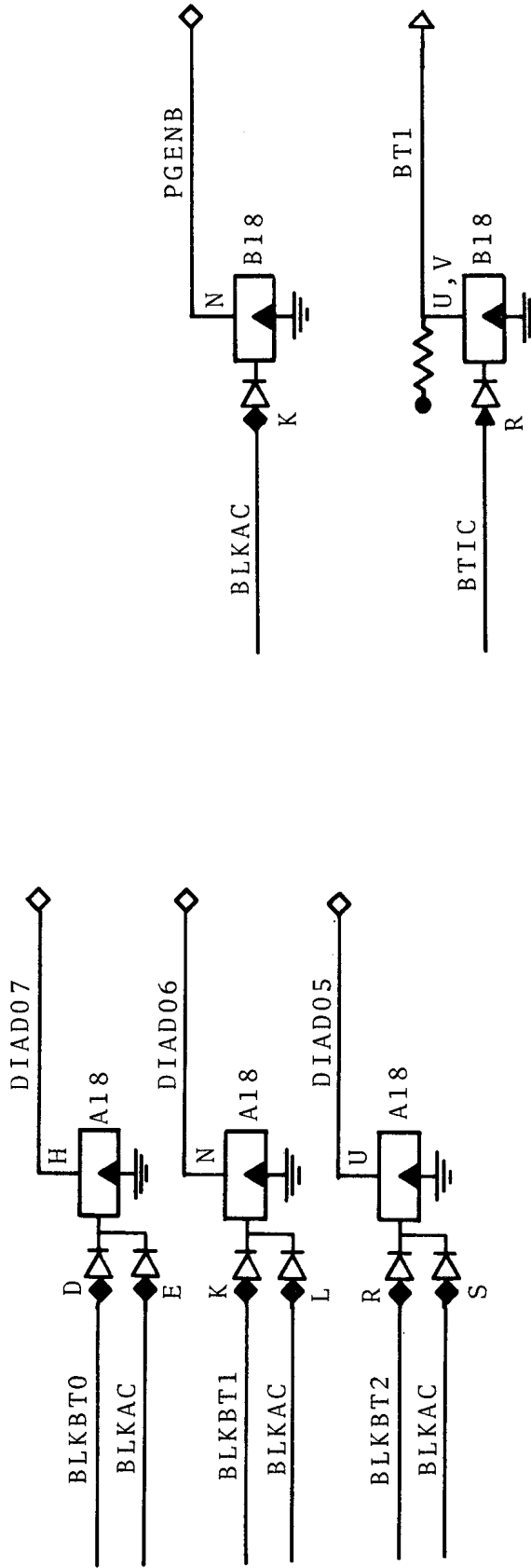


Diagram II-3. COMMON DATA ADDRESS GATING

Scan Address Buffers (Diagram II-4)

These buffers provide the required isolation and signal levels to allow each 201A line adaptor to ascertain whether the current scan address is actually its address. These signals are fed to an address card which decodes the scan address actually assigned to the line adaptor.

Address Decoding (Diagram II-5)

This address card, located in the individual line adaptor bay, provides the line adaptor with its data break address within a scan block and the signals to determine if the current scan address is the line adaptor address.

Data-Break and Device Selection (Diagram II-6)

The first set of gates in Diagram II-6 derives the individual BKSL# signals from the multiplexor signals BKAC#. The BLKAC signal goes to -3v if any of the four 201A line adaptors is granted a data-break cycle by the multiplexor. The signals CTWD1 and CTWD2 are the assertion that the device codes corresponding to Control Word 1 or Control Word 2, respectively, have been detected during an IOT microinstruction.

Device Selection Gating (Diagram II-7)

The gates shown in Diagram II-7 are located in the individual line adaptor bays and provide the signals to differentiate between Control Word 1 and Control Word 2 operations.

Scan Interrupt Service Request (Diagram II-8)

Every time a character is transferred between a 201A line adaptor and the PDP-8's memory, its character service flag (#SRSV) is set, as described previously. The SCNSVC buss is pulled to ground the next time the scan address matches the

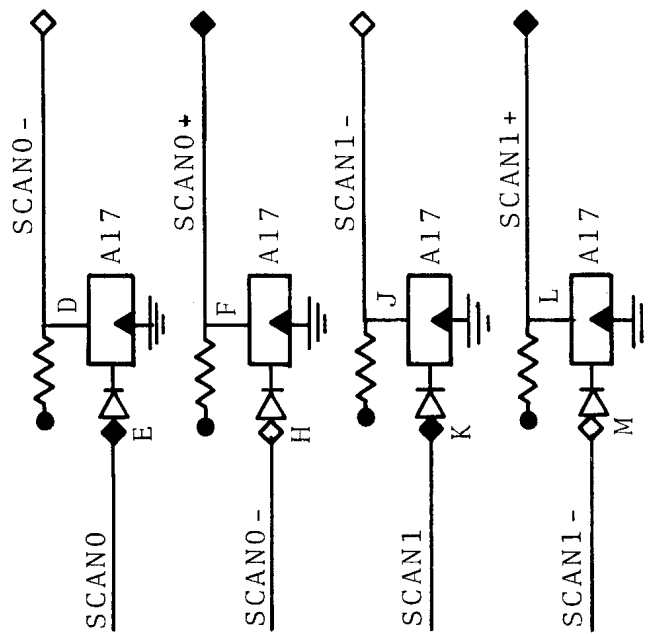
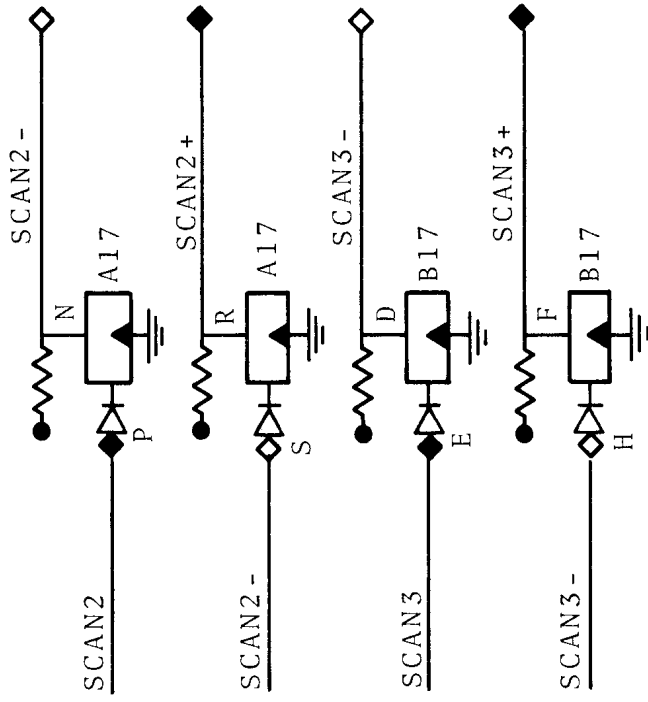


Diagram II-4. SCAN ADDRESS BUFFERS

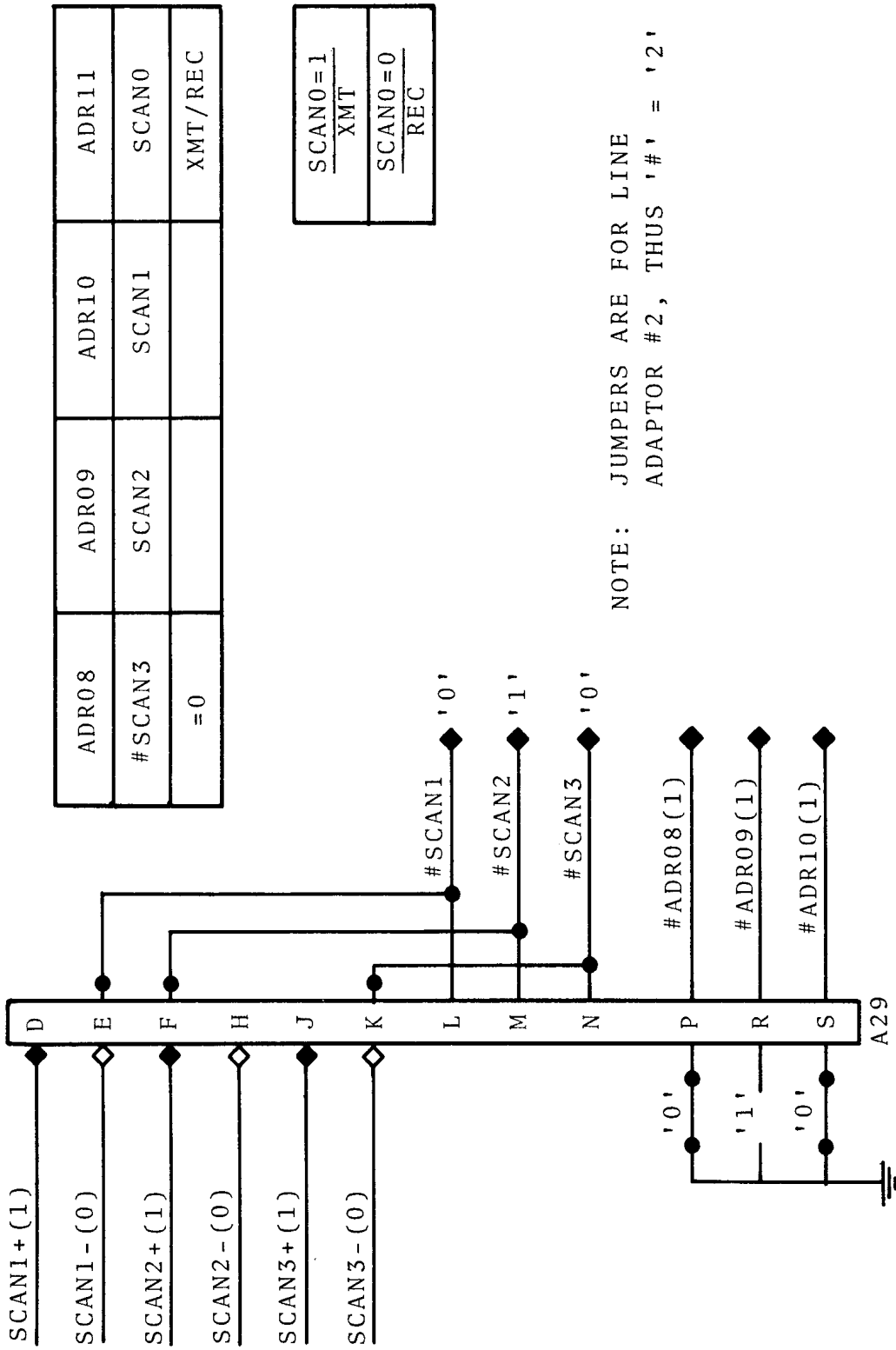


Diagram II-5. ADDRESS DECODING

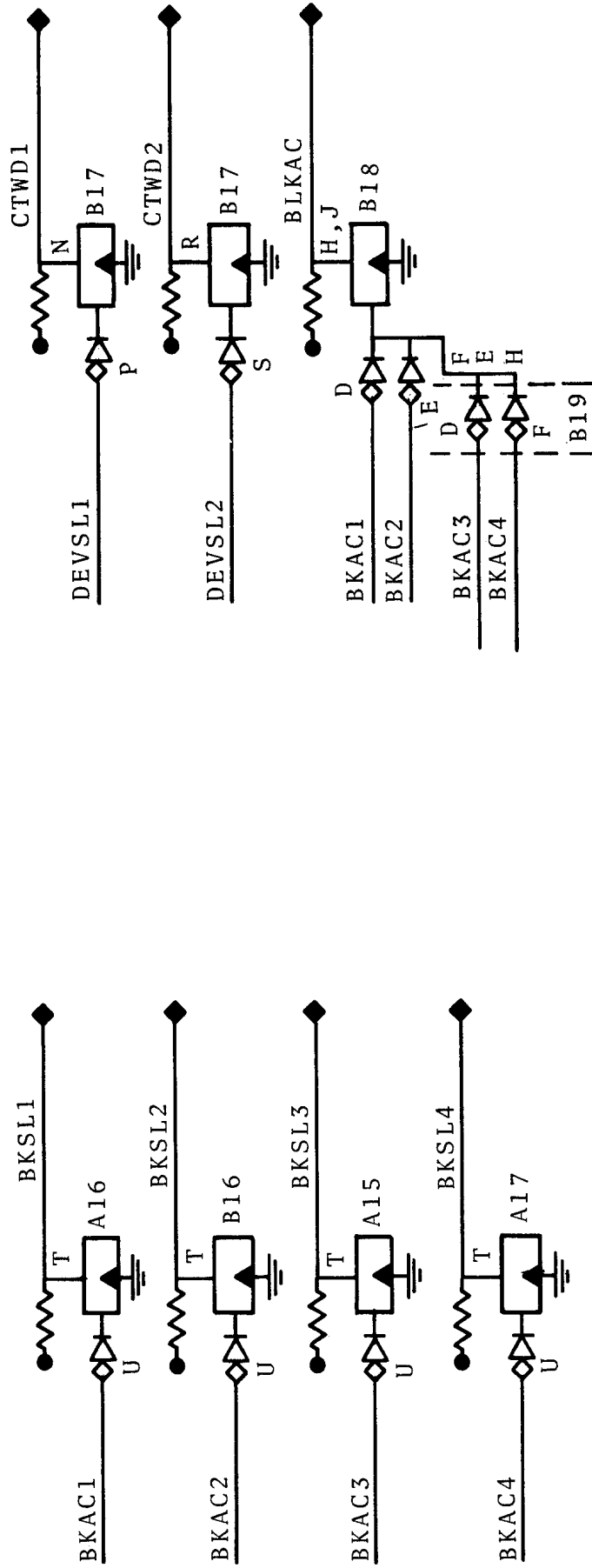


Diagram II-6. DATA-BREAK AND DEVICE SELECTION

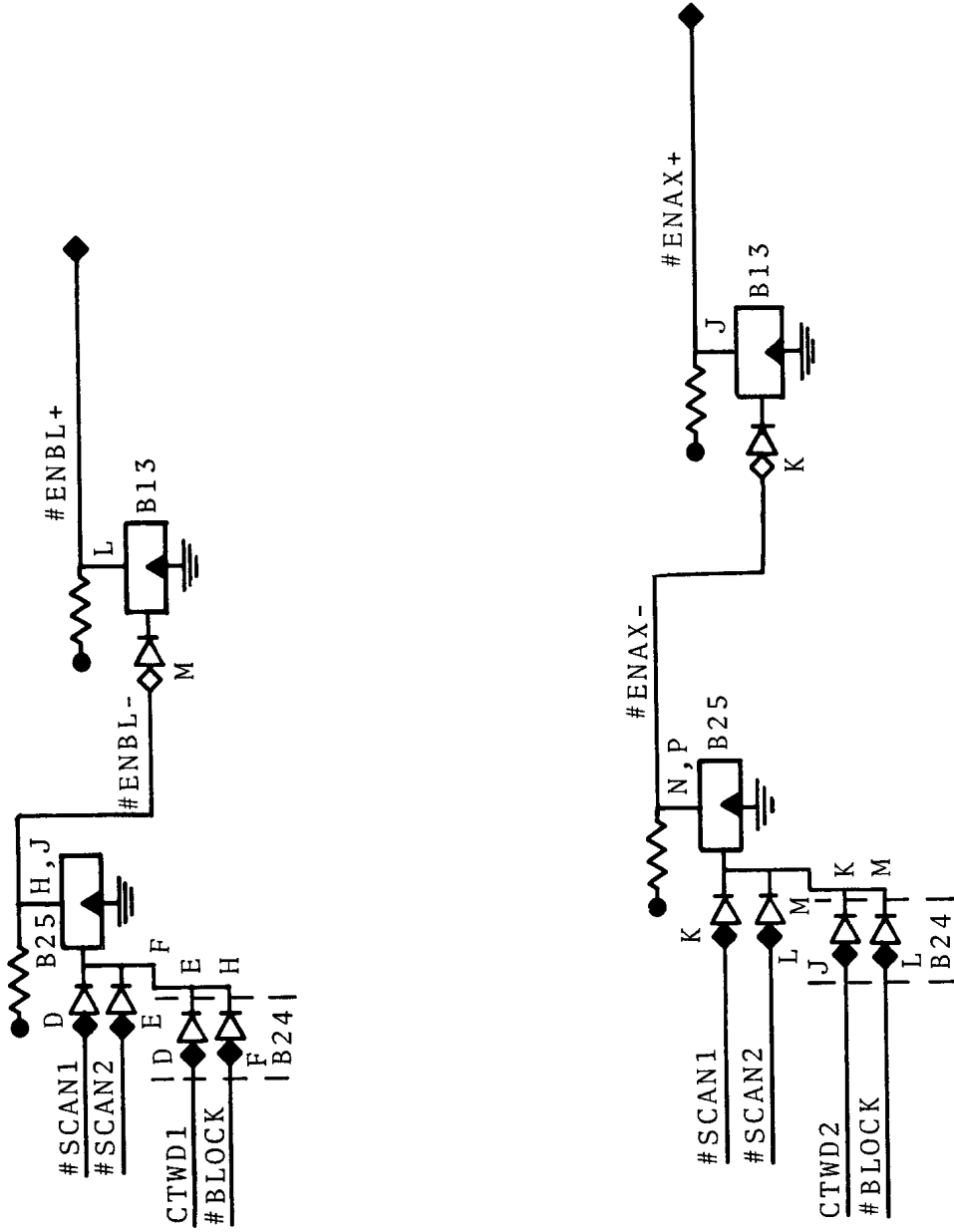


Diagram II-7. DEVICE SELECTION GATING

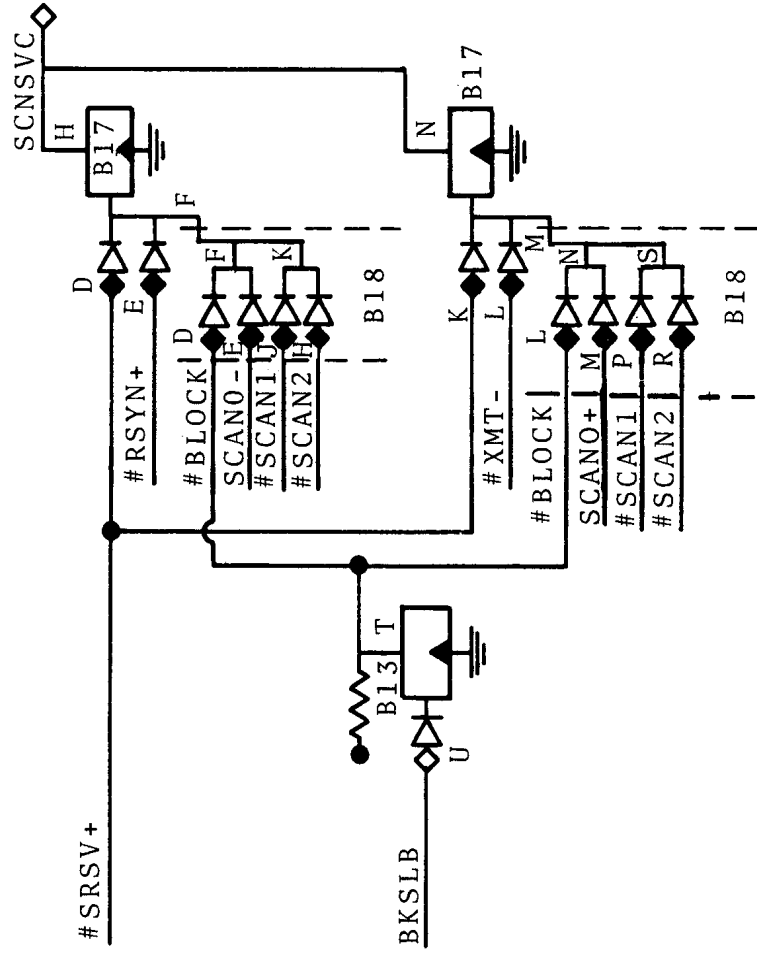


Diagram II-8. SCAN INTERRUPT SERVICE REQUEST

line adaptor's address, as specified by #BLOCK, #SCAN2, #SCAN1, #SCAN0₊. SCNSVC at this time causes a PDP-8 interrupt which the program can then identify.

Transmit Clock Gating (Diagram II-9)

The 201A data sets for the Data Concentrator have externally supplied transmit clocks. This specification allows transmit interrupt staggering and the use of different clock rates. The actual clock selection is made via a jumper card in Bay 1 while the driver for the data set is in the individual line adaptor bay.

"I'm Here" Indication (Diagram II-10)

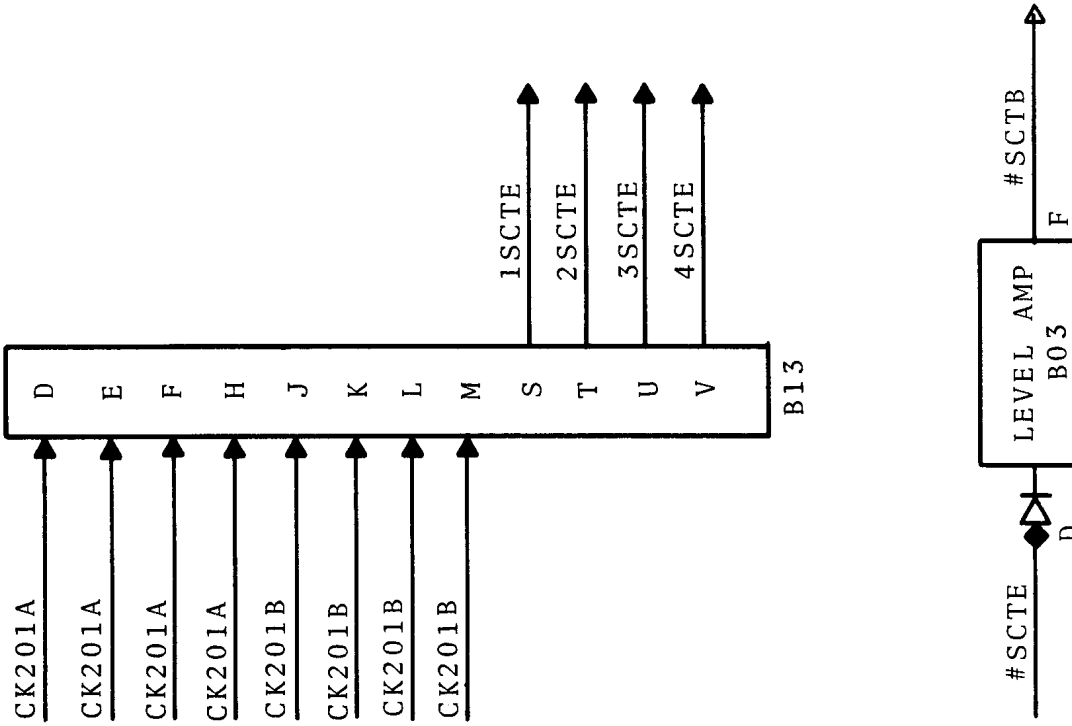
The gating in Diagram II-10, located in the individual line adaptor bays, provides to the scanner a "not here" or "off-line" indication through the #HERE signal.

Buffered Memory Buffer Buffers (Diagram II-11)

This set of buffers is needed for loading reasons in each block of line adaptors. The buffers also provide the necessary inversion to give the correct signal polarity as needed in the line adaptors.

Accumulator Output Buffers (Diagram II-12)

This set of buffers is needed to provide the necessary driving capabilities for the line adaptors. The buffers also provide the necessary inversion to give the correct signal polarity to the line adaptors.



NOTE: JUMPER FROM DESIRED
CLOCK TO #SCTE

Diagram II-9. TRANSMIT CLOCK GATING

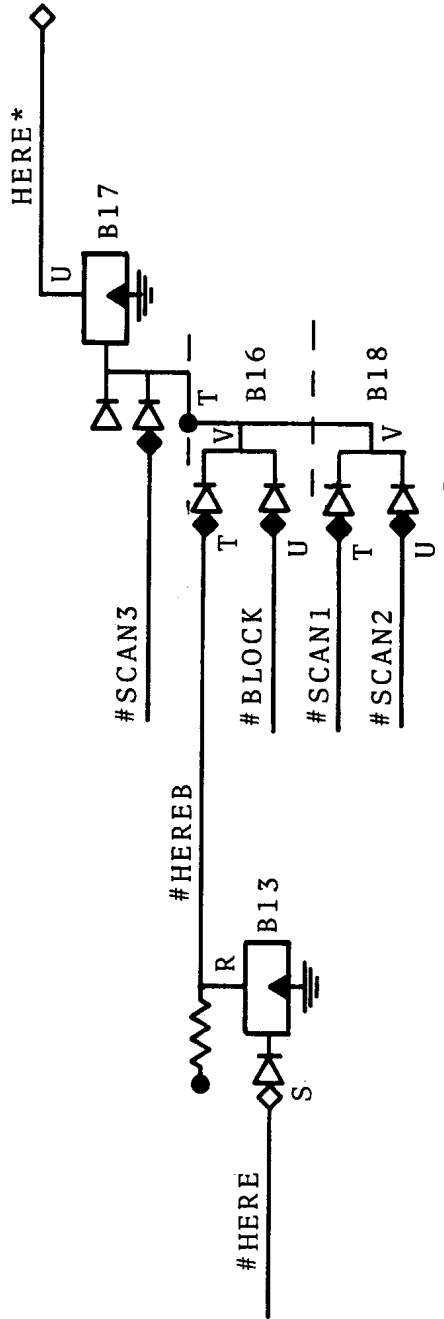


Diagram II-10. 'I'M HERE' INDICATION

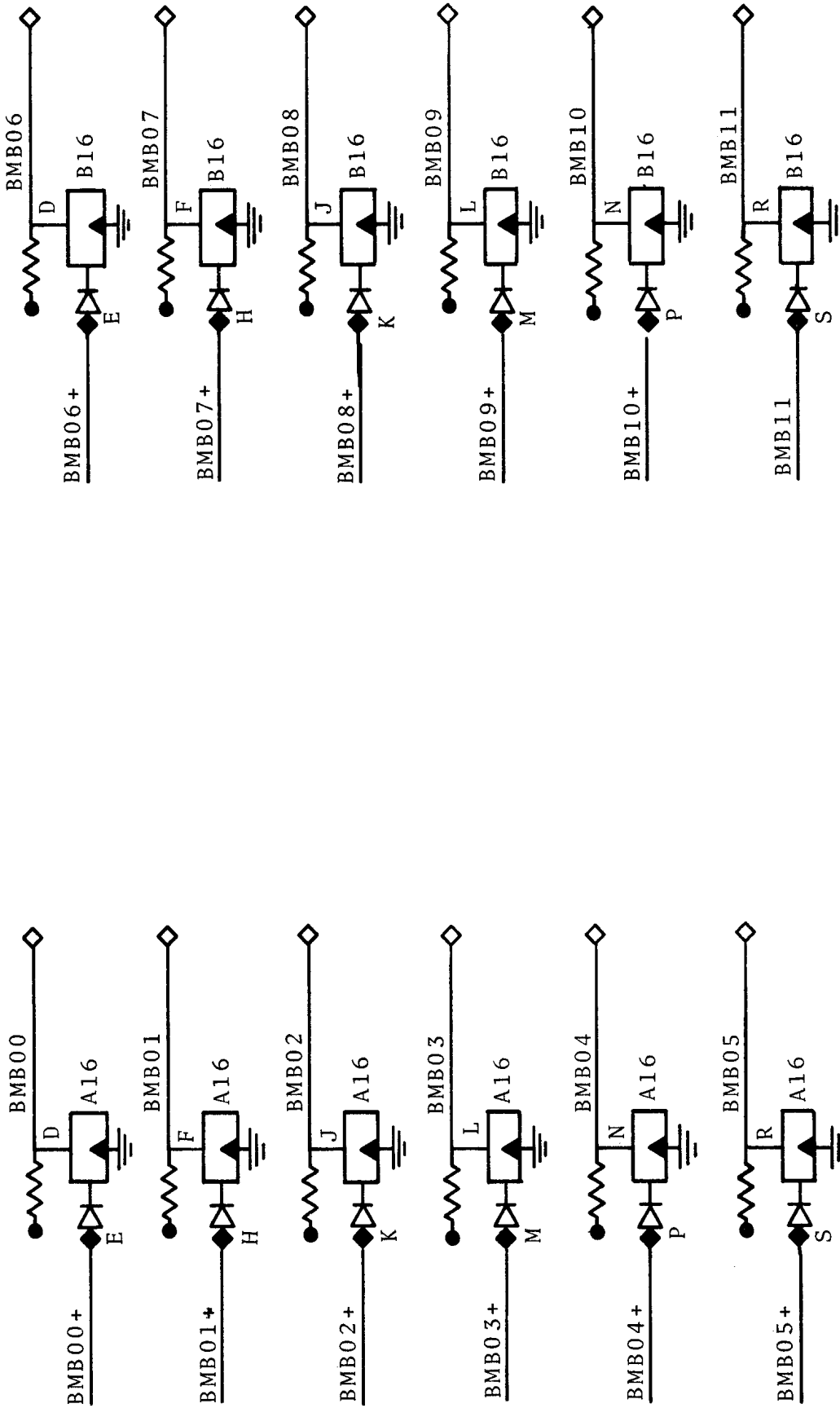


Diagram II-11. BUFFERED MEMORY BUFFER BUFFERS

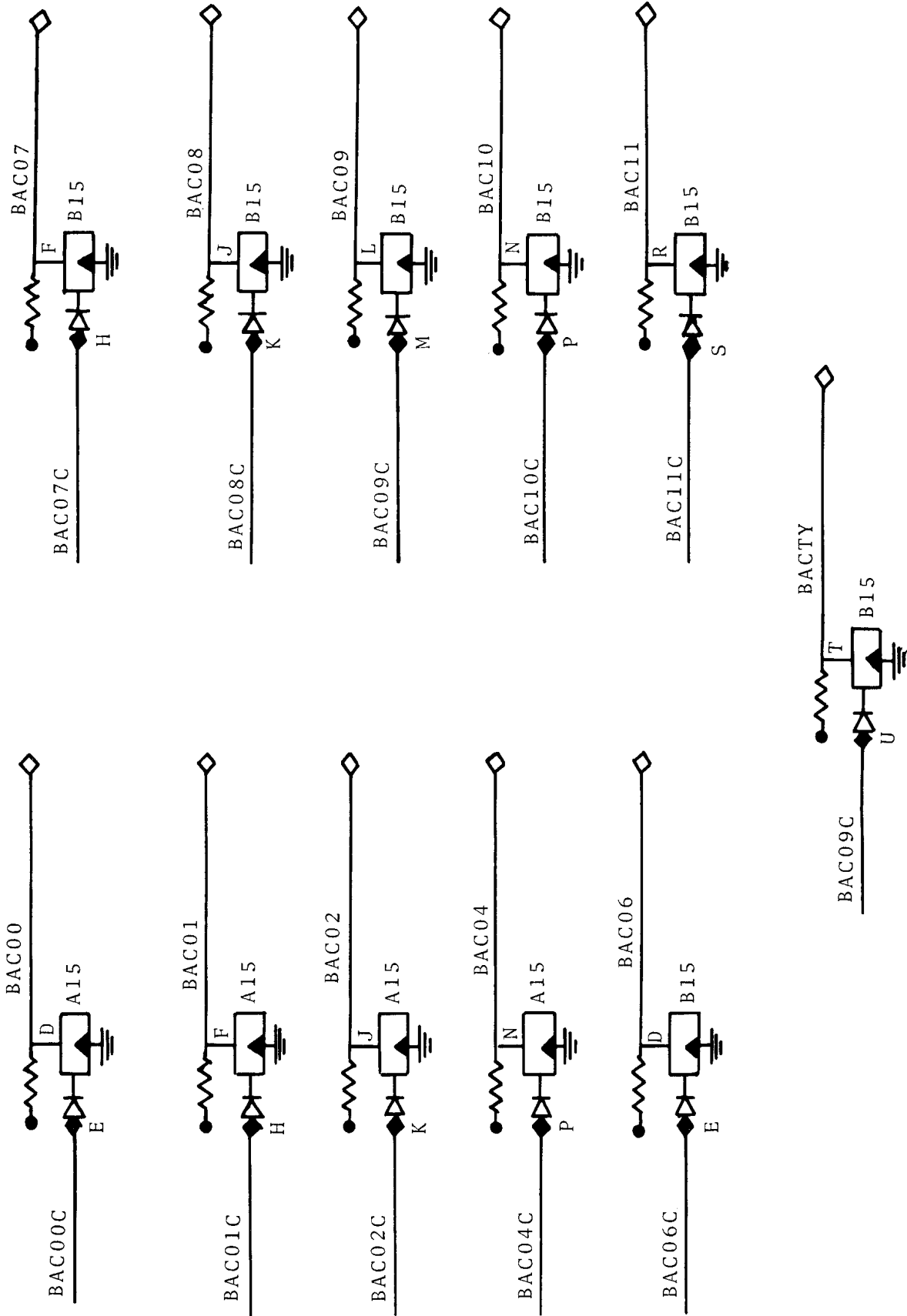


Diagram II-12. ACCUMULATOR OUTPUT BUFFERS

Miscellaneous Circuits (Diagram II-13)

PRYREQ and SPSVC identify to the scanner that the interrupt (SCNSVC) is from a 201A line adaptor. The DTALST buss is used to indicate to the scanner that a line adaptor has a data lost condition (this gate is in the individual line adaptor). The remaining gates provide the necessary electrical signal inversion.

Cable Layout (Diagram II-14)

The input/output cables for the 201A line adaptors are shown in Diagram II-14. The correspondences between the signal names, module positions, and pin connections for the 201A line adaptor block and the multiplexor or scanner are given in Tables II-1 through II-9.

Module Utilizations (Tables II-10 through II-21)

Tables II-10 through II-21 give the module utilization for the four 201A line adaptors comprising the block on the Data Concentrator. In addition to the module utilization, a complete signal name map is also shown.

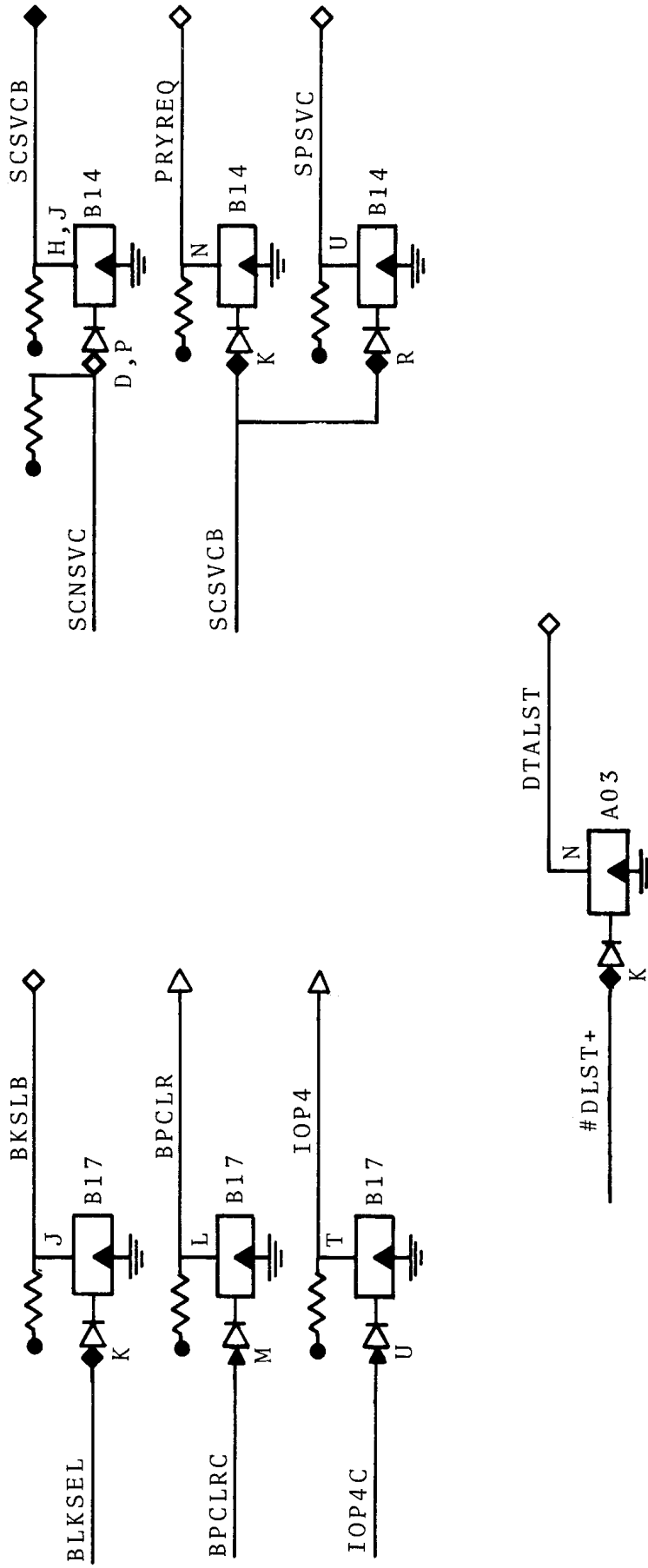


Diagram II-13. MISCELLANEOUS CIRCUITS

	01 02	03 04	05 06	07 08	09 10	11 12	13 14
D	BAC00C	BMB00+	DIAD00	DABT00	EAC00	SCAN0	--
E	BAC01C	BMB01+	DIAD01	DABT01	EAC01	SCAN1	--
F	BAC02C	BMB02+	DIAD02	DABT02	EAC02	SCAN2	--
H	BAC03C	BMB03-	DIAD03	DABT03	EAC03	SCAN3	--
J	BAC04C	BMB03+	DIAD04	DABT04	EAC04	DEVSL1	--
K	BAC05C	BMB04-	DIAD05	DABT05	EAC05	DEVSL2	--
L	BAC06C	BMB04+	DIAD06	DABT06	EAC06	--	CK201A
M	BAC07C	BMB05-	DIAD07	DABT07	EAC07	--	CK201B
N	BAC08C	BMB05+	DIAD08	DABT08	EAC08	--	CKTLPA

'A'

D	BAC09C	BMB06-	DIAD09	DABT09	EAC09	BKRQ1	PRYREQ
E	BAC10C	BMB06+	DIAD10	DABT10	EAC10	BKAC1	SPSVC
F	BAC11C	BMB07-	DIAD11	DABT11	EAC11	BKRQ2	PGENB
H	IOP1C	BMB07+	--	--	--	BKAC2	BLKSEL
J	IOP2C	BMB08-	DICTL	--	--	BKRQ3	BLKBT0
K	IOP4C	BMB08+	BBREAK	--	--	BKAC3	BLKBT1
L	BT1C	BMB09+	ADDACC	--	--	BKRQ4	BLKBT2
M	BT2AC	BMB10+	--	--	--	BKAC4	DTALST
N	BPCLRC	BMB11+	--	--	--	--	HERE*

'B'

Diagram II-13. CABLE LAYOUT

TABLE II-1

BUFFERED ACCUMULATOR OUTPUTS

201A LINE ADAPTOR			MULTIPLEXOR		
INTERFACE CONNECTION	SIGNAL NAME	LOGIC SYMBOL	LOGIC SYMBOL	SIGNAL NAME	INTERFACE CONNECTION
A01D, A02D	BAC00C			CAC00-	A01D
A01E, A02E	BAC01C			CAC01-	A01E
A01H, A02H	BAC02C			CAC02-	A01H
A01K, A02K	BAC03C			CAC03-	A01K
A01M, A02M	BAC04C			CAC04-	A01M
A01P, A02P	BAC05C			CAC05-	A01P
A01S, A02S	BAC06C			CAC06-	A01S
A01T, A02T	BAC07C			CAC07-	A01T
A01V, A02V	BAC08C			CAC08-	A01V
B01D, B02D	BAC09C			CAC09-	B01D
B01E, B02E	BAC10C			CAC10-	B01E
B01H, B02H	BAC11C			CAC11-	B01H

TABLE II-2

BUFFERED MEMORY BUFFER OUTPUT LINES

201A LINE ADAPTOR			MULTIPLEXOR		
INTERFACE CONNECTION	SIGNAL NAME	LOGIC SYMBOL	LOGIC SYMBOL	SIGNAL NAME	INTERFACE CONNECTION
A03D, A04D	BMB00+	—▶	—▶	CMB00-	A02D
A03E, A04E	BMB01+	—▶	—▶	CMB01-	A02E
A03H, A04H	BMB02+	—▶	—▶	CMB02-	A02H
A03K, A04K	BMB03-	—◊	—◊		
A03M, A04M	BMB03+	—▶	—▶	CMB03-	A02M
A03P, A04P	BMB04-	—◊	—◊		
A03S, A04S	BMB04+	—▶	—▶	CMB04-	A02S
A03T, A04T	BMB05-	—◊	—◊		
A03V, A04V	BMB05+	—▶	—▶	CMB05-	A02V
B03D, B04D	BMB06-	—◊	—◊		
B03E, B04E	BMB06+	—▶	—▶	CMB06-	B02E
B03H, B04H	BMB07-	—◊	—◊		
B03K, B04K	BMB07+	—▶	—▶	CMB07-	B02K
B03M, B04M	BMB08-	—◊	—◊		
B03P, B04P	BMB08+	—▶	—▶	CMB08-	B02P
B03S, B04S	BMB09+	—▶	—▶	CMB09-	B02S
B03T, B04T	BMB10+	—▶	—▶	CMB10-	B02T
B03V, B04V	BMB11+	—▶	—▶	CMB11-	B02V

TABLE II-3

PROGRAMMED INPUT/OUTPUT CONTROL

201A LINE ADAPTOR			MULTIPLEXOR		
INTERFACE CONNECTION	SIGNAL NAME	LOGIC SYMBOL	LOGIC SYMBOL	SIGNAL NAME	INTERFACE CONNECTION
B01K, B02K	IOP1C	→	→	CIOP1	B01K
B01M, B02M	IOP2C	→	→	CIOP2	B01M
B01P, B02P	IOP4C	→	→	CIOP4	B01P

TABLE II-4



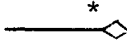



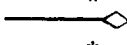

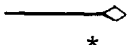









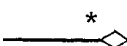

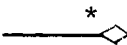

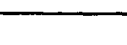

DATA-BREAK ADDRESS LINES

201A LINE ADAPTOR			MULTIPLEXOR		
INTERFACE CONNECTION	SIGNAL NAME	LOGIC SYMBOL	LOGIC SYMBOL	SIGNAL NAME	INTERFACE CONNECTION
A05D, A06D	DIAD00	—*◇	—◇	DADD00	A03D
A05E, A06E	DIAD01	—*◇	—◇	DADD01	A03E
A05H, A06H	DIAD02	—*◇	—◇	DADD02	A03H
A05K, A06K	DIAD03	—*◇	—◇	DADD03	A03K
A05M, A06M	DIAD04	—*◇	—◇	DADD04	A03M
A05P, A06P	DIAD05	—*◇	—◇	DADD05	A03P
A05S, A06S	DIAD06	—*◇	—◇	DADD06	A03S
A05T, A06T	DIAD07	—*◇	—◇	DADD07	A03T
A05V, A06V	DIAD08	—*◇	—◇	DADD08	A03V
B05D, B06D	DIAD09	—*◇	—◇	DADD09	B03D
B05E, B06E	DIAD10	—*◇	—◇	DADD10	B03E
B05H, B06H	DIAD11	—*◇	—◇	DADD11	B03H

*Note: Collector of a Grounded-Emitter Transistor.

TABLE II-5



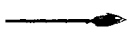

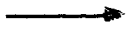

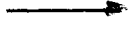

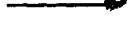



DATA-BREAK INPUT LINES

201A LINE ADAPTOR			MULTIPLEXOR		
INTERFACE CONNECTION	SIGNAL NAME	LOGIC SYMBOL	LOGIC SYMBOL	SIGNAL NAME	INTERFACE CONNECTION
A07D, A08D	DABT00			DBIT00	A04D
A07E, A08E	DABT01			DBIT01	A04E
A07H, A08H	DABT02			DBIT02	A04H
A07K, A08K	DABT03			DBIT03	A04K
A07M, A08M	DABT04			DBIT04	A04M
A07P, A08P	DABT05			DBIT05	A04P
A07S, A08S	DABT06			DBIT06	A04S
A07T, A08T	DABT07			DBIT07	A04T
A07V, A08V	DABT08			DBIT08	A04V
B07D, B08D	DABT09			DBIT09	B04D
B07E, B08E	DABT10			DBIT10	B04E
B07H, B08H	DABT11			DBIT11	B04H

*Note: Collector of a Grounded-Emitter Transistor.

TABLE II-6

DATA BREAK CONTROL SIGNALS

201A LINE ADAPTOR			MULTIPLEXOR		
INTERFACE CONNECTION	SIGNAL NAME	LOGIC SYMBOL	LOGIC SYMBOL	SIGNAL NAME	INTERFACE CONNECTION
B 05M, B 06M	DICTL			TRADI	B 03M
B 05P, B 06P	BBREAK			CBBRK	B 03P
B 05S, B 06S	ADDACC			CADACP	B 03S
B 01S, B 02S	BTIC			CBT1	B 01S
B 01T, B 02T	BT2AC			CBT2A	B 01T
B 01V, B 02V	BPCLRC			CPWCLR	B 01V

*Note: Collector of a Grounded-Emitter Transistor.

TABLE II-7

DATA BREAK REQUEST AND SELECT


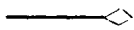

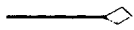












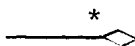

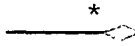
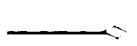
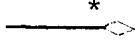
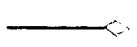
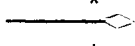

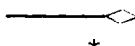
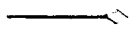
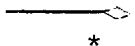
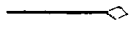
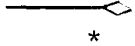
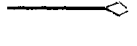
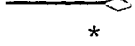

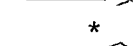



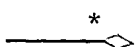



201A LINE ADAPTOR			MULTIPLEXOR		
INTERFACE CONNECTION	SIGNAL NAME	LOGIC SYMBOL	LOGIC SYMBOL	SIGNAL NAME	INTERFACE CONNECTION
B11D	BKRQ1			REQ2	D01D
B11E	BKAC1			SEL2	D01E
B11H	BKRQ2			REQ3	D01H
B11K	BKAC2			SEL3	D01K
B11M	BKRQ3			REQ4	D01M
B11P	BKAC3			SEL4	D01P
B11S	BKRQ4			REQ5	D01S
B11T	BKAC4			SEL5	D01T

TABLE II-8

EXTENDED ACCUMULATOR INPUTS

201A LINE ADAPTOR			SCANNER		
INTERFACE CONNECTION	SIGNAL NAME	LOGIC SYMBOL	LOGIC SYMBOL	SIGNAL NAME	INTERFACE CONNECTION
A09D, A10D	EAC00			EAC00+	A07D, A08D
A09E, A10E	EAC01			EAC01+	A07E, A08E
A09H, A10H	EAC02			EAC02+	A07H, A08H
A09K, A10K	EAC03			EAC03+	A07L, A08K
A09M, A10M	EAC04			EAC04+	A07M, A08M
A09P, A10P	EAC05			EAC05+	A07P, A08P
A09S, A10S	EAC06			EAC06+	A07S, A08S
A09T, A10T	EAC07			EAC07+	A07T, A08T
A09V, A10V	EAC08			EAC08+	A07V, A08V
B09D, B10D	EAC09			EAC09+	B07D, B08D
B09E, B10E	EAC10			EAC10+	B07E, B08E
B09H, B10H	EAC11			EAC11+	B07H, B08H

*Note: Collector of a Grounded-Emitter Transistor.

TABLE II-9

SCAN ADDRESS

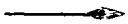



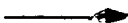









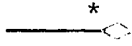

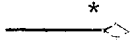
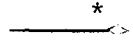
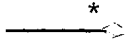
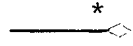
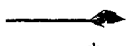

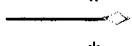
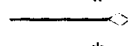


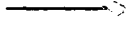
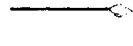
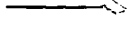

201A LINE ADAPTOR			SCANNER		
INTERFACE CONNECTION	SIGNAL NAME	LOGIC SYMBOL	LOGIC SYMBOL	SIGNAL NAME	INTERFACE CONNECTION
A11D, A12D	SCAN 0			BXMT-	C03D
A11E, A12E	SCAN 1			BAD1-	C03E
A11H, A12H	SCAN 2			BAD2-	C03H
A11K, A12K	SCAN 3			BAD3-	C03K
B12M	BLKBT0			GND	D01M
B12P	BLKBT 1			GND	D01P
B12S	BLKBT2			GND	D01S

TABLE II-10



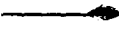
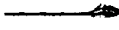
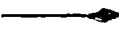
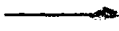
SCANNER CONTROL SIGNALS

201A LINE ADAPTOR			SCANNER		
INTERFACE CONNECTION	SIGNAL NAME	LOGIC SYMBOL	LOGIC SYMBOL	SIGNAL NAME	INTERFACE CONNECTION
B12D	PRYREQ			PORQ+	D01D
B12E	SPSVC			SS0+	D01E
B12H	PGENB			PGENB+	D01H
B12K	BLKSEL			BKSLO-	D01K
B12T	DTALST			DLOST+	D01T
B12V	HERE*			LACHK-	D01V
A11M, A12M	DEVSL1			DSL+	C03M
A11P, A12P	DEVSL2			ESL+	C03P

*Note: Collector of a Grounded-Emitter Transistor

TABLE II-11

TRANSMIT CLOCK

201A LINE ADAPTOR			MULTIPLEXOR		
INTERFACE CONNECTION	SIGNAL NAME	LOGIC SYMBOL	LOGIC SYMBOL	SIGNAL NAME	INTERFACE CONNECTION
A13S, A14S	CK201A			CK2000	D03S
A13T, A14T	CK201B			CK2400	D03T
A13V, A14V	CKTLPA				

COMMON SECTION

PANEL 1

	A01	A02	A03	A04	A05	A06	A07	A08	A09	A10	A11	A12	A13	A14	A15	A16
A	W021	W021	W021	W021	W021	W021	W021	W021	W021	W021	W021	W021	W021	W021	W021	W021
B																
C																
D																
E																
F																
G																
H																
I																
J																
K																
L																
M																
N																
O																
P																
Q																
R																
S																
T																
U																
V																

TABLE II-12.

PANEL I COMMON SECTION

	A17	A18	A19	A20	A21	A22	A23	A24	A25	A26	A27	A28	A29	A30	A31	A32	
A	RIC7	RII1					W05C	W05C									A
B																	B
C																	C
D	SCANC-	BLKPTC															D
E	SCANC	BLKAC					ISRSV+	2SRSV+									E
F	SCANC+																F
H	SCANC-	DIADC7					IDLST+	2DLST+									H
J	SCAN1-																J
K	SCAN1	BLKBT1					IPAR+	2PAR+									K
L	SCAN1+	BLKAC															L
M	SCAN1-						1STRDY	2STRDY									M
N	SCAN2-	DIADC6															N
P	SCAN2						1TMRD+	2TMRD+									P
R	SCAN2+	BLKBT2															R
S	SCAN2-	BLKAC					1XMT+	2XMT+									S
T	BKSL4																T
U	BKAC4	DIADC5					1REC+	2REC+									U
V																	V

	B17	B18	B19	B20	B21	B22	B23	B24	B25	B26	B27	B28	B29	B30	B31	B32	
A	RIC7	RII1	R001				W05C	W05C									A
B																	B
C																	C
D	SCAN3-	BKAC1	BKAC3														D
E	SCAN3	BKAC2	BLKND				3SRSV+	4SRSV+									E
F	SCAN3+	BLKND	BKAC4														F
H	SCAN3-	BLKAC	BLKND				3DLST+	4DLST+									H
J	BKSLB	BLKAC					3PAR+	4PAR+									J
K	BLKSEL	BLKAC															K
L	BPCLR						3STRDY	4STRDY									L
M	BPCLRC																M
N	CIWD1	PGENB															N
P	DEVSL1						3TMRD+	4TMRD+									P
R	CIWD2	BTIC															R
S	DEVSL2						3XMT+	4XMT+									S
T	IOP4																T
U	IOP4C	BTI					3REC+	4REC+									U
V		BTI															V

TABLE II-13.

PANEL 2 PORT 0/LINE ADAPTOR 1

	A01	A02	A03	A04	A05	A06	A07	A08	A09	A10	A11	A12	A13	A14	A15	A16
A	W2C1C	EIAR	R111	W501	R111	R001	R302	R111	R201	R205	R205	R205	R205	R205	R201	R205
B																
C																
D																
E																
F																
G																
H																
I																
J																
K																
L																
M																
N																
O																
P																
Q																
R																
S																
T																
U																
V																

	B01	B02	B03	B04	B05	B06	B07	B08	B09	B10	B11	B12	B13	B14	B15	B16
A	W6C2	EIAR	W602	W501	W501	R202	R602	R602	R602	R602	R202	R107	R107	R121	R111	R002
B																
C																
D																
E																
F																
G																
H																
I																
J																
K																
L																
M																
N																
O																
P																
Q																
R																
S																
T																
U																
V																

TABLE II-14.

PANEL 2 ... PORT O/LINE ADAPTOR 1

	A17	A18	A15	A20	A21	A22	A23	A24	A25	A26	A27	A28	A29	A30	A31	A32
R202	R123	R123	R201	R201	R2C1	K201	R205	R2C5	R205	R205	R123	R123	W994	R123	R111	
A																
B																
C																
D	1FR3+	1SR06+	1SR06+	1INVMK	1ADAC	1START	1INVMK	1ISTCK	1BRKDN	1RSRV+	1EBPC+	1LEBPC+	1SCANI+	1ICFR3+	1IADR08	
E	IDY-	1SRC1+	1SR07+	1INVMK	1ADAC	1START	1INVMK	1CLSD-	1RQSD-	1DLST+	1IFMD+	1IFMD+	1SCAN1-	1ICFR2+	1BKSL1	
F		BKSL1	BKSL1	BAC07	1GND15	1GND20	1PWCLR	1PWCLR	1PWCLR	1PWCLR	1ENBL+	1ENBL+	1SCAN2+	1ENAX+		
H	ILINE-	DABTC6	DABTC6	IREC-			1EBPC+	1PAR+	1RSI	EAC00	EAC06	SCAN2-	EAC08	DIAD08		
J	ILINE+	DABTC7	DABTC7	1XMT+			1EBPC+	1PAR+	1RQSD+	EAC01	EAC07	SCAN3+	EAC09			
K	JCLUCK	1SR02+	1SR08+	1PWCLR	1PWCLR	1PWCLR	BAC06	BAC02	1XTRQ-	1PAR+	1STRDY	SCAN3-	1ICFR1+	1ADR09		
L	LLINE+	1SR03+	1SR09+	1IFMD+	1BKRQ+	1SVC-	BAC06	BAC02	1XTRQ+	1RQSD+	1ITMRD+	1SCANI	1ICFRQ+	1BKSL1		
M	IFR3+	BKSL1	BKSL1	1IFMD-			ICLOCK		BTI	1ENBL+	1ENBL+	1SCAN2	1ENAX+			
N	IFR3+	DABTC2	DABTC8				1INVMK	1INVMK	1INVMK	EAC02	EAC08	1SCAN3	EAC10	DIAD09		
P	IPATY-	DABTC3	DABTC9	1INVMK	1FR3+	1REC-	1ITMRD+	1DLST+	1RSRV+	1XTRQ+	EAC03	EAC09	1ADRC8	EAC11		
R	IPATY-	1SR04+	1SR10+	BAC07	1IFMD-	1XMT+	1RSRV-	1XTRQ-	1XTRQ+	1XTRQ+	1IRING	1ADR09	1RQSD+	1ADR10		
S	IPATY+	1SR05+	1SR11+	1CLCK	1START	1XMT-	1RSRV-	1ESRSV	1CLSD+	1ICARDT	1ADR10	1RQSD+	1BKSL1			
T		BKSL1	BKSL1	1ICTSY-	1XMT-	1REC-	BACTY	BAC01	BAC04	1ENBL+	1ENBL+					
U	IFR3+	DABTC4	DABTC10	1XMT-			BACTY	BAC01	BAC00	BAC04	EAC10			DIAD11	DIAD10	
V	IPATY+	DABTC5	DABTC11	1REC+			1CHRDN	1CHRDN	EAC05	EAC11				DICTL		

	B17	B18	B15	B20	B21	B22	B23	B24	B25	B26	B27	B28	B29	B30	B31	B32
R111	R002	R001	R111	R121	R121	R121	R121	R001	R111	R603	R602	R205	R205	R205	R205	

	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V
A	1RSRV+	1BLCK	1ITMRD+	1RQSD+																		
B	1RSY+	1SCAN0-	1XMTND	1CLSD+																		
C	1SNIND	1SNIND	1CARDT	1XMTND																		
D	1SCNSVC	1SCANI	1XMTND	1XMT-	1FNZR	1ADAC	1BLND	1ENBL-	1SVC-	1ICFR0-	1ICFR2-											
E	1SRV+	1SNIND	1XMTND	1FR3+	1IFMC+	1IFMC+	1XND	1XND	1GNDS9	1FR0+	1FR2+											
F	1XMT+	1BLCK	1FR2+	1FR0+	1EFTM+	1EFTM+	1EFTM+	1EFTM+	1GNDS9	1FRZE	1IFR0	1IFR0	1ICFR0+	1ICFR2+								
G	1SA2ND	1SCAN0+	1DYNE	1DYND	1IFMC+	1IFMC+	1XND	1XND	1GNDS9	1FRZE	1IFR0	1IFR0	1ICFR0+	1ICFR2+								
H	1SCNSVC	1SN2ND	1FR1+	1DY-	1XTRQ+	1REC+	1ENAX-	1ENAX-	1GNDS9	1FRZE	1IFR0	1IFR0	1ICFR0+	1ICFR2+								
I	1SCANI	1DYNE	1DY-	1XMT+	1IFMD+	1BIC	1PARND	1ENAX-	1GNDS9	1FRZE	1IFR0	1IFR0	1ICFR0+	1ICFR2+								
J	1SCANI	1DYNE	1DY-	1XMT+	1IFMD+	1BIC	1PARND	1ENAX-	1GNDS9	1FRZE	1IFR0	1IFR0	1ICFR0+	1ICFR2+								
K	1SCANI	1DYNE	1DY-	1XMT+	1IFMD+	1BIC	1PARND	1ENAX-	1GNDS9	1FRZE	1IFR0	1IFR0	1ICFR0+	1ICFR2+								
L	1SCANI	1DYNE	1DY-	1XMT+	1IFMD+	1BIC	1PARND	1ENAX-	1GNDS9	1FRZE	1IFR0	1IFR0	1ICFR0+	1ICFR2+								
M	1SCANI	1DYNE	1DY-	1XMT+	1IFMD+	1BIC	1PARND	1ENAX-	1GNDS9	1FRZE	1IFR0	1IFR0	1ICFR0+	1ICFR2+								
N	1SCANI	1DYNE	1DY-	1XMT+	1IFMD+	1BIC	1PARND	1ENAX-	1GNDS9	1FRZE	1IFR0	1IFR0	1ICFR0+	1ICFR2+								
O	1SCANI	1DYNE	1DY-	1XMT+	1IFMD+	1BIC	1PARND	1ENAX-	1GNDS9	1FRZE	1IFR0	1IFR0	1ICFR0+	1ICFR2+								
P	1SCANI	1DYNE	1DY-	1XMT+	1IFMD+	1BIC	1PARND	1ENAX-	1GNDS9	1FRZE	1IFR0	1IFR0	1ICFR0+	1ICFR2+								
Q	1SCANI	1DYNE	1DY-	1XMT+	1IFMD+	1BIC	1PARND	1ENAX-	1GNDS9	1FRZE	1IFR0	1IFR0	1ICFR0+	1ICFR2+								
R	1SCANI	1DYNE	1DY-	1XMT+	1IFMD+	1BIC	1PARND	1ENAX-	1GNDS9	1FRZE	1IFR0	1IFR0	1ICFR0+	1ICFR2+								
S	1SCANI	1DYNE	1DY-	1XMT+	1IFMD+	1BIC	1PARND	1ENAX-	1GNDS9	1FRZE	1IFR0	1IFR0	1ICFR0+	1ICFR2+								
T	1SCANI	1DYNE	1DY-	1XMT+	1IFMD+	1BIC	1PARND	1ENAX-	1GNDS9	1FRZE	1IFR0	1IFR0	1ICFR0+	1ICFR2+								
U	1SCANI	1DYNE	1DY-	1XMT+	1IFMD+	1BIC	1PARND	1ENAX-	1GNDS9	1FRZE	1IFR0	1IFR0	1ICFR0+	1ICFR2+								
V	1SCANI	1DYNE	1DY-	1XMT+	1IFMD+	1BIC	1PARND	1ENAX-	1GNDS9	1FRZE	1IFR0	1IFR0	1ICFR0+	1ICFR2+								

TABLE II-15.

PANEL 3 ... PORT 1/LINE ADAFTOR 2

	A17	A18	A15	A20	A21	A22	A23	A24	A25	A26	A27	A28	A29	A30	A31	A32
A	R202	R123	R123	R201	R201	R201	R205	R205	R205	R205	R123	R123	R123	R123	R111	
B																
C																
D	2FR3+	2SK00+	2SR06+	2INVMK	2INVMK	2INVMK	2INVMK	2STCK	2STCK	2BRKDN	2RSRV+	2EBPC+	SCAN1+	2CFR3+	2ADRO8	
E	2DY-	2SR01+	2SR07+	2INVMK	2ALAC	2START	2START	2CLSD-	2CLSD-	2RQSD-	2DLST+	2IFMD+	SCAN1-	2CFR2+	BKSL2	
F		BKSL2	BKSL2	BACC7	BACC7	BACC7	BACC7	2PWCLR	2PWCLR	2PWCLR	2ENBL+	2ENBL+	SCAN2+	2ENAX+		
H	2LINE-	DABT00	DABT06	2REC-	2REC-	2REC-	2REC-	2PARI	2PARI	2RS1	EAC00	EAC06	SCAN2-	EAC08	DIAD08	
J	2LINE+	DABT01	DABT07	2XMT+	2XMT+	2XMT+	2XMT+	EAC02	EAC02	EAC01	EAC07	SCAN3+	EAC09			
K	2CLOCK	2SR02+	2SR08+	2PWCLR	2PWCLR	2PWCLR	2PWCLR	2C5-	2C5-	2XTRC-	2PAR+	2STRDY	SCAN3+	2CFR1+	2ADRO9	
L	2LINE+	2SR03+	2SR09+	2IFMD+	2BKRQ+	2SVC-	2SVC-	2C5+	2C5+	2XTRQ+	2RQSD+	2TRRD+	2SCAN1	2CFR0+	BKSL2	
M	2FRAZ	BKSL2	BKSL2	2IFMD-	2IFMD-	2IFMD-	2IFMD-	2CLCCK	2CLCCK	FT1	2ENBL+	2ENBL+	2SCAN2	2ENAX+		
N	2FR3+	DABT02	DABT08	2RSTRT	2RSTRT	2RSTRT	2RSTRT	2INVMK	2INVMK	2INVMK	EAC02	EAC08	2SCAN3	EAC10	DIAD09	
P	2PATY-	DABT03	DABT09	2INVMK	2FR3+	2RREC-	2RREC-	2SKSV+	2SKSV+	2XTRQ+	EAC03	EAC09	2ADRC8	EAC11		
R	2PATY+	2SR04+	2SR10+	BACC7	2IFMC-	2XMT+	2XMT+	2RSRV-	2RSRV-	2XTRQ-	2XTRQ+	2TRNG	2ADRC9	2RQSD+	2ADRI0	
S		2SK05+	2SR11+	2CLOCK	2START	2XMT-	2XMT-	2RSRV-	2RSRV-	2CLSD+	2CLSD+	2CARDT	2ADRI0	2RQSD+	BKSL2	
T		BKSL2	BKSL2	2UTSY-	2XMT-	2REC+	2REC+	BACTY	BACTY	BAC04	2ENBL+	2ENBL+	BKSL2			
U	2FR3+	DABT04	DABT10	2XMT-	2XMT-	2XMT-	2XMT-	BACTY	BACTY	BAC04	EAC04	EAC10	DIAC11	DIAD10		
V	2PATY+	DABT05	DABT11	2REC+	2REC+	2REC+	2REC+	ZCHREN	ZCHREN	EAC05	EAC11		DICTL			

	B17	B18	B19	B20	B21	B22	B23	B24	B25	B26	B27	B28	B29	B30	B31	B32
A	R111	R002	R001	R111	R121	R121	R121	R001	R111	R603	R602	R205	R205	R205	R205	R205
B																
C																
D	2RSRV+	2BLUCK	2IMRO+	2RQSD+	2EP2	2EP2	2EP2	CTWD1	2SCAN1	1OP4	2GND59	2GND60	2GND61	2GND61	2GND61	
E	2RSYN+	SCANC-	2XMTD	2CLSD+	2RD+	2RD+	2RD+	2BLND	2SCAN2	2ENBL-	2JMP59	2CLOCK	2FRI+	2FRI+	2FRI+	
F	2SNIND	2SMIND	2CARTI	2XMTD	2DTSY+	2DTSY+	2DTSY+	2BLCCK	2BLND	2INVMK	2SVC-	2FRZE	2FRZE	2FRZE	2FRZE	
H	2SCNSVC	2SCAN1	2XMTD	2XMT-	2ENZR	2ENZR	2ENZR	2ENBL-	2ENBL-	2ENBL-	2SVC-	2FRZE	2FRZE	2FRZE	2FRZE	
J	2RSRV+	2SCAN2	2STRDY	2XMT-	2REC+	2REC+	2REC+	CTWD2	2ENBL-	2ENBL-	2GND59	2FR0+	2FR2+	2FR2+	2FR2+	
K	2XMT+	2SMINC	2XMTD	2FR3+	2IFMD+	2XMT+	2XMT+	2XMTD	2SCAN1	2ZROSR	2FRZE	2FR0+	2FR2+	2FR2+	2FR2+	
L	2XMT+	2BLUCK	2FR2+	2FRC+	2XMT+	2XMT+	2XMT+	2BLOCK	2SCAN2	2XTR0+	2PWCLR	2FR0	2GND61	BAC11	BAC09	
M	2SACND	SCANC+	2DYNC	2LYNU	2IFMD+	2RD+	2RD+	2XND	2XND	2LDFR	2JMP59	2LDFR	2LDFR	BAC11	BAC09	
N	2SCASVC	2SMZND	2FRI+	2DY-	2XTRC+	2REC+	2REC+	2BREA	2ENAX-	2ENAX-	2FR0+	2FR2+	2FR2+	2LDAUX	2LDAUX	
P		2SCAN1	2DYNC	2DY-	2XMT+	2IFMD+	2IFMD+	2BTIC	2ENAX-	2MBSR	2IFMD-	2FRI+	2FRI+	2CFR3+	2CFR3+	
R		2SCAN2	2EBPC+	2REC+	2REC-	2RSRV	2PARI	2DY+	2RD+	1OP4	2XMT-	2XMT-	2XMT-	2CFR1-	2CFR3-	
S	2SCAN3	2SMZND	2DYNC	2IFMD+	2FQSD-	2XMT+	2RD-	2PARND	2PATY-	2ENAX-	2IFMD+	2CFR1-	2CFR3-	2CFR1-	2CFR3-	
T	2HERND	2SCAN1	2IFMD+	2CLSD-	2XTRQ+	2REC+	2REC+	2PARNC	2LDAUX	2REC-	2GND60	2GND61	BAC10	BAC08	BAC08	
U	HERE#	2SCAN2	2DYND	2RSRV	2CARDT	2IFMD+	2DY+	2PARI	2RSTRT	2RSTRT	2GND60	2GND61	BAC10	BAC08	BAC08	
V		2HERND		2STRDY	2STRDY	2STRDY	2STRDY		2LDFR	2LDFR	2LDFR	2LDFR	2LDFR	2LDFR	2LDFR	

TABLE II-17.

PANEL 4... PORT 2/LINE ADAPTOR 3

A1	A02	A03	A04	A05	A06	A07	A08	A09	A10	A11	A12	A13	A14	A15	A16
A	W2C1C	E1A8	R111	W501	R111	R001	R302	R111	R201	R205	R205	R205	R205	R2C1	R205
B															
C															
D	3GND02	3GND02	3RD+	3GND04	3SCK	3SCK	3REC-	3SCK	3SCK	3SCK	3SCK	3SCK	3SCK	3SCK	3SCK
E	3SDB	3GND02	3RD+	3SCK	3SCK	3SCK	3REC-	3SCK	3SCK	3SCK	3SCK	3SCK	3SCK	3SCK	3SCK
F	3R53	3RINGB	3REC	3SCK	3SCK	3SCK	3REC-	3SCK	3SCK	3SCK	3SCK	3SCK	3SCK	3SCK	3SCK
G	3R53	3RINGB	3REC	3SCK	3SCK	3SCK	3REC-	3SCK	3SCK	3SCK	3SCK	3SCK	3SCK	3SCK	3SCK
H	3R53	3RINGB	3REC	3SCK	3SCK	3SCK	3REC-	3SCK	3SCK	3SCK	3SCK	3SCK	3SCK	3SCK	3SCK
I	3R53	3RINGB	3REC	3SCK	3SCK	3SCK	3REC-	3SCK	3SCK	3SCK	3SCK	3SCK	3SCK	3SCK	3SCK
J	3R53	3RINGB	3REC	3SCK	3SCK	3SCK	3REC-	3SCK	3SCK	3SCK	3SCK	3SCK	3SCK	3SCK	3SCK
K	3R53	3RINGB	3REC	3SCK	3SCK	3SCK	3REC-	3SCK	3SCK	3SCK	3SCK	3SCK	3SCK	3SCK	3SCK
L	3R53	3RINGB	3REC	3SCK	3SCK	3SCK	3REC-	3SCK	3SCK	3SCK	3SCK	3SCK	3SCK	3SCK	3SCK
M	3R53	3RINGB	3REC	3SCK	3SCK	3SCK	3REC-	3SCK	3SCK	3SCK	3SCK	3SCK	3SCK	3SCK	3SCK
N	3R53	3RINGB	3REC	3SCK	3SCK	3SCK	3REC-	3SCK	3SCK	3SCK	3SCK	3SCK	3SCK	3SCK	3SCK
O	3R53	3RINGB	3REC	3SCK	3SCK	3SCK	3REC-	3SCK	3SCK	3SCK	3SCK	3SCK	3SCK	3SCK	3SCK
P	3R53	3RINGB	3REC	3SCK	3SCK	3SCK	3REC-	3SCK	3SCK	3SCK	3SCK	3SCK	3SCK	3SCK	3SCK
Q	3R53	3RINGB	3REC	3SCK	3SCK	3SCK	3REC-	3SCK	3SCK	3SCK	3SCK	3SCK	3SCK	3SCK	3SCK
R	3R53	3RINGB	3REC	3SCK	3SCK	3SCK	3REC-	3SCK	3SCK	3SCK	3SCK	3SCK	3SCK	3SCK	3SCK
S	3R53	3RINGB	3REC	3SCK	3SCK	3SCK	3REC-	3SCK	3SCK	3SCK	3SCK	3SCK	3SCK	3SCK	3SCK
T	3R53	3RINGB	3REC	3SCK	3SCK	3SCK	3REC-	3SCK	3SCK	3SCK	3SCK	3SCK	3SCK	3SCK	3SCK
U	3R53	3RINGB	3REC	3SCK	3SCK	3SCK	3REC-	3SCK	3SCK	3SCK	3SCK	3SCK	3SCK	3SCK	3SCK
V	3R53	3RINGB	3REC	3SCK	3SCK	3SCK	3REC-	3SCK	3SCK	3SCK	3SCK	3SCK	3SCK	3SCK	3SCK

TABLE II-18.

PANEL 4 PORT 2/LINE ADAPTOR 3

	A17	A18	A19	A20	A21	A22	A23	A24	A25	A26	A27	A28	A29	A30	A31	A32
A	R202	R122	R123	R201	R2C1	R2C1	R2C5	R2C5	R2C5	R2C5	R123	R123	W954	R123	R111	
B																
C																
D	3FR3+	3SR06+	3SR06+	3INVMK	3ACAC	3START	3INVMK	3INVMK	3STCK	3BRKDN	3RSV+	3EBPC+	3SCAN1+	3CFR3+	3ADR08	
E	3DY-	3SR01+	3SR07+	3INVMK	3ACAC	3START	3INVMK	3INVMK	3CLSD-	3RCSC-	3DLST+	3IFMC+	3SCAN1-	3CFR2+	3BKSL3	
F		BKSL3	BKSL3	EAC07	3GND15	3GND20	3PWCLR	3PWCLR	3PWCLR	3PWCLR	3ENBL+	3ENBL+	3SCAN2+	3ENAX+		
H	3LINE-	DART00	DART06	3REC-			3PAR1	3PAR1	3CLSD+	3R0SE+	EAC07	EAC07	3SCAN3-	EAC09	DIAD08	
J	3LINE+	DART01	DART07	3XMT+			3EBPC+	3PAR+	3CLSD+	3R0SE+	EAC01	EAC07	3SCAN3+	EAC09		
K	3LOCK	3SR02+	3SR08+	3PWCLR	3F4CLF	3PWCLR	BAC76	BAC76	3CS+	3XTRQ-	3PAR+	3STRDY	3SCAN3-	3CFR1+	3ADR09	
L	3LINE+	3SR03+	3SR05+	3IFMD+	3BKRRQ+		3CLCK	3CLCK	3CS+	3XTRQ+	3R0SD+	3TRM0+	3SCAN1	3CFR0+	3BKSL3	
M	3FRZE	BKSL3	BKSL3	3IFMD-			3CLCK	3CLCK	3CS+	3XTRQ+	3R0SD+	3TRM0+	3SCAN2	3ENAX+		
N	3FR3+	DART02	DART03	3IFMD-			3CLCK	3CLCK	3CS+	3XTRQ+	3R0SD+	3TRM0+	3SCAN2	3ENAX+		
P	3PATY-	DART03	DART04	3INVMK	3FR3+	3REC-	3INVMK	3INVMK	3SKSV+	3XTRQ+	EAC03	EAC09	3ADR08	EAC11		
R		3SR04+	3SR11+	BAC07	3IFMD-	3XMT+	3SKSV+	3XTRQ+	3SKSV+	3XTRQ+	3XTRQ+	3RING	3ADR09	3RQSD+	3ADR10	
S	3PTRF+	3SR05+	3SR11+	3CLCK	3START	3XMT+	3SKSV-	3FSRSV	3FSRSV	3XTRQ-	3XTRQ+	3RING	3ADR09	3RQSD+	3BKSL3	
T		BKSL3	BKSL3	3UTSY-	3XMT-	3KLC+	3SKSV-	3FSRSV	3FSRSV	3XTRQ-	3XTRQ+	3RING	3ADR09	3RQSD+	3BKSL3	
U	3FR3+	DART04	DART05	3XMT-			BACTY	BACTY	BACTY	BACTY	BACTY	BACTY	BACTY	BACTY	DIAD11	DIAD10
V	3PATY+	DART05	DART11	3REC+			BACTY	BACTY	BACTY	BACTY	BACTY	BACTY	BACTY	BACTY	DIAD11	DIAD10
							3CHRDN	3CHRDN	3CHRDN	3CHRDN	3CHRDN	3CHRDN	3CHRDN	3CHRDN		
B17	B18	B19	B20	B21	B22	B23	B24	B25	B25	B26	B27	B28	B29	B30	B31	B32
R111	R002	R001	R111	R121	R121	R121	R001	R111	R111	R603	R602	R205	R205	R205	R205	
A																
B																
C																
D	3RSV+	3BLCK	3TRK0+	3RQSD+			CTAD1	3SCAN1	3STCK	3BRKDN	3RSV+	3EBPC+	3SCAN1+	3CFR3+	3ADR08	
E	3SYN+	3SCAN-	3XMTN	3CLSU+			2RLN	3SCAN2	3CLSD-	3RCSC-	3DLST+	3IFMC+	3SCAN1-	3CFR2+	3BKSL3	
F	3SNIND	3SNIND	3CARDT	3XMTN			3ELCK	3BLND	3PWCLR	3PWCLR	3ENBL+	3ENBL+	3SCAN2+	3ENAX+		
H	3SNSVC	3SCAN1	3XMTN	3XMT-			3ELCK	3BLND	3PAR1	3RS1	EAC07	EAC07	3SCAN2-	EAC08	DIAD08	
J	3RSV+	3SCAN2	3STRDY	3XMT-			3ELCK	3BLND	3PAR1	3RS1	EAC07	EAC07	3SCAN3-	EAC09		
K	3SNIND	3XMTN	3XMT-	3REC+			3ELCK	3BLND	3PAR1	3RS1	EAC07	EAC07	3SCAN3+	EAC09		
L	3XMT+	3BLCK	3FR2+	3REC+			3ELCK	3BLND	3PAR1	3RS1	EAC07	EAC07	3SCAN3-	EAC09		
M	3SN2ND	3SCAN+	3CYNE	3DY-			3ELCK	3BLND	3PAR1	3RS1	EAC07	EAC07	3SCAN3-	EAC09		
N	3SN2ND	3SCAN+	3CYNE	3DY-			3ELCK	3BLND	3PAR1	3RS1	EAC07	EAC07	3SCAN3-	EAC09		
P	3SN2ND	3SCAN+	3CYNE	3DY-			3ELCK	3BLND	3PAR1	3RS1	EAC07	EAC07	3SCAN3-	EAC09		
R	3SCAN2	3EBPC+	3REC+	3REC-			3ELCK	3BLND	3PAR1	3RS1	EAC07	EAC07	3SCAN3-	EAC09		
S	3SCAN3	3SN2ND	3DYND	3IFMD+			3ELCK	3BLND	3PAR1	3RS1	EAC07	EAC07	3SCAN3-	EAC09		
T	3HERND	3SCAN1	3IFMD+	3CLSL-			3ELCK	3BLND	3PAR1	3RS1	EAC07	EAC07	3SCAN3-	EAC09		
U	HERE#	3SCAN2	3DYND	3ESRSV			3ELCK	3BLND	3PAR1	3RS1	EAC07	EAC07	3SCAN3-	EAC09		
V		3HERNE		3STRDY			3ELCK	3BLND	3PAR1	3RS1	EAC07	EAC07	3SCAN3-	EAC09		

TABLE II-19.

	A01	A02	A03	A04	A05	A06	A07	A08	A09	A10	A11	A12	A13	A14	A15	A16
A	W201C	EIAR	R111	W501	R111	R0C1	R3C2	R111	R201	R2C5	R205	R205	R2C5	R205	R201	R205
B																
C																
D	4SDB	4GND02	4RD+	4SRCK	4SCRF+	4REC-	4GND04	4RECE-	4SR00+	4SR00+	4SR02+	4SR04+	4SR06+	4SR08+	4SR11+	4GND14
E	4RDB	4RINGB	4REC+	4SRCK	4LINE+	40TND1	4RQSD+	4RD+	4SR00-	4SR00-	4SR02-	4SR04-	4SR06-	4SR08-	4SR11-	4SHIF
F	4RSB	4RING	4REC-	4SRCK	4CIND1	4REC-	4GND06	4REC+	4SR00-	4SR00-	4SR02-	4SR04-	4SR06-	4SR08-	4SR11-	4SDBF+
H	4CSDB	4RING	4RD-	4SRCK	4CUTI	40TND2	4A06JK	4REC+	4SR00+	4SR00+	4SR02+	4SR04+	4SR06+	4SR08+	4SR11+	4GND14
J	4SRDB	4RING	4RD-	4SRCK	4CUTI	4REC-	4A06JK	4REC+	4SR00+	4SR00+	4SR02+	4SR04+	4SR06+	4SR08+	4SR11+	4GND14
K	4TRDYB	4GND02	4DLST+	4SRCK	4PTBF+	4RSND	4A06JK	4XMT-	4SR00+	4SR00+	4SR02+	4SR04+	4SR06+	4SR08+	4SR11+	4GND14
L	4RINGB	4CSDB	4GND04	4SRCK	4LINE-	4RSND	4A06JK	4XMT-	4SR00+	4SR00+	4SR02+	4SR04+	4SR06+	4SR08+	4SR11+	4GND14
M	4CCETE	4CS+	4DALST	4L04	4CTND2	4RSND	4A06JK	4XMT+	4SR00-	4SR00-	4SR02-	4SR04-	4SR06-	4SR08-	4SR11-	4GND14
N	4CS+	4CS+	4DALST	4L04	4CTND2	4RSND	4A06JK	4XMT+	4SR00-	4SR00-	4SR02-	4SR04-	4SR06-	4SR08-	4SR11-	4GND14
P	4SCTB	4CS+	4DALST	4L04	4CTND2	4RSND	4A06JK	4XMT+	4SR00-	4SR00-	4SR02-	4SR04-	4SR06-	4SR08-	4SR11-	4GND14
R	4SCRB	4GND02	4BFX	4SCRB	4XMT-	4RSND	4A06JK	4XMT-	4SR00-	4SR00-	4SR02-	4SR04-	4SR06-	4SR08-	4SR11-	4GND14
S	4SRDB	4SRDB	4GND02	4BFX	4XMT-	4RSND	4A06JK	4XMT-	4SR00-	4SR00-	4SR02-	4SR04-	4SR06-	4SR08-	4SR11-	4GND14
T	4STRDY	4DELAY	4STRDY	4SRDB	4XTEC+	4RSND	4A06JK	4XMT-	4SR00-	4SR00-	4SR02-	4SR04-	4SR06-	4SR08-	4SR11-	4GND14
U	4HERE	4STRDY	4STRDY	4SRDB	4XTEC+	4RSND	4A06JK	4XMT-	4SR00-	4SR00-	4SR02-	4SR04-	4SR06-	4SR08-	4SR11-	4GND14
V																
	B01	B02	B03	B04	B05	B06	B07	B08	B09	B10	B11	B12	B13	B14	B15	B16
	W602	EIAR	W602	W501	W5C1	R202	R6C2	R6C2	R602	R602	R202	R107	R107	R121	R111	R002
A																
B																
C	4GND34	4GND34	4SCTE	4SCK	4CCTD	4CCTD	4CCTD	4CCTD	4GND43	4SR03+	4SR03+	4SR05+	4SR07+	4SR09+	4SR11+	4SR13+
D	4JUT1	4GND34	4SCTE	4SCK	4CCTD	4CCTD	4CCTD	4CCTD	4SR03+	4SR03+	4SR05+	4SR07+	4SR09+	4SR11+	4SR13+	4SR15+
E	4SDB	4RDB	4SCTB	4SCK	4CCTD	4CCTD	4CCTD	4CCTD	4SR03+	4SR03+	4SR05+	4SR07+	4SR09+	4SR11+	4SR13+	4SR15+
F	4RQSD+	4RDBI	4RDBI	4RDBI	4RDBI	4RDBI	4RDBI	4RDBI	4SR03+	4SR03+	4SR05+	4SR07+	4SR09+	4SR11+	4SR13+	4SR15+
H	4RQSD+	4RDBI	4RDBI	4RDBI	4RDBI	4RDBI	4RDBI	4RDBI	4SR03+	4SR03+	4SR05+	4SR07+	4SR09+	4SR11+	4SR13+	4SR15+
J	4RDB	4RDBI	4RDBI	4RDBI	4RDBI	4RDBI	4RDBI	4RDBI	4SR03+	4SR03+	4SR05+	4SR07+	4SR09+	4SR11+	4SR13+	4SR15+
K	4RDB	4RDBI	4RDBI	4RDBI	4RDBI	4RDBI	4RDBI	4RDBI	4SR03+	4SR03+	4SR05+	4SR07+	4SR09+	4SR11+	4SR13+	4SR15+
L	4TRDYB	4CDETB	4CDETB	4CDETB	4CDETB	4CDETB	4CDETB	4CDETB	4SR03+	4SR03+	4SR05+	4SR07+	4SR09+	4SR11+	4SR13+	4SR15+
M	4TRDYB	4CDETB	4CDETB	4CDETB	4CDETB	4CDETB	4CDETB	4CDETB	4SR03+	4SR03+	4SR05+	4SR07+	4SR09+	4SR11+	4SR13+	4SR15+
N	4TRDYB	4CDETB	4CDETB	4CDETB	4CDETB	4CDETB	4CDETB	4CDETB	4SR03+	4SR03+	4SR05+	4SR07+	4SR09+	4SR11+	4SR13+	4SR15+
P	4V+B01	4CDETB	4CDETB	4CDETB	4CDETB	4CDETB	4CDETB	4CDETB	4SR03+	4SR03+	4SR05+	4SR07+	4SR09+	4SR11+	4SR13+	4SR15+
R	4V+B01	4CDETB	4CDETB	4CDETB	4CDETB	4CDETB	4CDETB	4CDETB	4SR03+	4SR03+	4SR05+	4SR07+	4SR09+	4SR11+	4SR13+	4SR15+
S	4V+B01	4CDETB	4CDETB	4CDETB	4CDETB	4CDETB	4CDETB	4CDETB	4SR03+	4SR03+	4SR05+	4SR07+	4SR09+	4SR11+	4SR13+	4SR15+
T	4V+B01	4CDETB	4CDETB	4CDETB	4CDETB	4CDETB	4CDETB	4CDETB	4SR03+	4SR03+	4SR05+	4SR07+	4SR09+	4SR11+	4SR13+	4SR15+
U	4V+B01	4CDETB	4CDETB	4CDETB	4CDETB	4CDETB	4CDETB	4CDETB	4SR03+	4SR03+	4SR05+	4SR07+	4SR09+	4SR11+	4SR13+	4SR15+
V	4V+B01	4CDETB	4CDETB	4CDETB	4CDETB	4CDETB	4CDETB	4CDETB	4SR03+	4SR03+	4SR05+	4SR07+	4SR09+	4SR11+	4SR13+	4SR15+

TABLE II-20.

PANEL 5 *** PORT 3/LINE ADAPTOR 4

	A17	A18	A19	A20	A21	A22	A23	A24	A25	A26	A27	A28	A29	A30	A31	A32
A	R202	R123	R201	R201	R201	R205	R205	R205	R205	R205	R123	R123	W994	R123	R111	
B																
C																
D	4FR3+	4SR06+	4SR07+	4INVMK	4AEC	4START	4INVMK	4INVMK	4STCK	4BRKDN	4SRSV+	4EBPC+	SCAN1+	4CFR3+	4ADR08	
E	4DY-	4SR01+	4SR07+	4INVMK	4AEC	4START	4INVMK	4INVMK	4CLSD-	4RQSD-	4DLST+	4IFMD+	SCAN1-	4CFR2+	BKSL4	
F		BKSL4	BKSL4	BAC07	4GND15	4GND2C	4PWCLR	4PWCLR	4PWCLR	4PWCLR	4ENBL+	4ENBL+	SCAN2+	4ENAX+		
H	4LINE-	DABT00	DABTC6	4REC-			4EBPC+	4PAR+	4CLSD+	4RQSD+	EAC00	EAC06	SCAN2-	EAC08	DIAD08	
J	4LINE+	DABT01	DABTC7	4XMT+			4BPC+	4PAR+	4PAR+	4RQSD+	EAC01	EAC07	SCAN3+	EAC09		
K	4LOCK	4SR02+	4SR08+	4PWCLR	4PWCLR	4PWCLR	BAC06	EAC02	4CS-	4XTRG-	4PAR+	4STRDY	SCAN3-	4CFR1+	4ADR09	
L	4LINE+	4SR03+	4SR05+	4IFMD+	4BKRQ+		BAC06	BAC02	4CS+	4XTRG+	4RQSD+	4TRRD+	4SCAN1	4CFR0+	BKSL4	
M	4FRZE	BKSL4	BKSL4	4IFMD-			4CLCK	4CLCK	ETI	4ENBL+	4ENBL+	4ENBL+	4SCAN2	4ENAX+		
N	4FR3+	DABTC2	DABT08	4RSTKT	4INVMK	4INVMK	4INVMK	4INVMK	4INVMK	4INVMK	EAC02	EAC08	4SCAN3	EAC10	DIAD09	
P	4PATY-	DABT03	DABTC9	4INVMK	4FR3+	4REC-	4TRMC+	4CLST+	4SRSV+	4XTRQ+	EAC03	EAC09	4ADR08	EAC11		
R		4SR04+	4SR10+	BAC07	4IFMC-	4XMT+			4SRSV-	4XTRQ-	4XTRQ+	4RING	4ADR09	4RQSD+	4ADR10	
S	4PIBF+	4SR05+	4SK11+	4CLCK	4START	4XMT+			4SRSV-	4ESRSV	4CLSD+	4CARDI	4ADR10	4RQSD+	BKSL4	
T		BKSL4	BKSL4	4DTSY-	4XMT-	4REC+	BACTY	BAC01	BAC00	BAC04	4ENBL+	4ENBL+	BKSL4			
U	4FR3+	DABT04	DABT10	4XMT-			BACTY	BAC01	BAC00	BAC04	EAC04	EAC10	DIAD11	DIAD10		
V	4PATY+	DABTC5	DABT11	4REC+			BACTY	BAC01	BAC00	BAC04	EAC05	EAC11	DICTL			

	B17	B18	B19	B20	B21	B22	B23	B24	B25	B26	B27	B28	B29	B30	B31	B32
A	R111	R002	R001	R111	R121	R121	R121	R121	R111	R603	R602	R205	R205	R205	R205	
B																
C																
D	4SRSV+	4BLOCK	4TRMD+	4RQSD+					4GND59	4GND60	4GND61	4GND60	4GND60	4GND61	4LDAUX	4LDAUX
E	4RSYN+	4SCAN-	4XMTND	4CLSD+					4BLND	4SCAN2	4ENBL-	4CLCK	4CLCK	4FR1+	4CFR0-	4CFR2-
F	4SNLND	4SNLND	4CARDT	4XMTND					4BLCK	4BLND	4INVMK	4FRZE	4FRZE	4PWCLR	4PWCLR	
H	4SNLND	4SCAN1	4XMTND	4XMT-	4ENZR	4ADAC	4ADAC	4ADAC	4BLND	4ENBL-	4SVC-	4CFR0-	4CFR2-			
J	4SRSV+	4SNLNE	4XMTND	4FR3+	4REC+	4SK11+	4ADACC	4ADACC	4ENBL-	4ENBL-	4GND59	4FRQ+	4FR2+	4CFR0+	4CFR2+	
K	4XMT+	4BLOCK	4FR2+	4FRQ+	4IFMD+	4FR3+	4FR3+	4FR3+	4XND	4SCAN1	4ZROSR	4FRZE	4FRZE	4GND61	BAC11	BAC09
L	4XMT+	4BLOCK	4FR2+	4FRQ+	4IFMD+	4FR3+	4FR3+	4FR3+	4XND	4SCAN1	4ZROSR	4FRZE	4FRZE	4GND61	BAC11	BAC09
M	4SNZND	4SCAN+	4DYNC	4CYND	4IFMC+	4REC+	BKSL4	BKSL4	4XND	4XND	4LDFR	4LDFR	4LDFR	4LDFR		
N	4SNLND	4SNZND	4FR1+	4DY-	4XTRQ+	4REC+	4BREA	4BREA	4XND	4XND	4LDFR	4LDFR	4LDFR	4LDFR		
P	4SCAN1	4DYNC	4DY-	4XMT+	4IFMD+	4BTIC	4PARND	4ENAX-	4ENAX-	4ENAX-	4IFMD-	4FR1+	4FR3+	4CFR1+	4CFR3+	
R	4SCAN2	4EBPC+	4REC+	4RECE-	4ESRSV	4PAR1	4DY+	4DY+	4RD+	4RD+	4XMT-	4XMT-	4CFR1-	4CFR3-		
S	4SCAN3	4SNZND	4DYNC	4IFMD+	4IFMD+	4FRD-	4PARND	4ENAX-	4ENAX-	4ENAX-	4IFMD+	4CFR1-	4CFR3-			
T	4HERND	4SCAN1	4IFMD+	4CLSC-	4XTRQ+	4REC+	4PARND	4ENAX-	4ENAX-	4ENAX-	4IFMD+	4CFR1-	4CFR3-			
U	4SCAN2	4DYNC	4ESRSV	4CARDT	4IFMD+	4DY+	4PAR1	4PAR1	4PAR1	4PAR1	4RSTRT	4GND60	4GND61	BAC10	BAC08	BAC08
V	4HERND	4SCAN2	4DYNC	4STRDY	4PATY+	4PATY+	4PATY+	4PATY+	4PATY+	4PATY+	4LDFR	4LDFR	4LDFR	BAC10	BAC08	BAC08

TABLE II-21.

APPENDIX III

PDP-8/201A LINE ADAPTOR INTERFACE
FOR USE WITH A
PDP-8 WITHOUT USING THE DATA-BREAK FACILITY

APPENDIX III

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APPENDIX III

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APPENDIX III

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PDP-8/201A LINE ADAPTOR INTERFACE
FOR USE WITH A
PDP-8 WITHOUT USING THE DATA-BREAK FACILITY

The only difference between this version of the 201A communication adaptor and the basic 201A communication adaptor presented in Appendix I is that it uses a character buffer internal to the 201A line adaptor interface instead of using the data-break facility and PDP-8 core buffers. This necessitates the addition of control circuitry to transfer characters between the SDR register and this internal buffer (BUF) and additional micro-instructions to read, write, and clear BUF. The additional device code for the set of IOTs is taken to be the fourth in the set used by 201A communication adaptor (see Programming and Control Considerations).

This set of IOTs is defined as follows:

Read Character Buffer (6XX1)

This micro-instruction causes the contents of the 201A line adaptor character buffer to be logically ORed to the accumulator.

Clear Character Buffer (6XX2)

This micro-instruction causes the 201A line adaptor character buffer to be cleared.

Write Character Buffer (6XX4)

This micro-instruction causes the contents of the PDP-8 accumulator to be loaded into the 201A line adaptor character buffer (BUF).

In order to use the same basic 201A line adaptor, the data break control signals were simulated, except that the transfer is to and from BUF instead of core. The remainder of the Appendix presents the detailed logic circuits with a brief description of their function.

Pseudo Data-Break Control (Diagram III-1)

Through the #BKRQ flip-flop, the line adaptor initiates the transfer to or from the SDR register from or to the BUF register. When #BKRQ is set, the direction of transfer is specified by the DICTL signal. The #BKRQ flip-flop is cleared by the first BT1 pulse after it is set. The next BT1 pulse is used to generate the #BRKDN signal which causes the reading or strobing of the BUF register. The #BRKQ flip-flop is set each time the frame counter overflows while in the text state and when the line adaptor first enters the transmit state to fetch the first character to be transmitted. All of the logic in Diagram III-1 is in Bay 2 of the interface.

Control Gating (Diagram III-2)

The PDP-8's address-accepted signal is simulated by the ADRAC flip-flop, and the buffered-break signal is effected by the BBRK flip-flop. The sequencing through the states effected by BBRK and ADRAC is accomplished by the BT1, and BT2 pulses. The BUF register is cleared by a PDP-8 power clear signal, an explicit IOT, and by the interface before it loads the SDR register into it. The signal used to load the SDR register into BUF is READ, while LOAD is generated by the IOT used to write or load BUF from the PDP-8 accumulator.

BUF Register (Diagram III-3)

Diagram III-3 shows the internal buffer register.

BUF Gating (Diagram III-4)

Diagram III-4 shows the drivers and control gating necessary to load the BUF register into the PDP-8 accumulator.

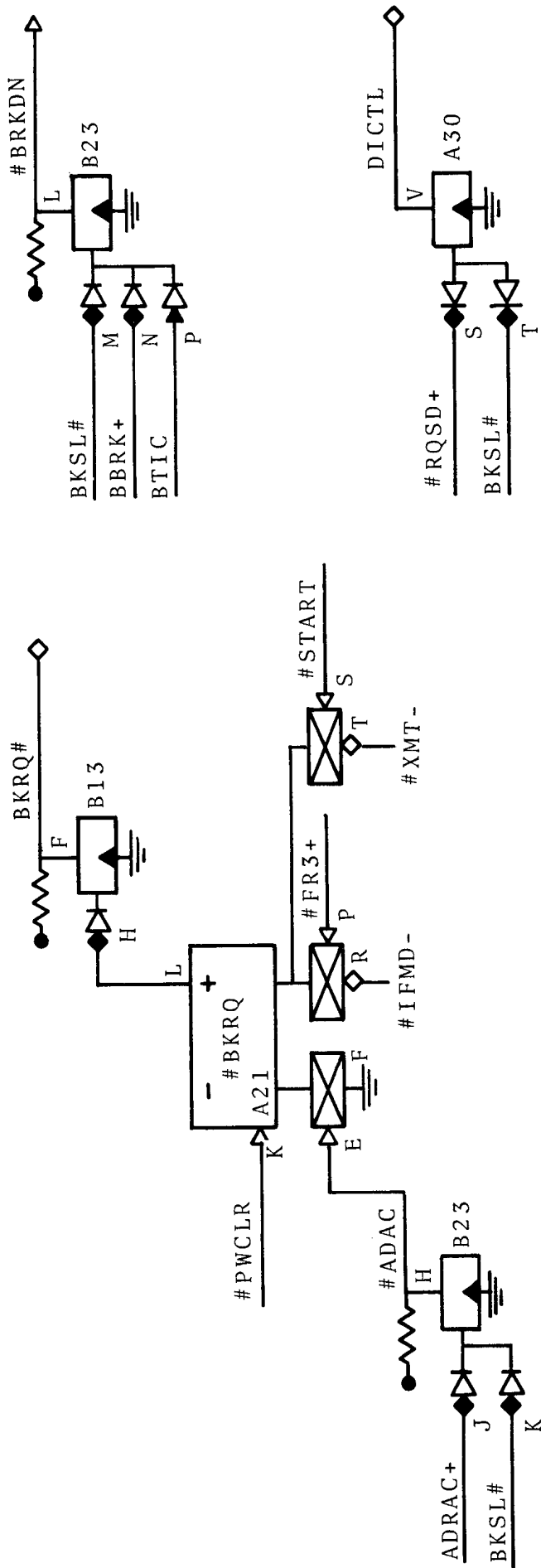


Diagram III-1. PSEUDO DATA BREAK CONTROL

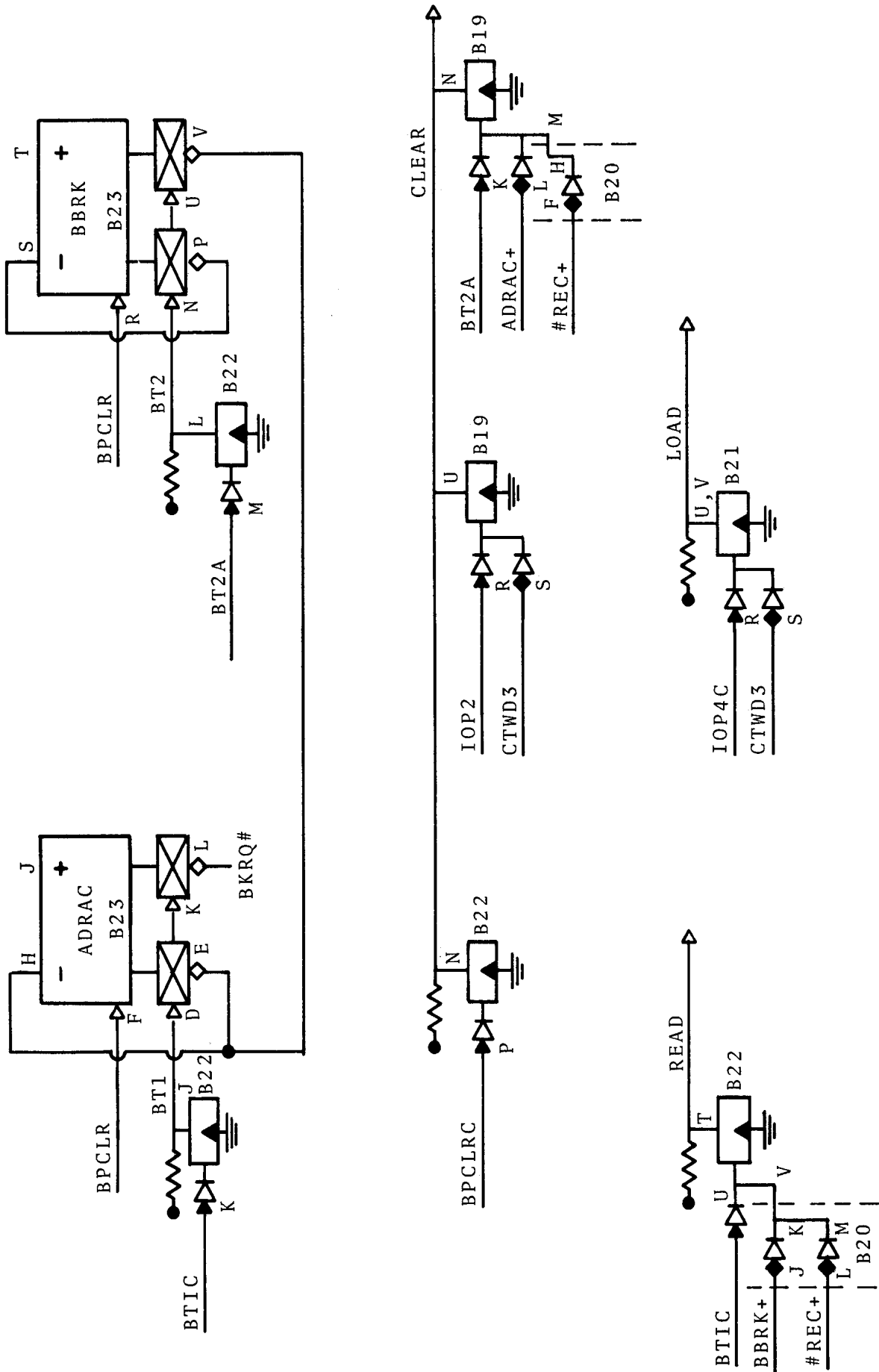


Diagram III-2. CONTROL GATING

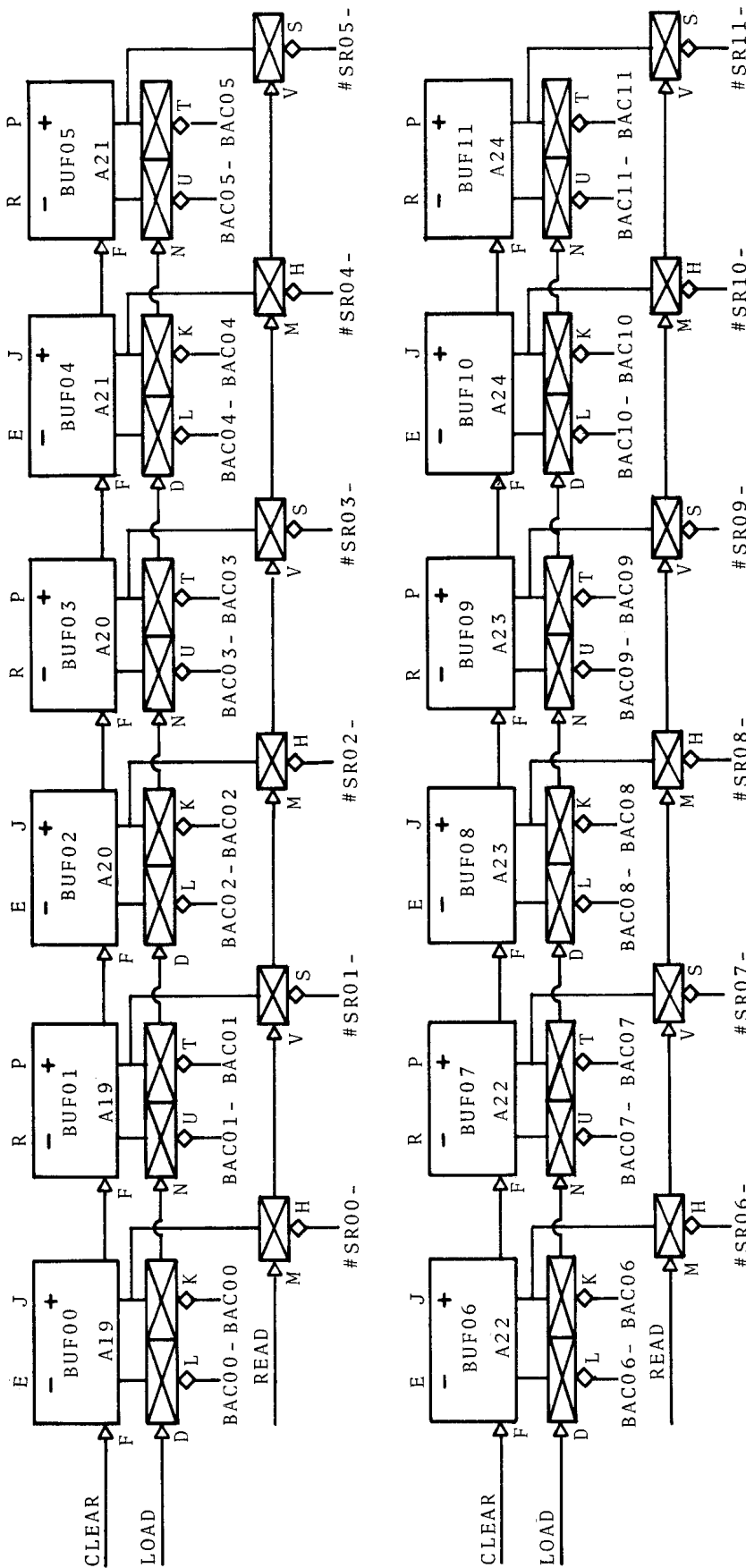


Diagram III-3. BUF REGISTER

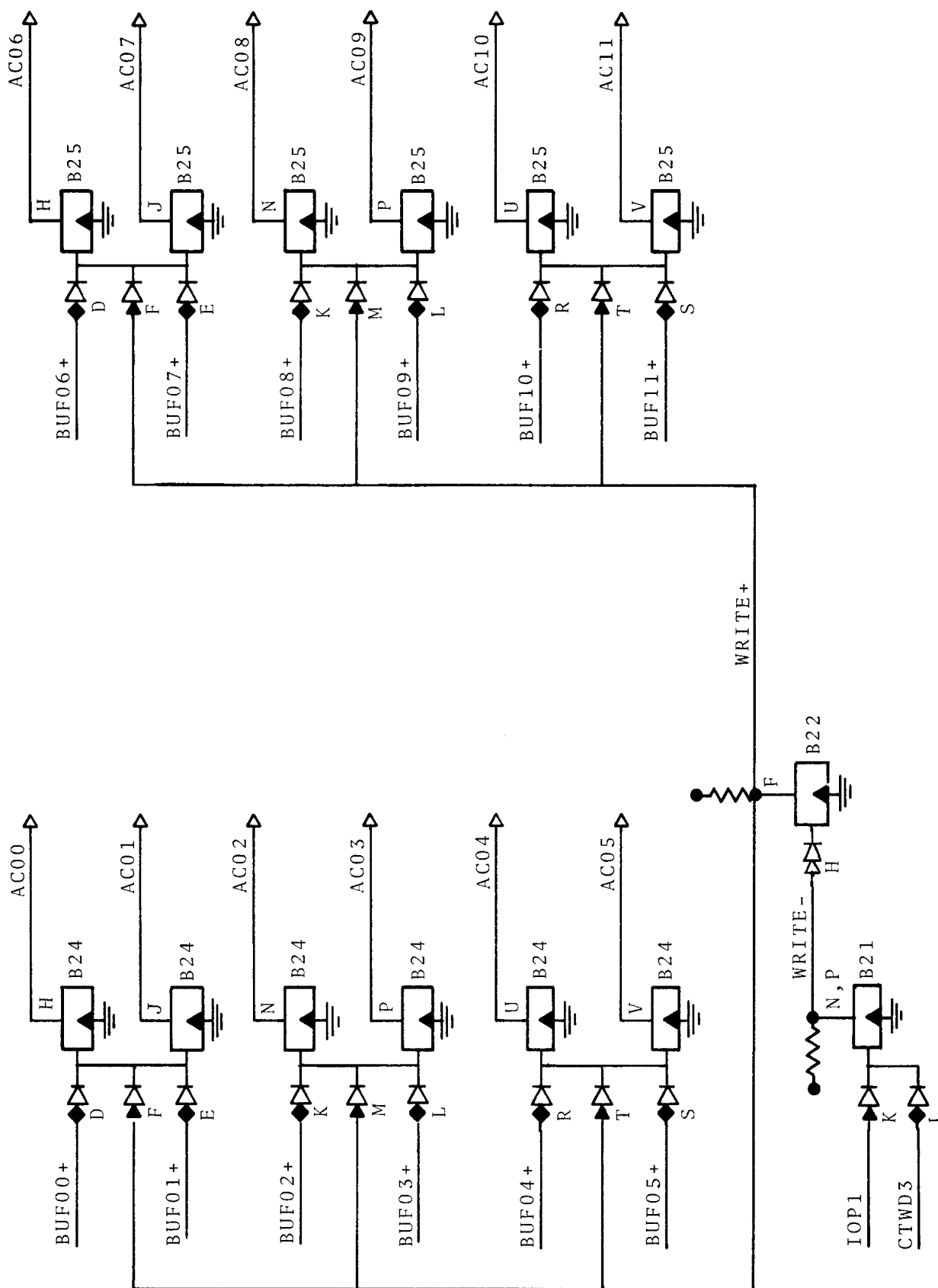


Diagram III-4. BUF GATING

SDR Register (Diagram III-5)

Diagram III-5 is a revision of Diagram 1, described in the report, to reflect the loading of the SDR register from BUF instead from the buffered memory buffer.

Device Select Code (Diagram III-6)

The device select code is a two octal digit number which selects an external device during an input/output operation. The device code appears in positions 3 through 8 of the memory buffer during an IOT instruction, alerting the external device when it is being selected.

This version of the 201A L.A. has associated with it four separate device codes as discussed above. In order to specify the four devices it is sufficient, because of the aforementioned requirements, to define only a four-bit number, which appears in positions 3-6 of the M.B. during an IOT instruction. This number must also be realized in the hardware, and this is accomplished via an R002 diode module.

Thus to specify the desired set of devices codes the appropriate diodes are removed. For example, using the set 40,41,42,43, as before, the diodes connected to pins E, H, L, and P must be removed.

The remainder of Diagram III-6 shows the gating necessary to obtain the signals to identify each of the devices.

Device Selection Gating (Diagram III-7)

The gates shown in Diagram III-7 are located in Bay 2 and provide the signals to differentiate between Control Word 1 and Control Word 2 operation.

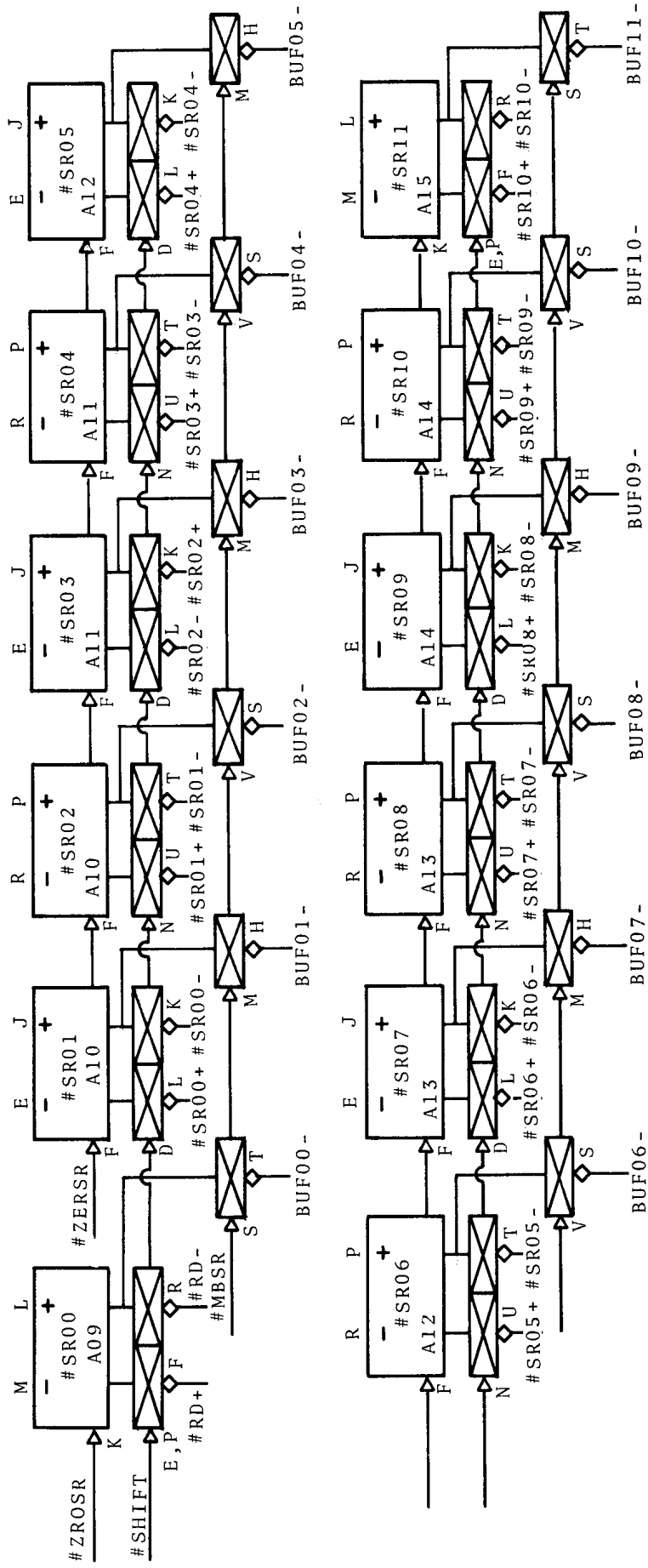


Diagram III-5. SDR REGISTER

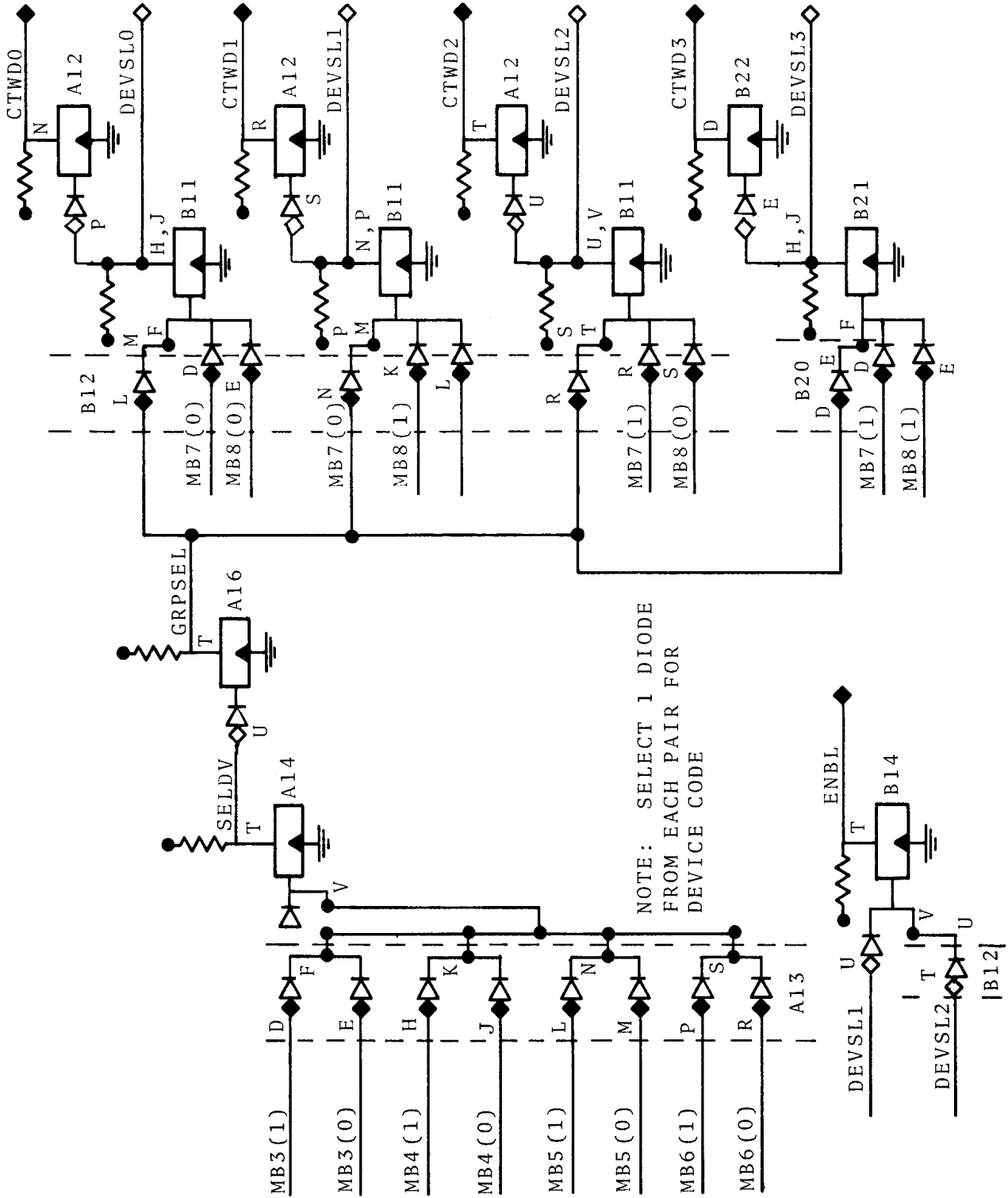


Diagram III-6. DEVICE SELECT CODE

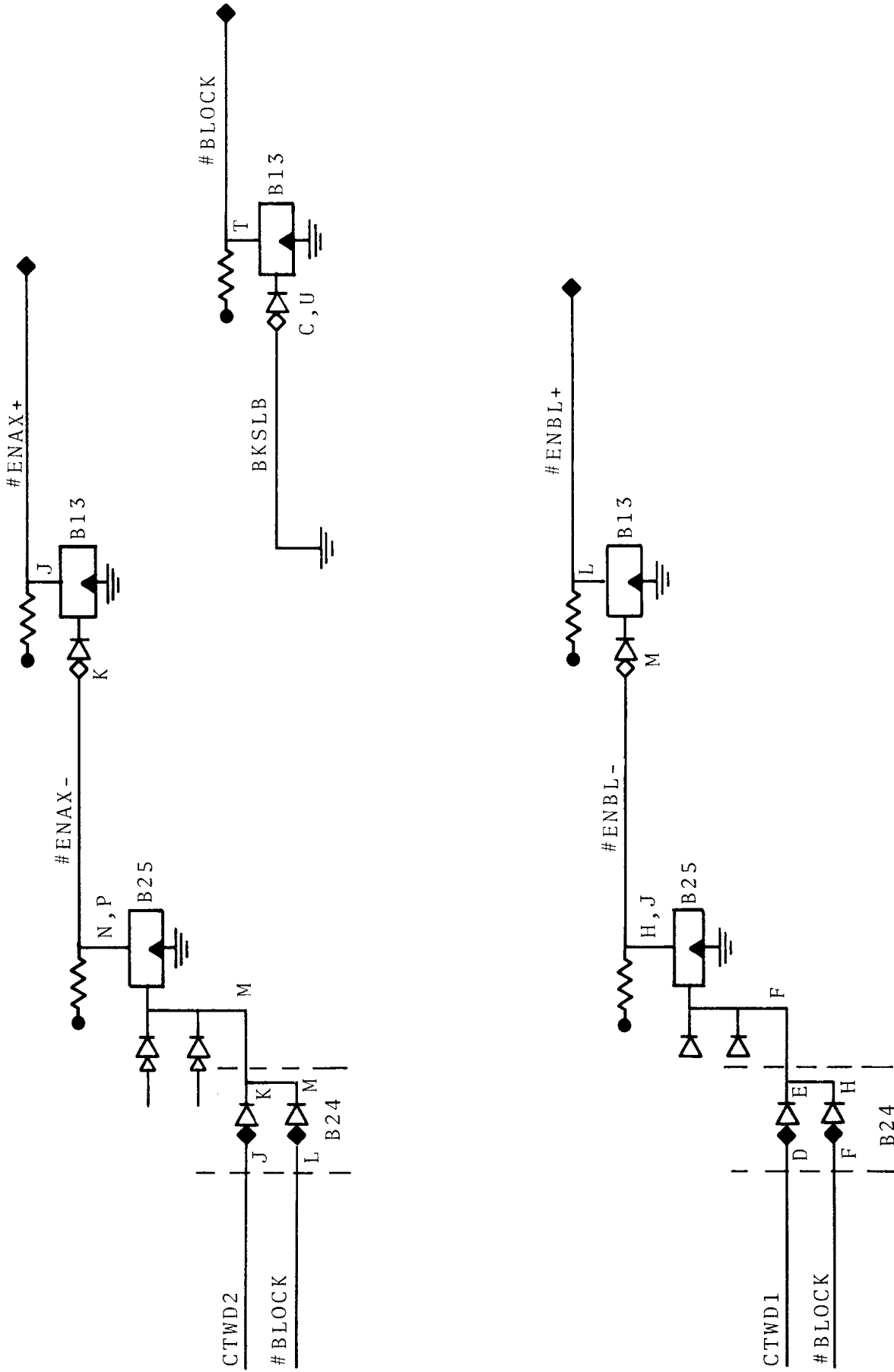


Diagram III-7. DEVICE SELECTION GATING

Interrupt Control (Diagram III-8)

Every time a character is transferred between the 201A L.A. and the BUF register, a character service flag (#SRSV) is set, as described before.

This flag in turn sets the appropriate flag, transmit (XINT) or receive (RINT), which causes an interrupt request. If interrupts are enabled in the PDP-8, a program interrupt is generated. Via the appropriate IOT micro-instruction, the program can identify the device causing the interrupt. The SKIP signal will be generated and a program skip forced if this IOT is executed. It is the program's responsibility to clear the interrupt after it is identified, and the remainder of the gates allow for this.

Extended Accumulator Control (Diagram III-9)

In order to provide the IOT structure described under Programming and Control Considerations, the extended accumulation (EAC) buss was implemented. The full power of the EAC is not realized until there are multiple devices using the buss, since it provides the mechanism for multiple inputs to the PDP-8 AC. Diagram III-9 shows the gating necessary to generate the SKIP signal on a skip under mask IOT.

Accumulator Input Gating (Diagram III-10)

Diagram III-10 shows the buffers which gate the EAC buss onto the AC buss. For other devices to use the EAC buss, they need provide only the appropriate input to the ENBL gate and the gates for the EAC buss.

Extended Accumulator Buffers (Diagram III-11)

Diagram III-11 shows a set of buffers necessary to accomplish the inversion to gate the EAC onto the AC. The clamped loads for the EAC buss are also indicated.

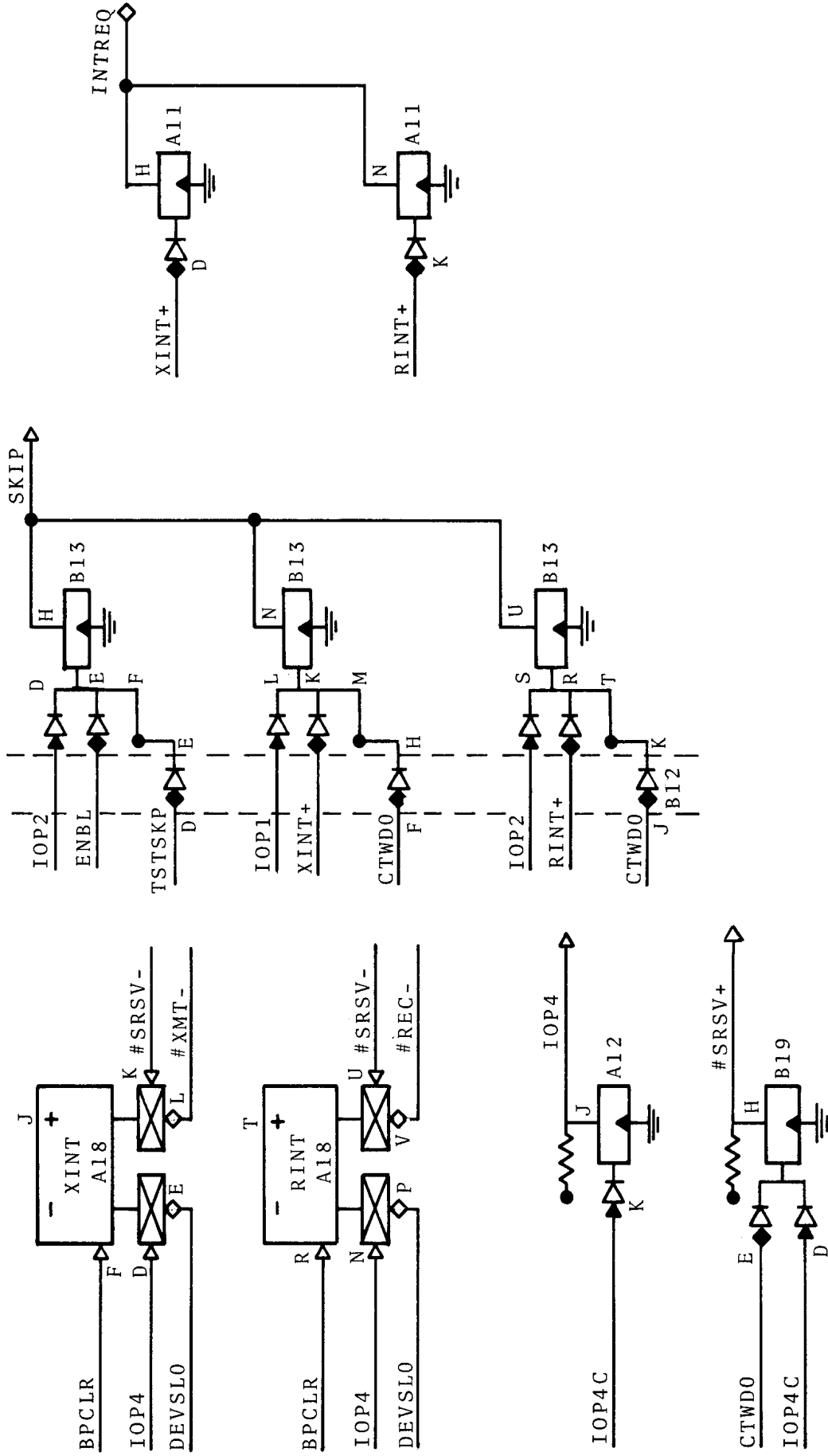


Diagram III-8. INTERRUPT CONTROL

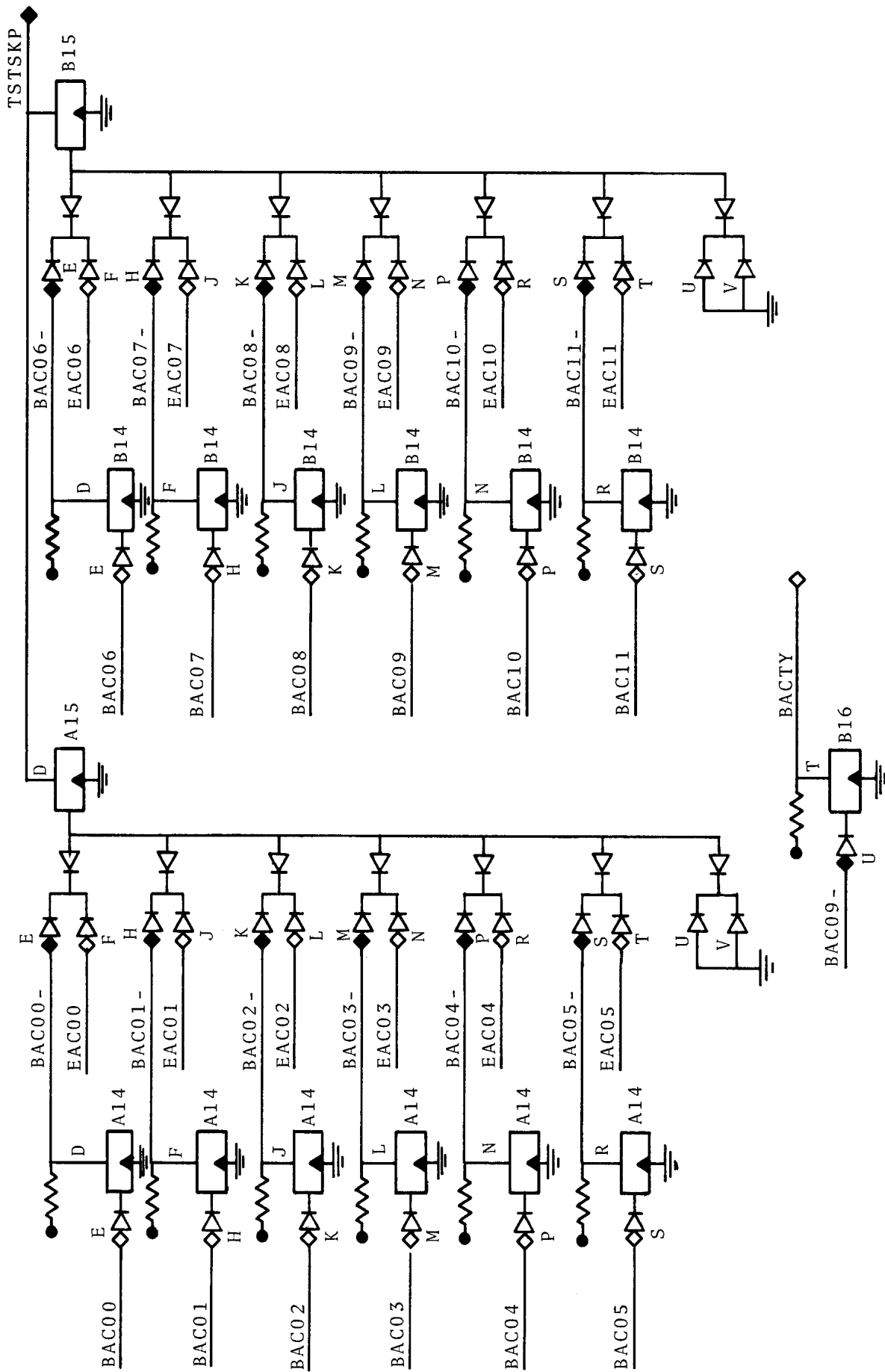


Diagram III-9. EXTENDED ACCUMULATOR CONTROL

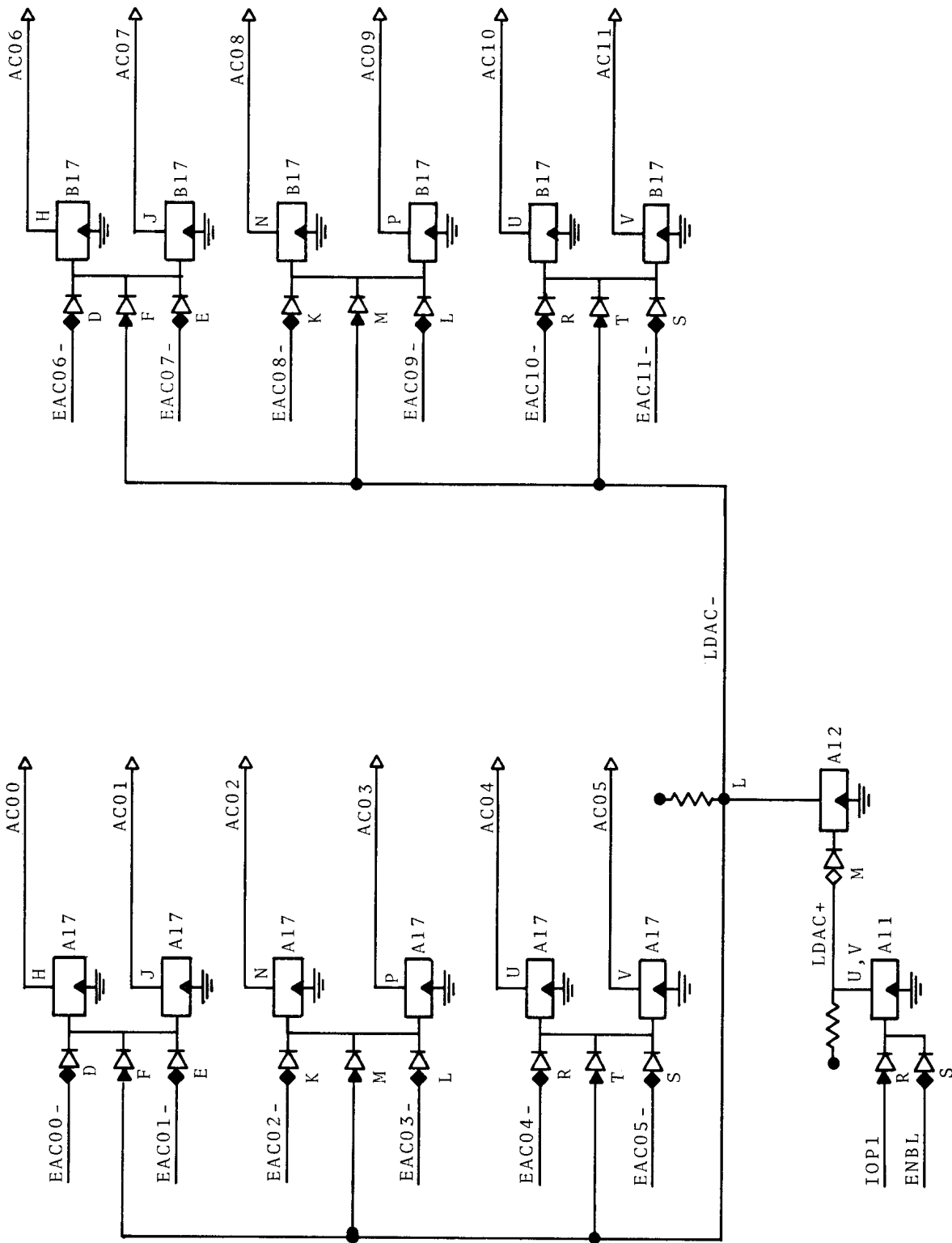


Diagram III-10. ACCUMULATOR INPUT GATING

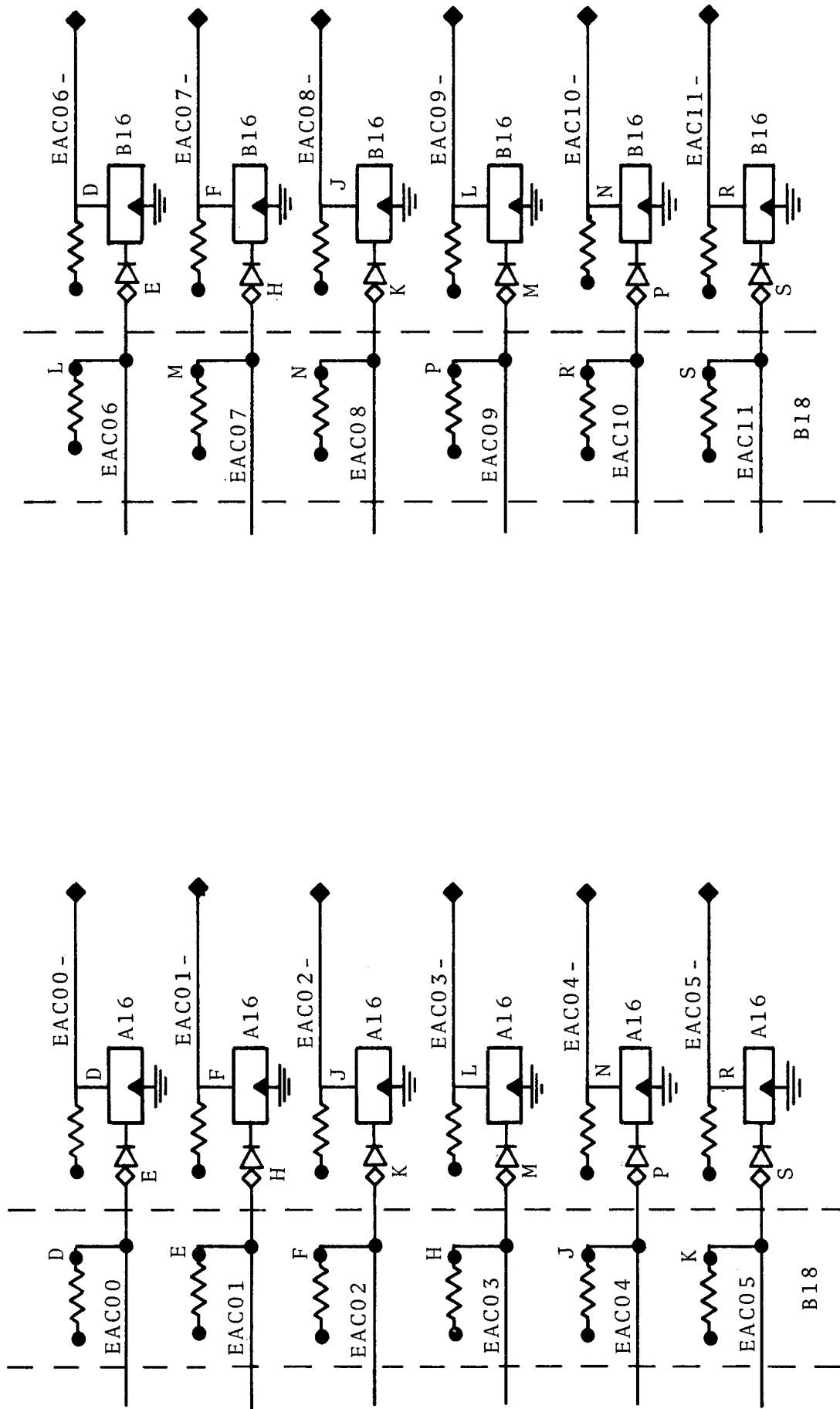


Diagram III-11. EXTENDED ACCUMULATOR BUFFERS

Miscellaneous Circuits (Diagram III-12)

Diagram III-12 is best described as the left-over circuits without a logical home.

Cable Layout (Diagram III-13)

The input/output cables for this version of the 201A line adaptor are shown in Diagram III-13. The correspondence between signal names, module positions, and pin connections for the 201A line adaptor and the PDP-8 are given in Tables III-1 through III-4.

Module Utilization (Tables III-5 through III-8)

Tables III-5 through III-8 give the module utilization for this version of the 201A line adaptor. In addition to the module utilization, a complete signal name map is also shown (Tables III-5 through III-8).

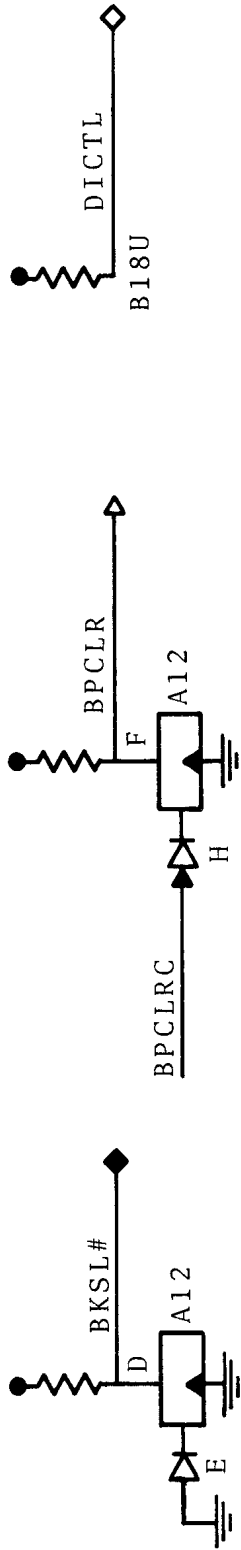


Diagram III-12. MISCELLANEOUS CIRCUITS

	01	02	03	04	05	06
D	BAC00	BMB00	AC00			
E	BAC01	BMB01	AC01			
F	BAC02	BMB02	AC02			
H	BAC03	BMB03 -	AC03			
J	BAC04	BMB03	AC04			
K	BAC05	BMB04 -	AC05			
L	BAC06	BMB04	AC06			
M	BAC07	BMB05 -	AC07			
N	BAC08	BMB05	AC08			
P						
R						
S						
T						
U						
V						

'A'

	01	02	03	04	05	06
D	BAC09	BMB06 -	AC09			
E	BAC10	BMB06	AC10			
F	BAC11	BMB07 -	AC11			
H	IOP1	BMB07	SKIP			
J	IOP2	BMB08 -	INTREQ			
K	IOP4C	BMB08	--			
L	BT1C	BMB09	--			
M	BT2A	BMB10	--			
N	BPCLRC	BMB11	--			
P						
R						
S						
T						
U						
V						

'B'

Diagram III-13. CABLE LAYOUT

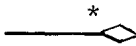
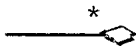
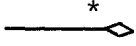
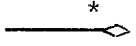
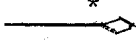
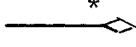
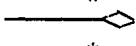
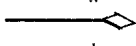
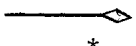
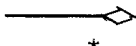
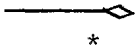
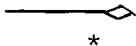
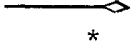
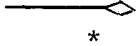
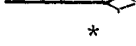
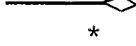
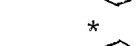
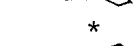
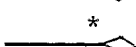
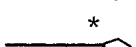
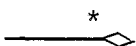
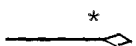


TABLE III-1

BUFFERED ACCUMULATOR OUTPUTS

201A LINE ADAPTOR			PDP-8		
INTERFACE CONNECTION	SIGNAL NAME	LOGIC SYMBOL	LOGIC SYMBOL	SIGNAL NAME	INTERFACE CONNECTION
A01D, A02D	BAC00			BAC0	ME34D
A01E, A02E	BAC01			BAC1	ME34E
A01H, A02H	BAC02			BAC2	ME34H
A01K, A02K	BAC03			BAC3	ME34K
A01M, A02M	BAC04			BAC4	ME34M
A01P, A02P	BAC05			BAC5	ME34P
A01S, A02S	BAC06			BAC6	ME34S
A01T, A02T	BAC07			BAC7	ME34T
A01V, A02V	BAC08			BAC8	ME34V
B01D, B02D	BAC09			BAC9	MF34D
B01E, B02E	BAC10			BAC10	MF34E
B01H, B02H	BAC11			BAC11	MF34H

TABLE III-2

ACCUMULATOR INPUTS

201A LINE ADAPTOR			PDP-8		
INTERFACE CONNECTION	SIGNAL NAME	LOGIC SYMBOL	LOGIC SYMBOL	SIGNAL NAME	INTERFACE CONNECTION
A05D, A06D	AC00			AC0	PE2D
A05E, A06E	AC01			AC1	PE2E
A05H, A06H	AC02			AC2	PE2H
A05K, A06K	AC03			AC3	PE2K
A05M, A06M	AC04			AC4	PE2M
A05P, A06P	AC05			AC5	PE2P
A05S, A06S	AC06			AC6	PE2S
A05T, A06T	AC07			AC7	PE2T
A05V, A06V	AC08			AC8	PE2V
B05D, B06D	AC09			AC9	PF2D
B05E, B06E	AC10			AC10	PF2E
B05H, B06H	AC11			AC11	PF2H

*Note: Collector of Grounded-Emitter Transistor

TABLE III-3

TIMING CONTROL SIGNALS

201A LINE ADAPTOR			PDP-8		
INTERFACE CONNECTION	SIGNAL NAME	LOGIC SYMBOL	LOGIC SYMBOL	SIGNAL NAME	INTERFACE CONNECTION
B01S, B02S	BTIC	→	→	BT1	MF34S
B01T, B02T	BT2A	→	→	BT2A	MF34T
B01V, B02V	BPCLRC	→	→	B POWER CLEAR	MF34V

TABLE III-4

PROGRAMMED INPUT/OUTPUT CONTROL

201A LINE ADAPTOR			PDP-8		
INTERFACE CONNECTION	SIGNAL NAME	LOGIC SYMBOL	LOGIC SYMBOL	SIGNAL NAME	INTERFACE CONNECTION
B05M, B06M	INTREQ	*1 —◇	*1 —◇	INTERRUPT REQUEST	PF2M
B05K, B06K	SKIP	*1 —◇	*1 —◇	SKIP	PF2K
B01K, B02K	IOP1	—▶	—▶	IOP1	MF34K
B01M, B02M	IOP2	—▶	—▶	IOP2	MF34M
B01P, B02P	IOP4C	—▶	—▶	IOP4	MF34P

*Note: Collector of Grounded-Emitter Transistor.

PANEL 1 ... COMMON SECTION (WITHOUT DATA BREAK)

A01	A02	A03	A04	A05	A06	A07	A08	A09	A10	A11	A12	A13	A14	A15	A16
W021	W021	W021	W021	W021	W021	W021	W021	W021	W021	R111	R107	R002	R107	R141	R107
A															
B															
C															
D	BAC00	BAC00	BMB00	BMB00	AC00	AC00				XINT+	GNDAI2	BMB03-	BAC00-	TSTSKP	EAC00-
E	BAC01	BAC01	BMB01	BMB01	AC01	AC01					GNDAI2	BMB03	BAC00	BAC00-	EAC00
F	BAC02	BAC02	BMB02	BMB02	AC02	AC02					BPCLR	SELND	BAC01-	EAC00	EAC01-
G	BAC03	BAC03	BMB03	BMB03-	AC03	AC03				INTREQ	BPCLRC	BMB04-	BAC01	BAC01-	EAC01
H	BAC04	BAC04	BMB04	BMB04-	AC04	AC04					IOPI	BMB04	BAC02-	EAC01	EAC02-
I	BAC05	BAC05	BMB05	BMB05-	AC05	AC05				RINT+	IOPI	SELVD	BAC02	BAC02-	EAC02
J	BAC06	BAC06	BMB06	BMB06-	AC06	AC06					LDAC-	BMB05-	BAC03-	EAC02	EAC03-
K	BAC07	BAC07	BMB07	BMB07-	AC07	AC07				INTREQ	CTWDO	BMB05	BAC03	BAC03-	EAC03
L	BAC08	BAC08	BMB08	BMB08-	AC08	AC08					CTWDO	SELND	BAC04-	EAC03	EAC04-
M											DEVSL0	BMB06-	BAC04	BAC04-	EAC04
N											CTWDO	BMB06	BAC04-	EAC04	EAC05-
O											CTWDO	BMB07	BAC05-	EAC04	EAC05-
P											IOPI	BMB07	BAC05	BAC05-	EAC05
Q											ENBL	SELND	BAC05	BAC05-	EAC05
R											CTWDO	SELND	BAC05	GRPSEL	GRPSEL
S											LDAC+	DEVSL2	SELND	GNDAI5	SELVD
T											LDAC+	DEVSL2	SELND	GNDAI5	SELVD
U															
V															
W01	B01	B02	B03	B04	B05	B06	B08	B09	B10	B11	B12	B13	B14	B15	B16
W02	W021	W021	W021	W021	W021	W021	W021	W021	W021	R111	R001	R111	R107	R141	R107
A															
B															
C															
D	BAC09	BAC09	BMB06-	BMB06-	AC09	AC09				BMB07	TSTSKP	IOPI2	BAC06-	TSTSKP	EAC06-
E	BAC10	BAC10	BMB06	BMB06	AC10	AC10				BMB08	SKIPI	ENBL	BAC06-	BAC06-	EAC06
F	BAC11	BAC11	BMB07-	BMB07-	AC11	AC11				DEVND0	CTWDO	SKIPI	BAC07-	EAC06	EAC07-
G	IOPI	IOPI	BMB07	BMB07	SKIP	SKIP				DEVSL0	CTWDO	SKIP	BAC07	BAC07-	EAC07
H	IOPI	IOPI	BMB07	BMB07	SKIP	SKIP				BMB07	SKIPI	XINT+	BAC08-	EAC07	EAC08-
I	IOPI	IOPI	BMB07	BMB07	SKIP	SKIP				BMB08-	GRPSEL	IOPI	BAC08-	EAC08	EAC08-
J	IOPI	IOPI	BMB07	BMB07	SKIP	SKIP				DEVND1	DEVND0	SKIPI	BAC09-	EAC08	EAC09-
K	IOPI	IOPI	BMB07	BMB07	SKIP	SKIP				DEVSL1	GRPSEL	SKIPI	BAC09	BAC09-	EAC09
L	IOPI	IOPI	BMB07	BMB07	SKIP	SKIP				DEVSL1	GRPSEL	SKIPI	BAC10-	EAC09	EAC10-
M	IOPI	IOPI	BMB07	BMB07	SKIP	SKIP				DEVSL1	DEVND1	SKIPI	BAC10	BAC10-	EAC10
N	IOPI	IOPI	BMB07	BMB07	SKIP	SKIP				BMB07-	GRPSEL	RINT+	BAC11-	EAC10	EAC11-
O	IOPI	IOPI	BMB07	BMB07	SKIP	SKIP				BMB08	DEVND2	IOPI2	BAC11	BAC11-	EAC11
P	IOPI	IOPI	BMB07	BMB07	SKIP	SKIP				DEVND2	DEVSL2	SKIPI	ENBL	EAC11	BACTY
Q	IOPI	IOPI	BMB07	BMB07	SKIP	SKIP				DEVSL2	ENBLND	SKIPI	ENBL	EAC11	BACTY
R	IOPI	IOPI	BMB07	BMB07	SKIP	SKIP				DEVSL2	ENBLND	SKIPI	ENBLND	GND815	BAC09-
S	IOPI	IOPI	BMB07	BMB07	SKIP	SKIP				DEVSL2	ENBLND	SKIPI	ENBLND	GND815	BAC09-
T	IOPI	IOPI	BMB07	BMB07	SKIP	SKIP									
U	IOPI	IOPI	BMB07	BMB07	SKIP	SKIP									
V	IOPI	IOPI	BMB07	BMB07	SKIP	SKIP									

TABLE III-5.

PANEL 2 ... PORT 0/LINE ADAPTOR # (WITHOUT DATA BREAK)

	A17	A18	A19	A20	A21	A22	A23	A24	A25	A26	A27	A28	A29	A30	A31	A32
A																
B																
C																
D																
E																
F																
G																
H																
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K																
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M																
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Q																
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S																
T																
U																
V																

	B17	B18	B19	B20	B21	B22	B23	B24	B25	B26	B27	B28	B29	B30	B31	B32
A																
B																
C																
D																
E																
F																
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M																
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TABLE III-8.

Unclassified

Security Classification

DOCUMENT CONTROL DATA - R&D

(Security classification of title, body of abstract and indexing annotation must be entered when the overall report is classified)

1. ORIGINATING ACTIVITY (Corporate author) THE UNIVERSITY OF MICHIGAN CONCOMP PROJECT		2a. REPORT SECURITY CLASSIFICATION Unclassified	
		2b. GROUP	
3. REPORT TITLE A 201A DATA COMMUNICATION ADAPTOR FOR THE PDP-8: PRELIMINARY ENGINEERING DESIGN REPORT			
4. DESCRIPTIVE NOTES (Type of report and inclusive dates) Technical Report			
5. AUTHOR(S) (Last name, first name, initial) WOOD, David E.			
6. REPORT DATE February 1968		7a. TOTAL NO. OF PAGES 134	7b. NO. OF REFS
8a. CONTRACT OR GRANT NO. DA-49-083 OSA-3050		9a. ORIGINATOR'S REPORT NUMBER(S) Memorandum 15	
b. PROJECT NO.		9b. OTHER REPORT NO(S) (Any other numbers that may be assigned this report)	
c.			
d.			
10. AVAILABILITY/LIMITATION NOTICES Qualified requesters may obtain copies of this report from DDC.			
11. SUPPLEMENTARY NOTES		12. SPONSORING MILITARY ACTIVITY Advanced Research Projects Agency	
13. ABSTRACT <p>This report discusses the design and use of equipment built for data communication to and from a PDP-8 through a 201A data set. The purpose of the data communication interface is to allow a PDP-8 to send and receive digital data through a 201A data set in half-duplex mode. Basic design objectives and decisions are described first. A brief overall system description together with a sketch of a data format scheme and programming considerations is followed by a detailed description of the interface logic.</p>			

14. KEY WORDS	LINK A		LINK B		LINK C	
	ROLE	WT	ROLE	WT	ROLE	WT
Data Communication Logical Design Data Transmission Serial Synchronous Data Transmission Digital Computer Interface						

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