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A 21.4 pW/frame-pixel PWM image sensor with sub-threshold leakage reduction and two-step readout

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Abstract: In this work we present a sub-1V pulse-width-modulation (PWM) CMOS image sensor. Ultra-low power consumption is achieved through the sub-threshold pixel bias, time-to-digital conversion and the array-level asynchronous counter. The 2-step readout scheme is adopted to improve the frame rate up to 68 fps. The prototype chip with 64 × 64 array has been fabricated in a 0.18 µm 1P6M CMOS process. Minimum functional analog supply of 0.36 V can be achieved, and the whole chip consumes only 1.14 µW at 13 fps, or 21.4 pW/frame-pixel. The dynamic range and FPN are measured to be 70 dB and 0.49% respectively.

Keywords: image sensor, low power, pulse-width-modulation (PWM)

Classification: Electron devices, circuits, and systems

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1 Introduction

Traditionally CMOS image sensors (CISs) are targeted to high-end applications where resolution and image quality is of great importance [1, 2]. Nowadays, the emerging applications of portable electronics, implantable biomedical imagers [3] and smart home devices [4] have generated an increasing demand for ultra-low power image sensors. This trend is also revealed from market data [5]. In a wireless capsule endoscopy system [6], a low-power image sensor is necessary in order for the tiny capsule to take images and send data out during the 6–8 hours' examination. The latest wireless house-security camera is able to work continuously for 6 months with only one pack of Lithium batteries, and therefore its image sensor has to be very power-efficient.

With techniques like on-chip supply-boosting [7], current mode APS [8] and logarithmic APS [10], the power consumption of image sensors have been effectively reduced. But in order to ensure enough signal swing, the supply voltage (Vdd) of these analog pixels cannot be scaled too much [9]. Recently, various approaches concerning the use of the pulse-width-modulation (PWM) technique have been investigated [11]. In PWM imaging, the incident light intensity is represented by the width of the pixel output pulse in digital level instead of analog voltages or currents. This has relieved the issue of voltage headroom when the pixel supply voltage is lowered to cut power.

Several prototype PWM imager chips have been proposed. Early pioneering works by Bermak et al. [12] demonstrated proper function of PWM imagers, but the supply voltages are still high and the pixel fill-factor are below 30% owing to

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the complicated pixel comparators. Kagawa et al. [13] then presented a low-voltage PWM imager with 1.4 V–1.8 V supply voltage. Cho et al. [14] used a TBR readout scheme and the supply voltage was further reduced to 0.75 V. Hanson et al. [15] adopted a 2-transistor in-pixel comparator and achieved 0.5 V supply voltage operation. Recently Chung et al. [16] proposed a 0.5 V, 147.3 pW/frame-pixel PWM imager, and their novel pixel structure was effective in cancelling the FPN (fixed-pattern-noise) and extending the dynamic range. Their work has remarkably improved the image quality of PWM imagers.

Although the PWM imagers have shown good low power capability, there is still room for improvement. Leakage is a great concern in the domain of low Vdd and sub-threshold pixel operation. Some of the PWM imagers employ a threshold (Vth)-referred-reset [14, 16] scheme to cancel the Vth variation, but leakage current from the reset transistor becomes a significant source of dark current [17]. The leakage current from inactive rows of pixels is also troublesome, since it will steal charge from the column data bus and may result in significantly narrowed pulse widths (PWs). These effects will degrade SNR and dynamic range (DR) [8]. Moreover, the counters used to translate the PWs into digital codes will limit the sensor frame rate. Pixel-level counter enables real-time readout of each pixel [14], but its fill factor is greatly sacrificed. The use of column-shared counters [15, 16] is not very effective in terms of power and area, and the sensor frame rate is affected because the operation of a certain row has to wait sometime before the end of the previous one, or the data being read out in the counters might be unexpectedly replaced by new data.

To overcome these problems, we propose a low-voltage PWM image sensor which only consumes μW-level power. The pixel employs Vth-referred-reset to cancel the FPN induced by the in-pixel comparator. The dual-reset transistors are adopted to lower the leakage current. The sensor uses a global counter with a 2-step latched-readout scheme, which improves the frame rate. Prototype-chip measurement results show that the sensor is functional to capture images with analog Vdd as low as 0.36 V, and the whole chip only consumes 1.14 μW at 13 fps.

2 Proposed image sensor circuit design

The top-level system architecture of the proposed image sensor is shown in Fig. 1(a). This is an ultra-low power PWM image sensor with 10-b digital output. In this section, the design of the ultra-low power PWM pixel, the optimization for low sub-threshold leakage and some other peripheral blocks of the sensor will be introduced, discussed and analyzed.

2.1 The PWM pixel operation

The proposed PWM pixel schematic is shown in the blue dashed box in Fig. 1(b). It is composed of 7 NMOS transistors and a P-sub/N-well photodiode as the light-sensing element. The associated column-shared circuit is also shown in the red dashed box above. In this sensor, instead of analog pixel output, the light intensity of each pixel in the j^{th} column is represented by the PW of the column data line, Vcol[j]. It is first charged to AVDD through M9, and then discharged to ground

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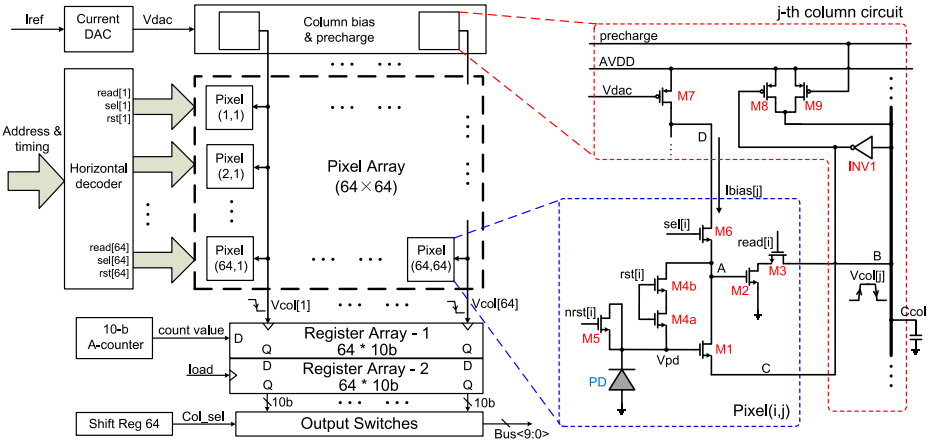
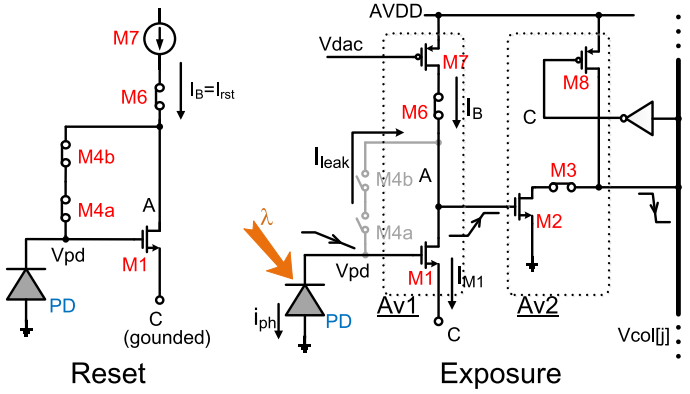
level, at a time relevant to the incident light intensity. To illustrate the PWM operation more clearly, Fig. 1(b) is redrawn in Fig. 2. The timing of the pixel operation is shown in Fig. 3.



(a) (b)

Fig. 1. Proposed PWM image sensor. (a) Whole chip architecture. (b) Pixel and column bias schematics.



(a) (b)

Fig. 2. Simplified PWM pixel. (a) reset (b) exposure

The pixel experiences a reset phase (Fig. 2(a)) and an exposure phase (Fig. 2(b)) during operation. When the reset phase starts, M1 becomes diode-connected, so the voltage at node A (V_A), as well as the photodiode voltage (V_{pd}) are set by the threshold voltage of M1 (V_{th1}) and the reset bias current I_{rst}. The I_{rst} is designed at 10~100 nA level to limit the pixel power consumption. As a result, M1 has to operate in sub-threshold region, giving the expression for V_A and V_{pd} [18]:

$$V_{A,reset} = V_{pd,reset} = V_{th1} + \eta V_T \ln\left(\frac{I_{rst}}{I_t \cdot (W/L)_{M1}}\right) \quad (1)$$

Where η is a device parameter, V_T is the thermal voltage and $(W/L)_{M1}$ is the aspect ratio of M1.

During the exposure phase that follows, the pixel bias current I_{M7} sharply drops to its minimum value, and V_A is therefore discharged to ground level. The read

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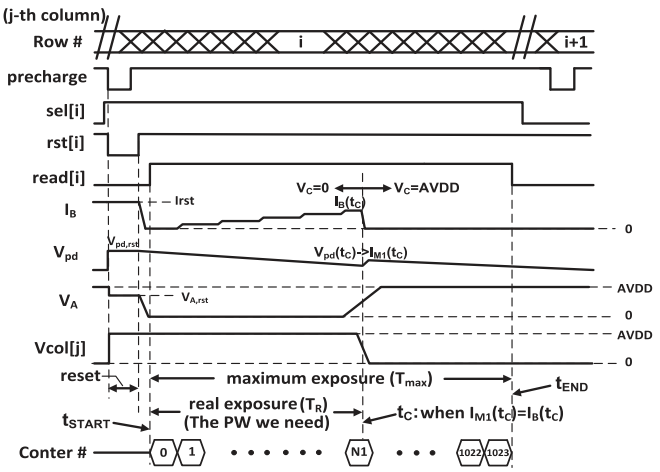

Fig. 3. Timing diagram of the pixel operation.

enable switch M3 will stay cutoff until V_A is totally discharged, so M2 will not be falsely opened by the reset level of V_A.

With the decrease of V_{pd} and the increase of I_B, there will be a moment, t_C, when V_A gradually rises to AVDD, because V_A is the output of the 2-transistor comparator [15] formed by M1 and M7. However, since the slew rate at node A is limited by the sub-threshold pixel bias current, the rising edge of V_A is not so steep as to be carefully measured later on by the counter. So we need another gain stage (M2 and M8) to create a steeper (falling) transition edge on Vcol[j]. Now starting from the beginning of the exposure phase (t_{START}), the PW of this pixel has been generated on Vcol[j].

In the pixel operation described above, the output PW (T_R), or the transition moment (t_C), depends on how fast V_{pd} decreases. Now this t_C, indicative of the incident light intensity, is recorded by the global counter in Fig. 1(a) with a 10-bit digital value N1, and is then latched into the register array-1.

The node "C" is initially grounded in Fig. 2(b). But it rises up to AVDD as soon as the transition moment t_C arrives and Vcol[j] falls to "0". Then no current flows through M1 and M7, and the pixel power consumption is effectively cut. The stronger the light, the sooner t_C arrives, and the more power that is saved.

2.2 FPN cancelling

The FPN issue of PWM pixels is very annoying since the threshold voltage of the comparator in each pixel has a statistical variation, due to the non-uniformities in CMOS process. This has great impact on the FPN of such sensors [15]. The latest solution is to reset the pixel with respect to the comparator threshold voltage [13, 14, 16], so that the "V_{th}" term is ingeniously cancelled out and the pixel-level FPN is significantly reduced.

In this work, the reset level of V_{pd} has been derived in Eq. (1). When the exposure phase finishes (Vcol[j] falls at t_0 moment), according to the sub-threshold I-V theory of MOSFET [18], the V_{pd} is expressed by:

$$V_{pd}(t_C) = V_{th1} + \eta V_T \ln\left(\frac{I_B(t_C)}{I_t \cdot (W/L)_{M1}}\right) \quad (2)$$

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The PW of this pixel (T_R in Fig. 3) is then given by the charge difference ΔQ on the V_{pd} node during this exposure period, divided by the photo-current, i_{ph}:

$$T_R = \frac{\Delta Q}{i_{ph}} = \frac{C_{pd}(V_{pd,rst} - V_{pd}(t_C))}{i_{ph}} = \frac{C_{pd}\eta V_T}{i_{ph}} \ln\left(\frac{I_{rst}}{I_B(t_C)}\right) \quad (3)$$

Where C_{pd} is the photodiode capacitance. The result of Eq. (3) suggests that the Vth-induced FPN can be totally cancelled in the pixel level [16].

2.3 Sub-threshold leakage reduction

The leakage current from V_{pd} node is a serious problem for both conventional and PWM pixels. In our case, we hope that V_{pd} is discharged only by the photo-current, i_{ph}, as shown in Fig. 2(b). But we notice that there is a leakage path from V_{pd} to node A, and then through M1 to ground, because $V_{pd} > V_A$ during exposure. To make matters worse, when V_A falls from AVDD to 0 at the beginning of exposure, there is a capacitive coupling through the C_{gd} of M1, and V_{pd} node will lose more charge. As a result, V_{pd} will decrease much faster than expected, and the obtained PW will be much narrower.

The simplest way to reset the pixel is to use a single transistor M4, as shown in Fig. 4(a). Since M4 cannot be completely cut off even when rst = 0, the sub-threshold leakage current I_{leak1} should not be neglected, especially when i_{ph} is comparable with I_{leak1} (at pA level).

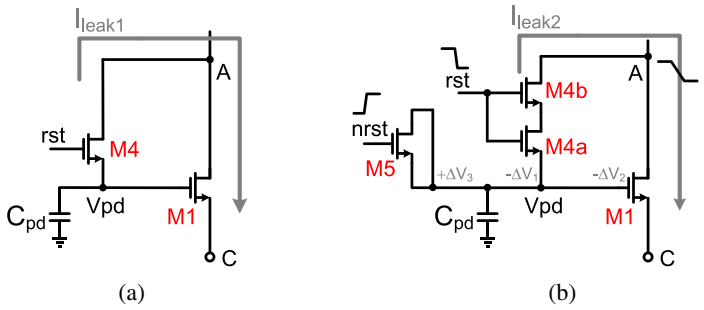

Fig. 4. The reset transistor(s). (a) Single transistor. (b) The proposed 2 serial reset transistors and M5.

In this work we used two transistors in serial as the reset transistors, as shown in Fig. 4(b). When M4a and M4b are stacked, their off-resistance is increased and therefore the leakage current is reduced. In real design, a more careful sizing strategy of M4a and M4b is taken to optimize the overall pixel performance. The length of M4b is designed relatively larger to limit leakage current, while a minimum size M4a is used, both to improve the pixel fill-factor and to minimize the capacitive coupling effect on V_{pd} node.

For the 2 cases in Fig. 4(a) and (b), the V_{pd} and V_{col} waves are compared and shown in Fig. 5. From this simulation result we find that the leakage of the single reset transistor is significantly higher. The simulation result is $I_{leak1} = 2.4\,\text{pA}$ against $I_{leak2} = 0.7\,\text{pA}$. In the case of a 10-bit counter and dark environment ($i_{ph} = 0$), the error on pixel value reaches 132 or 13%.

The M5 in Fig. 4(b) is intended to compensate for the negative voltage ripple on V_{pd} node. They are induced by the switching action of V_{rst} and V_A, and are

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denoted by $-\Delta V1$ and $-\Delta V2$ respectively. When nrst, the reverse signal of rst, is applied to M5, the positive ripple $+\Delta V3$ will cancel out the sum of $-\Delta V1$ and $-\Delta V2$ if the area of M5 is carefully designed. All these efforts are devoted to keep our V_{pd} node "unaffected". This requires:

$$\frac{C_{gd,M4a}}{C_{pd}+C_{gd,M4a}}\cdot DVDD+\frac{C_{gd,M1}}{C_{pd}+C_{gd,M1}}\cdot AVDD=\frac{2C_{gd,M5}}{C_{pd}+2C_{gd,M5}}\cdot DVDD \quad (4)$$

When C_{pd} is large and AVDD = DVDD, the following device size relation can be derived from Eq. (4):

$$(WL)_{M5}=\frac{1}{2}[(WL)_{M1}+(WL)_{M4a}] \quad (5)$$

In real design, the $(WL)_{M5}$ is tuned to make V_{pd} return to its reset value at the beginning of exposure, and this $(WL)_{M5}$ turns out to be very close to the calculation result obtained in Eq. (5).

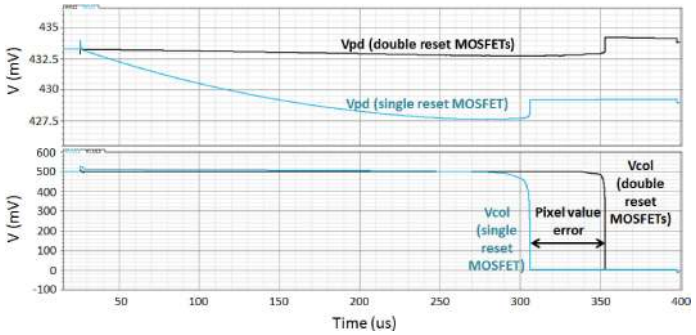

Fig. 5. V_{pd} and V_{col} transient simulation. The double MOSFET reset has smaller sub-threshold leakage on V_{pd} and saves more pixel PW on V_{col}.

There is another leakage source in Fig. 1(b) which takes place on the column data line (Vcol[j]). Apart from the active pixel, all the other inactive pixels in the same column also contribute leakage currents to Vcol[j]. The effect of the cumulative leakage on Vcol[j] cannot be ignored, especially when the array size increases [15]. As a result, Vcol[j] will be discharged faster, and the output PW of the active pixel will be narrower than expected. To relieve this column leakage, M8 is added as a feedback compensator. As long as Vcol[j] is high, M8 keeps "on" and will compensate for the charge loss on Vcol[j] due to the column leakage, until M2 of the active pixel really discharges it. The W/L of M2 has to be much larger than M8 to ensure proper discharging operation on Vcol[j].

2.4 High speed, low power data readout

The timing diagram of data readout is illustrated in Fig. 6, and the readout sub-circuit is redrawn in Fig. 7 with more details. All pixels are exposed and read out in a column parallel, rolling-shutter manner. Let's take the j^{th} column and the i^{th} row for example. As shown in Fig. 7(a), the falling edge on Vcol[j] triggers the DFFs in register array-1, storing the corresponding counter value N(i) on Q1[j]. This value is then loaded into another register array Q2[j], and is then ready to be serially read out through a switch array controlled by a global shift register.

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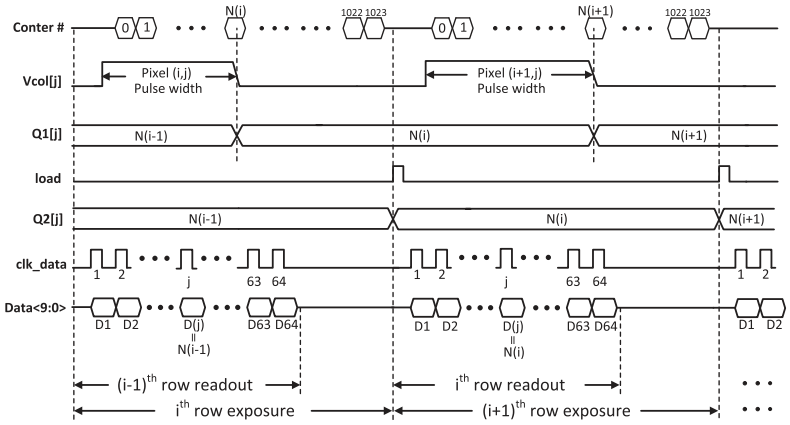

Fig. 6. Timing diagram of the data readout. The exposures of two consecutive rows are seamless and overlap with the readout, which improve the frame rate.

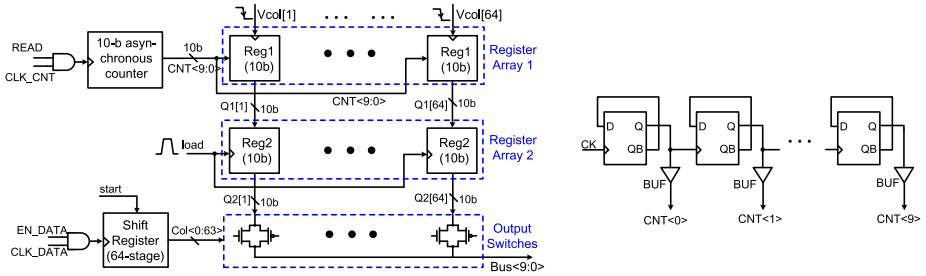

Fig. 7. The readout sub-circuits. (a) Schematic block diagram. (b) 10-b asynchronous counter.

Instead of column-level counters [14, 15] which are both area costing and power consuming, we adopt a 10-bit global counter to count the PW of each column. As shown in Fig. 7(b), the counter is asynchronous which is even more power efficient [19] than synchronous ones.

The two register arrays in Fig. 7(a) serve different purposes. Register array-1 uses the falling edge on Vcol[j] to record the counter values, whereas register array-2 is designed to improve the frame rate. One can see from Fig. 6 that register array-1 is released after loading its values to Q2[j], ready for instant exposure of the next row. As a result, the readout period of the previous row is completely enclosed in the exposure period of the current row. Although the readout speed is still subject to the rolling-shutter operation mode, this 2-stage readout scheme has been very efficient for the proposed sensor architecture with a row number of 64.

3 Fabrication and experimental results

3.1 Prototype chip fabrication

The prototype image sensor with a 64×64 array has been fabricated in a 0.18 µm 1P6M CMOS logic technology. All NMOS and PMOS transistors are thin gate, normal threshold devices. The chip microphotograph is shown in the left part of Fig. 8. The whole chip area is 1.7 mm × 2.2 mm.

The pixel PD is fabricated with a P-sub/N+ structure which is more area-efficient than a P-sub/N-well PD. The in-pixel transistors are all NMOSFETs to

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save area. The pixel size is 18 µm*18 µm with a 54% fill factor, as shown in the right part of Fig. 8. The pixel size is relatively larger than conventional CISs to ensure to proper photo-electronic function of the photodiode and to improve the sensitivity. But larger C_{pd} has lowered the conversion gain which has negative effect on noise electrons. The pixel layout is yet to be optimized to achieve smaller pixel pitch and higher fill factor.

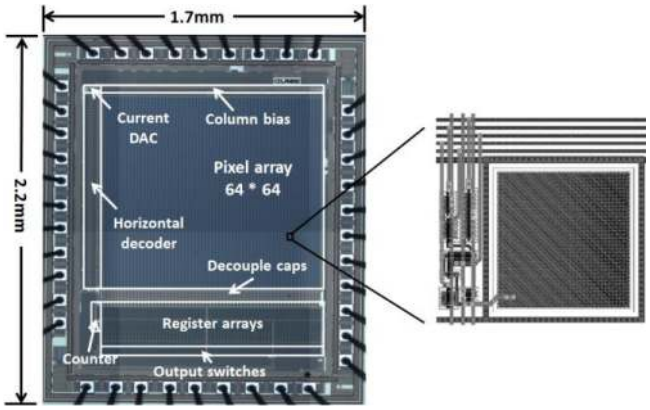

Fig. 8. Chip microphotograph (left) and the pixel layout (right).

3.2 Experimental results

A test platform is established to carry out the measurements and capture images. This platform includes a PCB carrying the proposed chip, an FPGA board for data control/storage/USB transmission, and a PC software for data acquisition and image reconstruction.

The image sensor chip is functional with analog power supply (AVDD) ranging from 0.36 V to 1.3 V. The digital power supply (DVDD) will have to be about 200 mV higher than AVDD to ensure proper switching operation of the pixel selection (M6 in Fig. 1(b)). The maximum frame rate can reach 68 fps, thanks to the efficient 2-stage readout in Fig. 6. However, with the growth of array size, the frame rate will ultimately be limited by the rolling-shutter exposure mode.

The power consumption is measured under a typical 0.6 V AVDD and 50 lux uniform illumination. Fig. 9 shows the power consumption against different frame rates. The iFoM, defined as the overall power consumed by each single pixel per frame, is plotted as well. The whole chip power consumption ranges from 0.50 µW (30.3 pW/frame-pixel) at 4 fps to 5.08 µW (18.1 pW/frame-pixel) at 68 fps. The iFoM decreases with the increase of frame rate, because the digital power (mostly dynamic power) will take up a larger percentage at higher frame rates.

The FPN of an image sensor refers to the standard deviation from the mean pixel value, often divided by the saturated pixel value, under uniform illumination. In order to derive the FPN under uniform illumination (PRNU), the test system is tuned so that the average pixel grayscale value is around half the maximum value. The whole image grayscale matrix is captured under AVDD = 0.6 V and a frame rate of 13 fps. The deviation from the mean pixel value is plotted in Fig. 10(a), followed by a statistical histogram in Fig. 10(b).

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It is noticeable from Fig. 10(a) that values at the center part of the captured frame are mostly flat, whereas pixels on the edge have somewhat smaller grayscale values. This means they are darker than other pixels, which is probably due to the edge effect of the pixel array and may be relieved through the use of a dummy pixel ring [20].

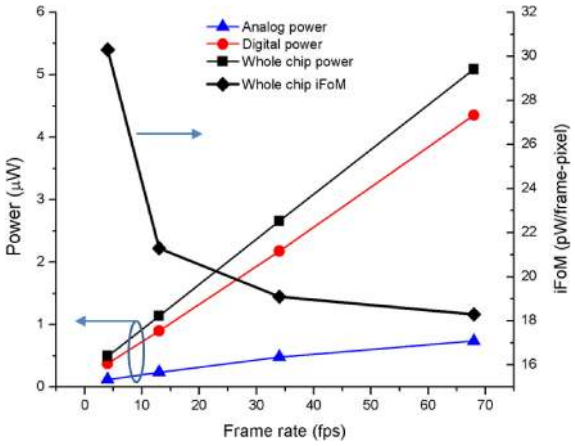
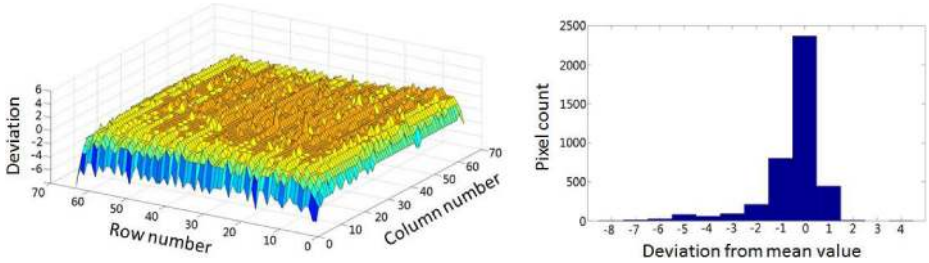


Fig. 9. Power consumptions and iFoM under different frame rates.



(a) (b)

Fig. 10. FPN measurement. (a) Deviation from mean pixel value (whole frame) under uniform illumination. (b) Histogram of the pixel grayscale value.

Statistical results in Fig. 10(b) show that nearly 90% pixels are within ±1 grayscale (out of 256 saturation grayscale) from the mean pixel value, which shows good uniformity. The calculated standard deviation of pixel value is 1.25 grayscale, corresponding to 0.49% raw FPN without off-chip digital CDS.

The dynamic range is measured by determining the maximum and the minimum distinguishable illumination levels. The proposed image sensor chip is able to detect light from 3.8 lux to 12 Klux, corresponding to a dynamic range of 70 dB.

A set of sample images are captured under the typical settings (AVDD = 0.6 V, 13 fps), as shown in Fig. 11. The pixel exposure time is set as 370 us to get bright enough pictures. Fig. 11(a), (b) are images on a paper, and Fig. 11(c), (d) are objects in real life. Some horizontal stripes can be observed, which is probably due to the light source used that is a flat panel driven by AC power.

A comparison of the major performances with other state-of-the-art works is listed in Table I. The proposed image sensor is able to work under very low power supply and relatively high frame rate, with acceptable FPN and dynamic range

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performances. The overall power iFoM is the best among the listed works, thanks to the sub-threshold pixel operation and the array-level asynchronous counter.

(a) (b) (c) (d)

Fig. 11. Captured sample images under AVDD = 0.6 V and 13 fps. (a), (b) Captured images on a white paper. (c), (d) Captured images of real life objects.

Table I. Low power image sensor performances compared with other works

	[13]	[15]	[16]	This work
CMOS Technology	0.35 µm 2P3M CMOS	0.13 µm bulk	0.18 µm 1P6M CMOS	0.18 µm 1P6M CMOS
Pixel pitch	10 µm	5 µm	10 µm	18 µm
Array size	128 × 96	128 × 128	64 × 40	64 × 64
Fill factor	18.5%	32%	25.4%	54%
Power supply	1.4 V–1.8 V	0.45 V–0.7 V	0.5 V	0.36 V–1.3 V*
Frame rate	5.5 fps	0.5 fps/8.5 fps	11.8 fps-78.5 fps	4 fps-68 fps
Dynamic range	48.8 dB	N/A	82 dB	70 dB
FPN	0.7%	4.8%	0.055%	0.49%
iFoM (pW/frame-pix)	108 @1.4 V	8.6 @8.5 fps 85.4 @0.5 fps	147.3 @78.5 fps 163.9 @11.8 fps	30.5 @4 fps, 0.6 V 18.3 @68 fps, 0.6 V

*Refers to analog power supply.

4 Conclusion

In this work we present an ultra-low power CMOS image sensor with 64 × 64 array size in 0.18 µm CMOS process. The prototype chip measurement results show proper imaging operation at 0.36 V power supply with 0.49% raw FPN and 70 dB dynamic range. The power iFoM has been significantly reduced to 21.4 pW/frame-pixel owing to the sub-threshold pixel operation and global asynchronous counter, which is promising to be applied in low power imagers like biomedical electronics and portable devices. Further works is required to optimize the pixel layout and to improve the frame rate which is limited by the array size, so as to maintain low power consumption in high resolution applications.

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