A 210mW Graphics LSI implementing Full 3D Pipeline with 264Mtexels/s Texturing for Mobile Multimedia Applications

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Outline

- Introduction
- System Integration Overview
- Low Power IP Blocks
  - RISC, BEQ, 3DRE, DRAM, PPO
- Low Cost Process Technology
- Implementation Results
- Summary

Multimedia Processing on Hand

PDA/Cellphone

Multimedia Applications
- Realtime Audio
- Realtime Video
- Realtime 3D Graphics

System Requirements
- Long Battery Lifetime
- Small Footprint
- Low Cost

- **2D/3D Graphics LSI for Mobile Multimedia**
  - Highest Level of Integration for Portable 3D
  - Low Power Techniques
  - Low Cost DRAM Process

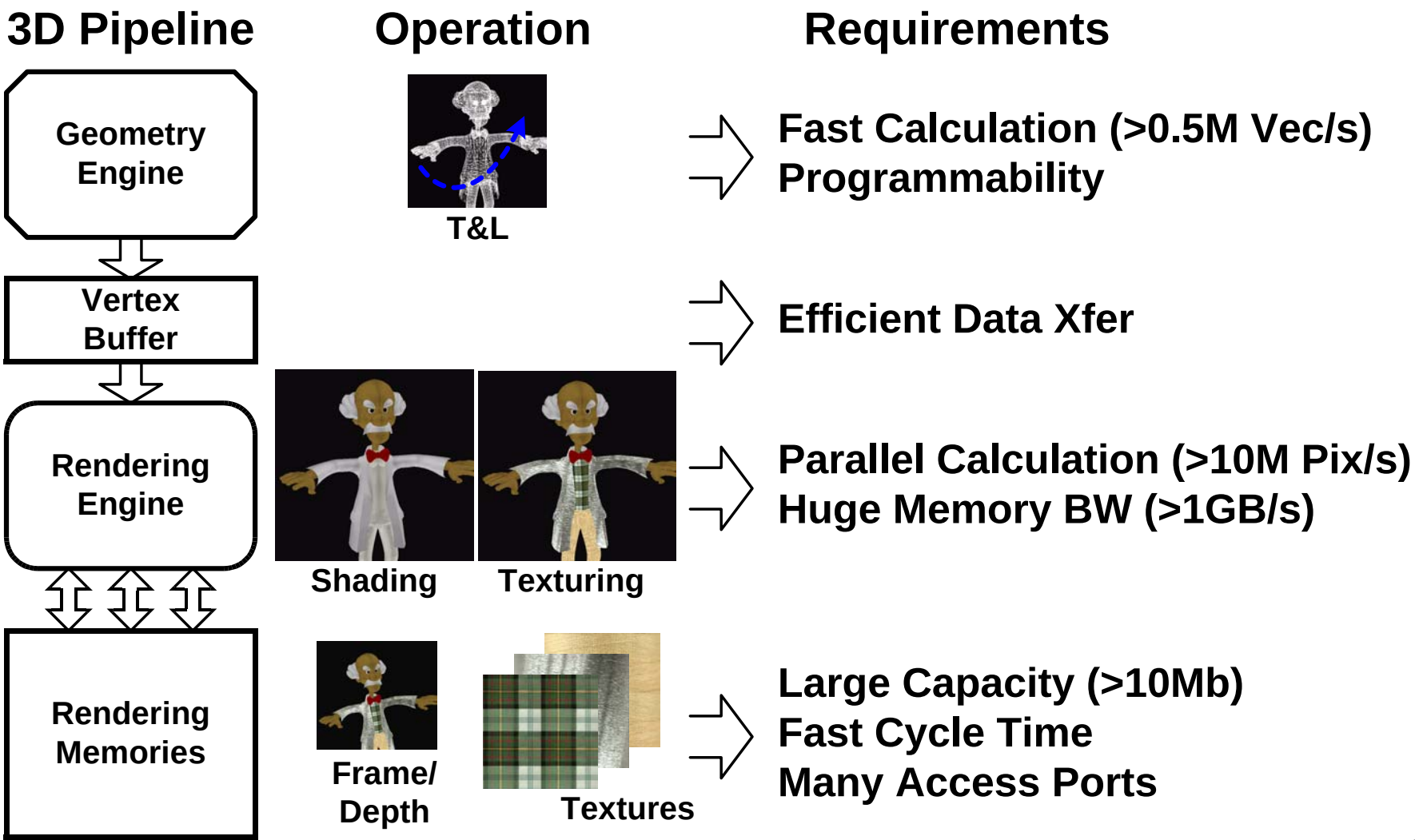
Portable 3D Graphics

- **Wireless Applications on Hands**
  - **3D Avatar, 3D Games, Advertisements**
- **Functional Requirements**
  - **Texture Mapping + Special Rendering Effects**
  - **Gouraud Shading, Alpha Blending, Depth Comparison**

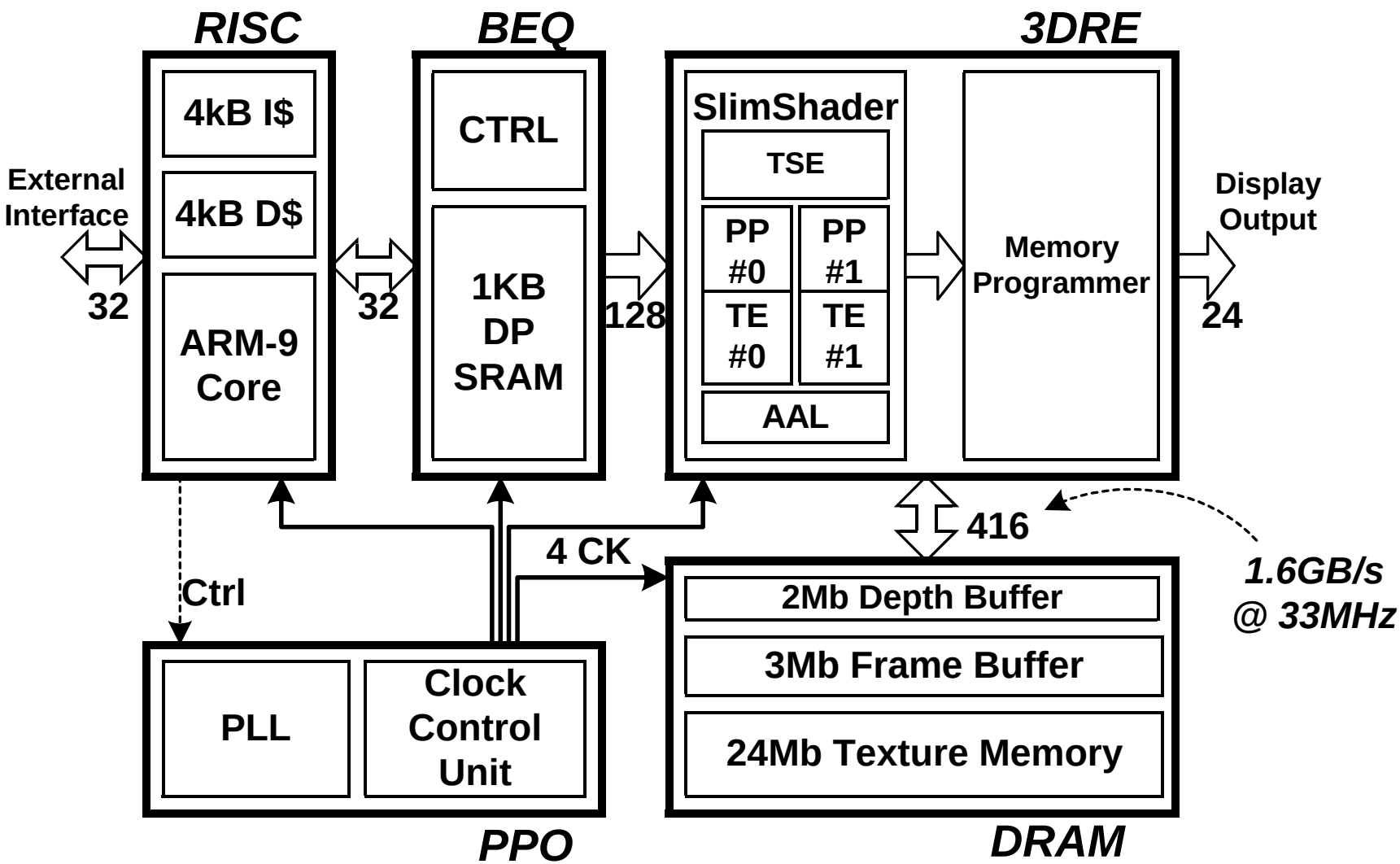
Standouts of 3D Rendering Engine

	ISSCC2000	ISSCC2001	**This Work**
Generation	1st		**2nd**
Process Technology	0.35μm EML	0.18μm EML	**0.16μm DRAM**
Power Consumption of 3D Rendering Engine	590mW	120mW	**140mW (Texture)** **80mW (No Texture)**
Pixel Fill Rate	40Mpixels/s	70Mpixels/s	**66Mpixels/s**
Texturing Performance	X	X	**264Mtexels/s** **Bilinear MIPMAP** **Perspective Correct**
Special Rendering Effects	X	X	**Programmable**
Size of Embedded DRAM	0.5Mbits (FB / ZB)	6Mbits (FB / ZB)	**29Mbits** **(FB / ZB / TM)**

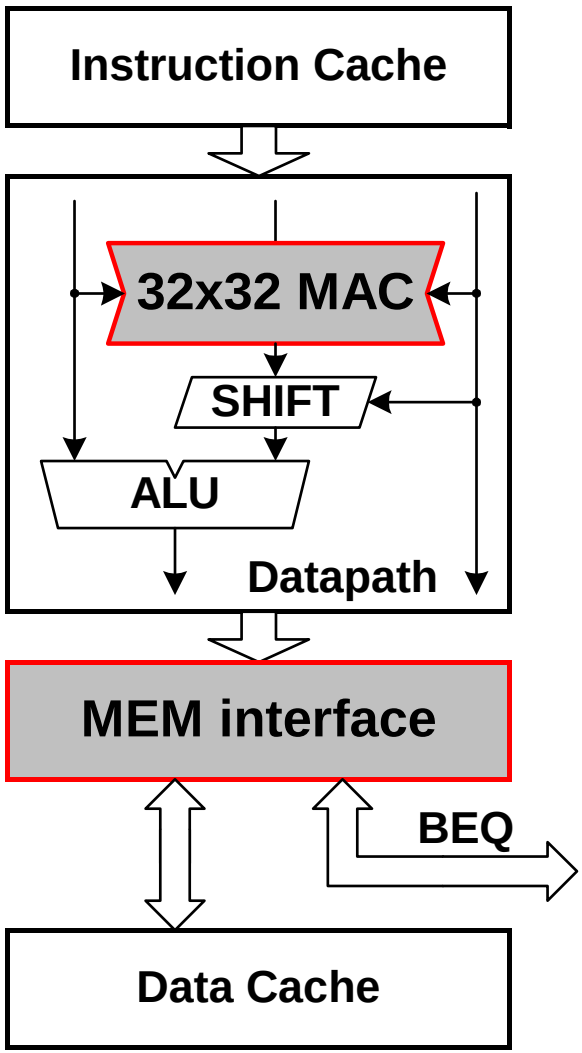
Integration of Full 3D Pipeline



Architecture Overview



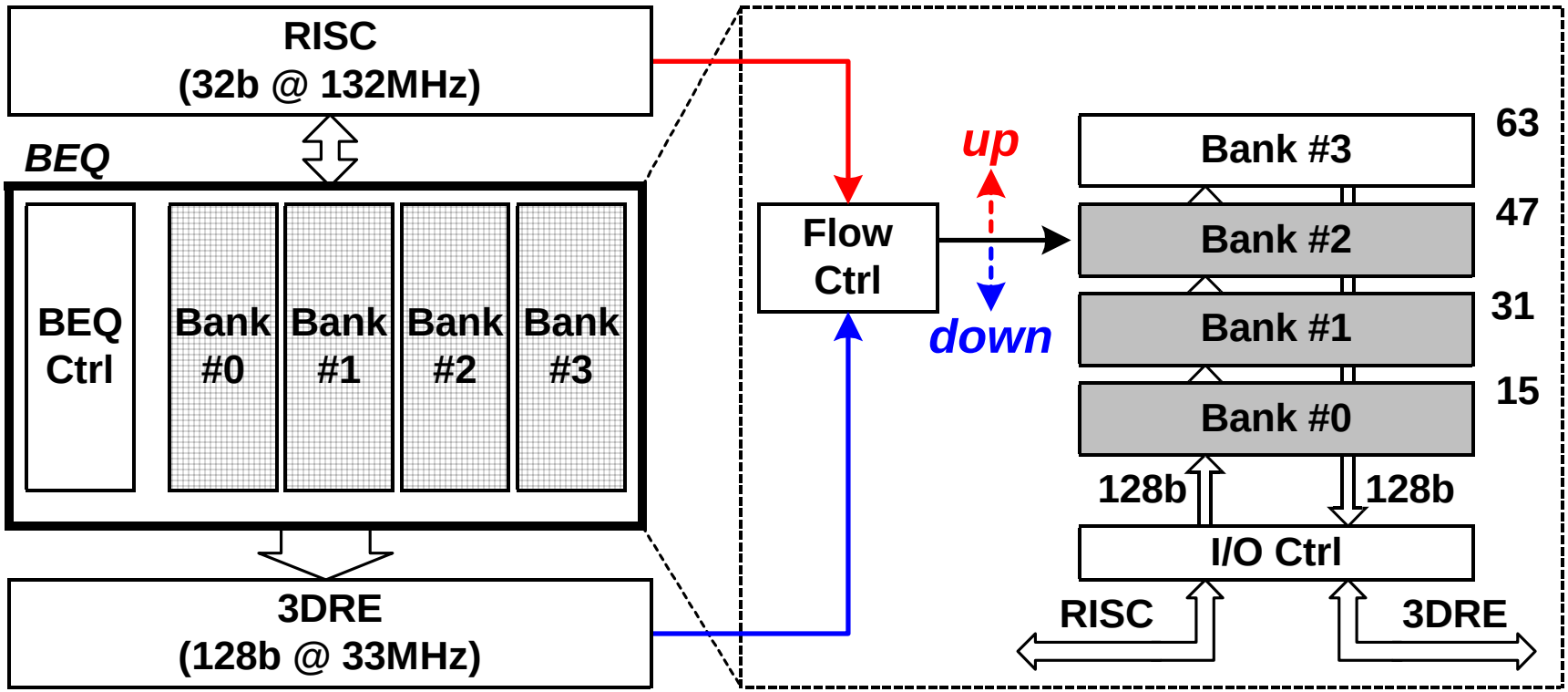
Multimedia-Enhanced RISC



- **Enhancement with MAC**
  - 32x32 MAC in a single cycle
  - 3D Geometry Acceleration
    - 1.04Mvertices/s
    - 43% Improvement
  - Hand-Optimized S/W Library
  - MPEG-4 SP@L1 Decode
- **Memory Interface**
  - Direct path to BEQ
  - On-Chip SP-RAM Support
  - Non-Cacheable Addressing

Bandwidth Equalizer

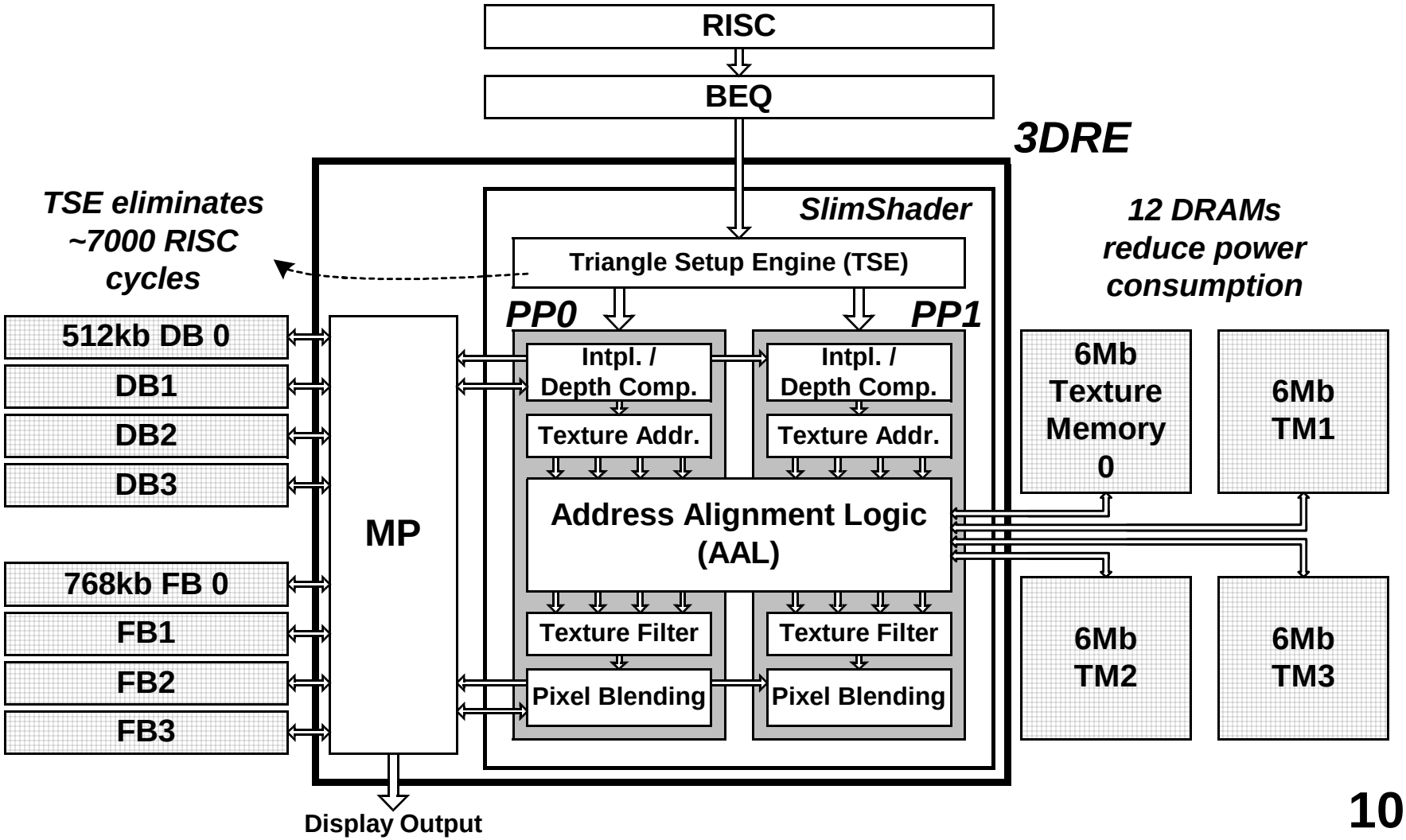
: Low Power Technique (1)



- Partial Activation of DP-SRAM 20% Power Save
- Polygon Buffer / SP-RAM

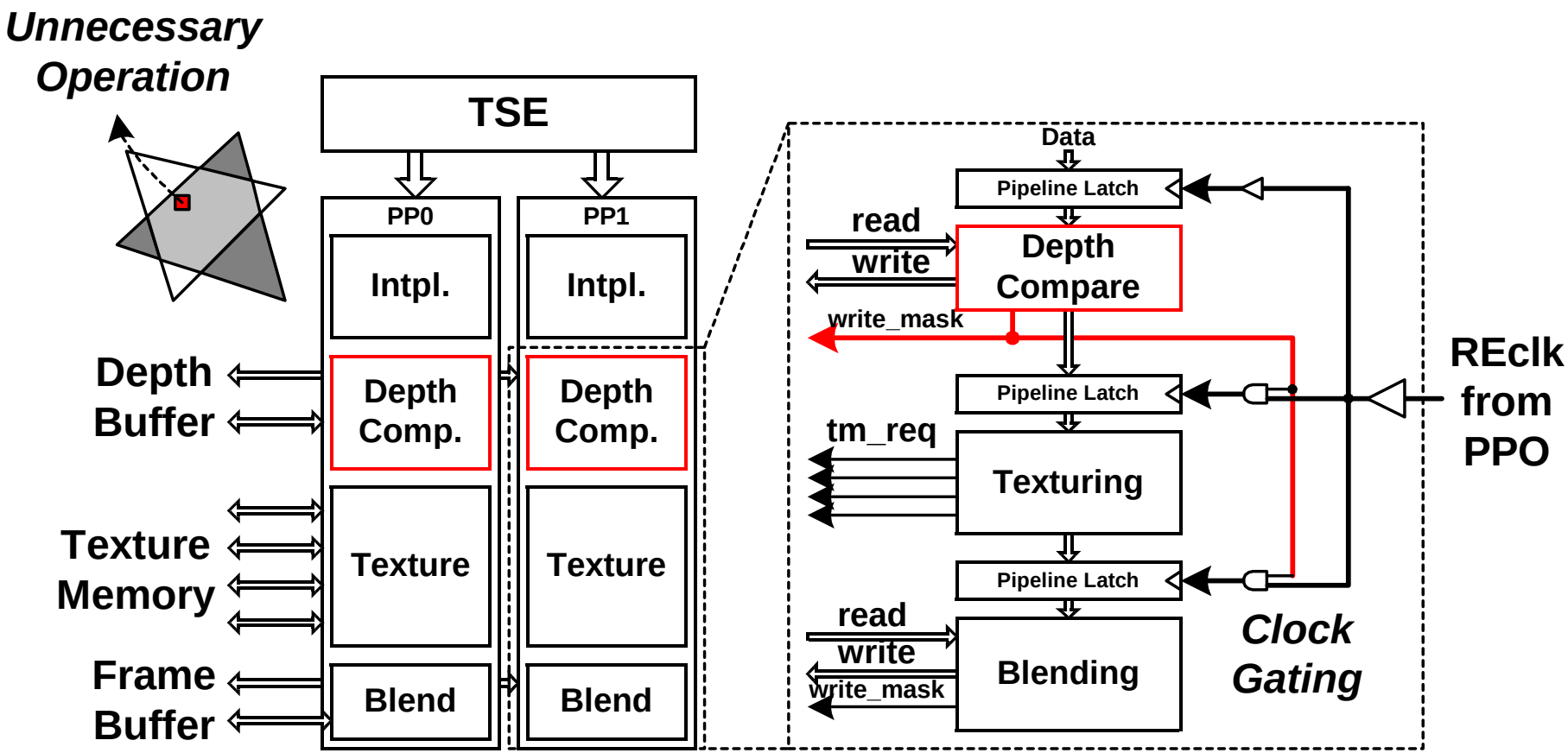
3D Rendering Engine Architecture

: Low Power Technique (2)



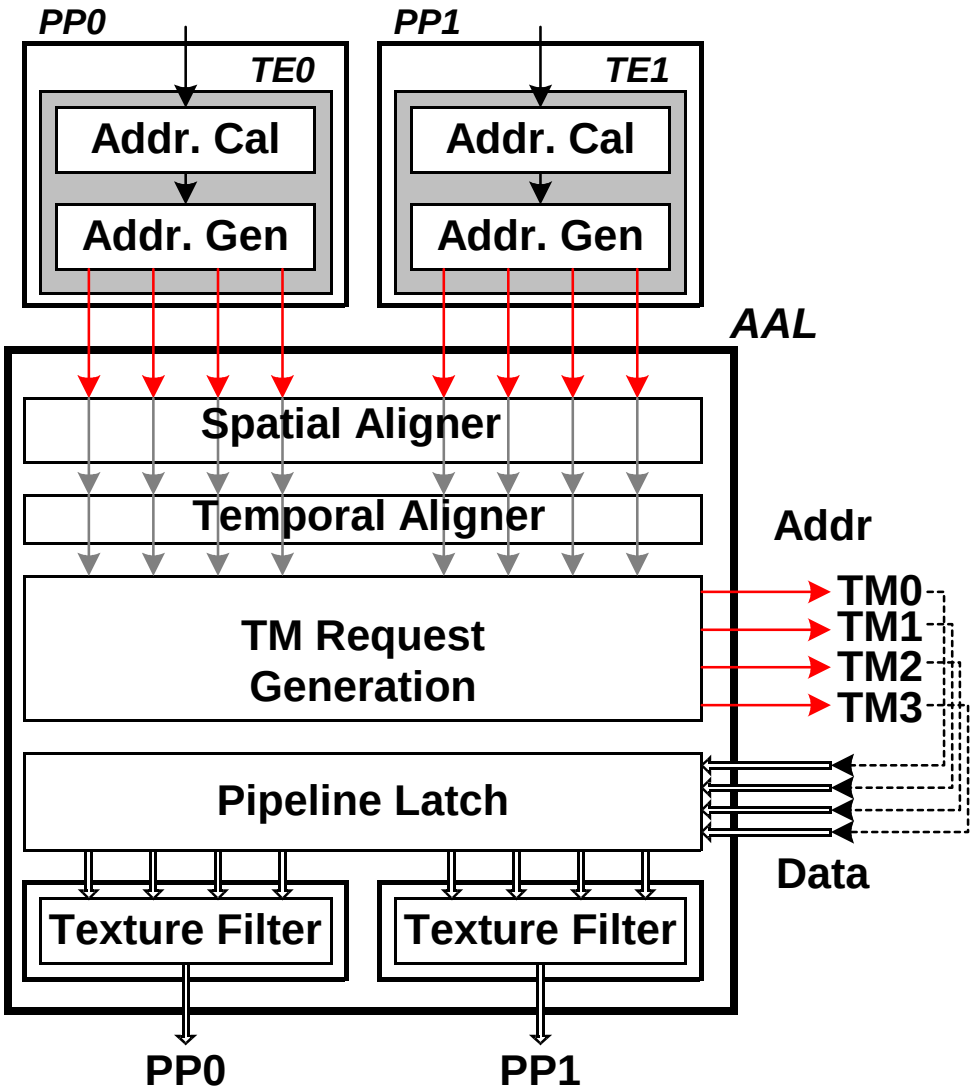
Depth First Clock Gating

: Low Power Technique (3)



- DFCG prevents Unnecessary Transition

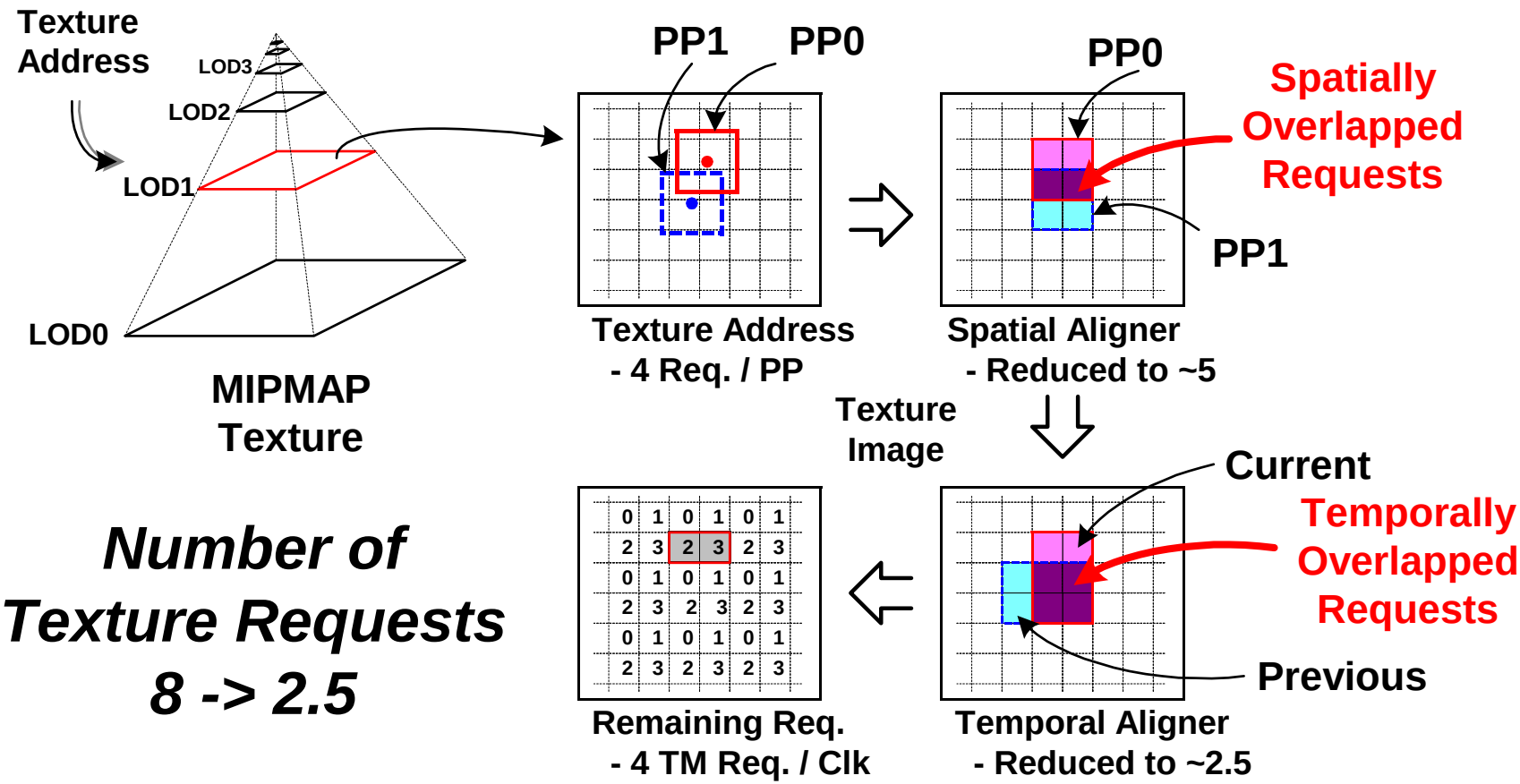
High Performance & Low Power Texturing
: Low Power Technique (4)



- **Address Calculation**
  - Perspective-Correct
  - Per-Pixel Dividers
  - Removes Artifacts
- **Texture Filtering**
  - Bilinear MIPMAP
  - Improves Pixel Quality
- **AAL**
  - Reduces the TM Requests
  - Simple Texture Cache
- **Embedded TMs**
  - Eliminates Off-chip loading

Address Alignment Logic

: Low Power Technique (5)

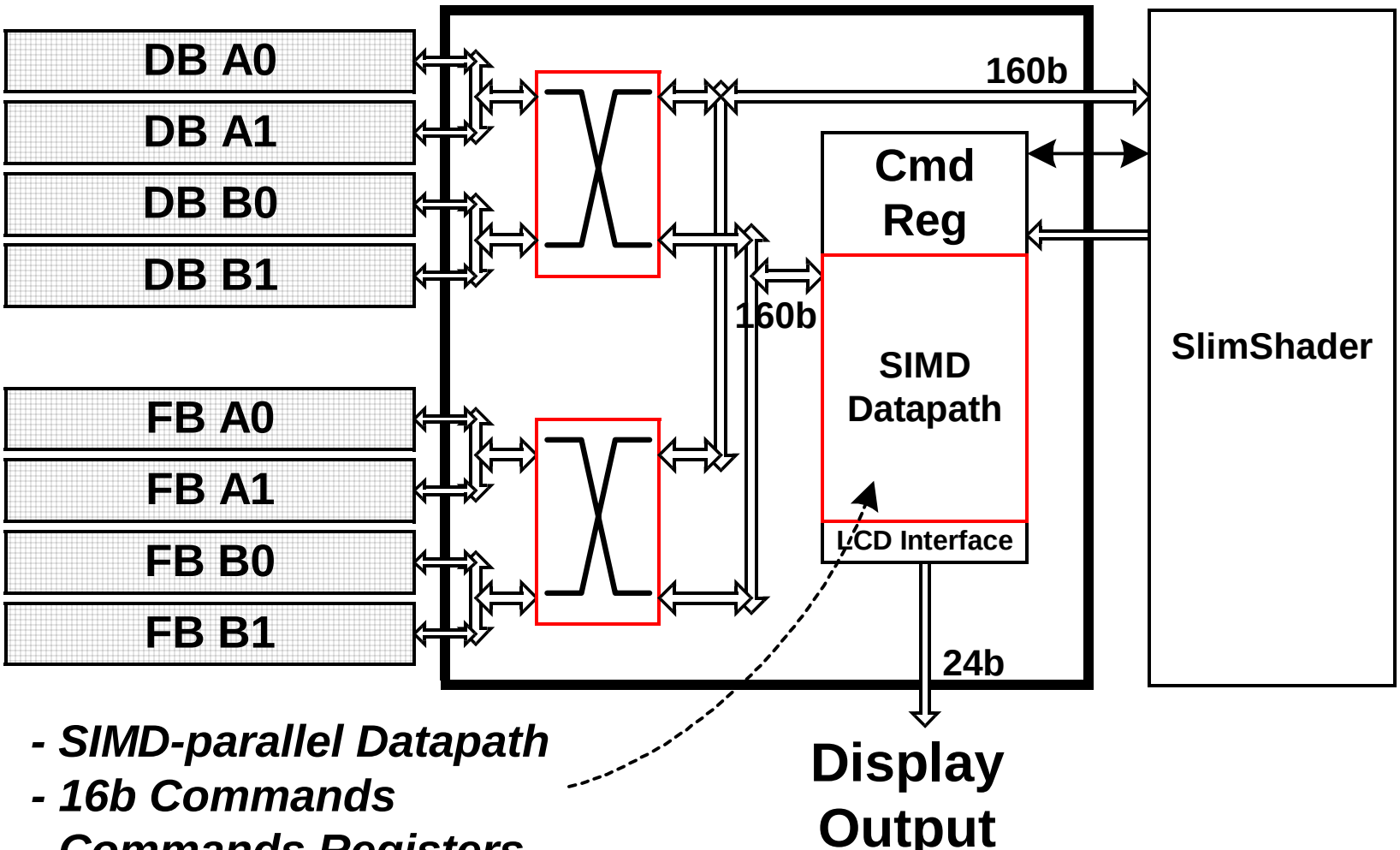


Number of Texture Requests 8 -> 2.5

- **DFCG and AAL reduce 20% Power**

Memory Programmer

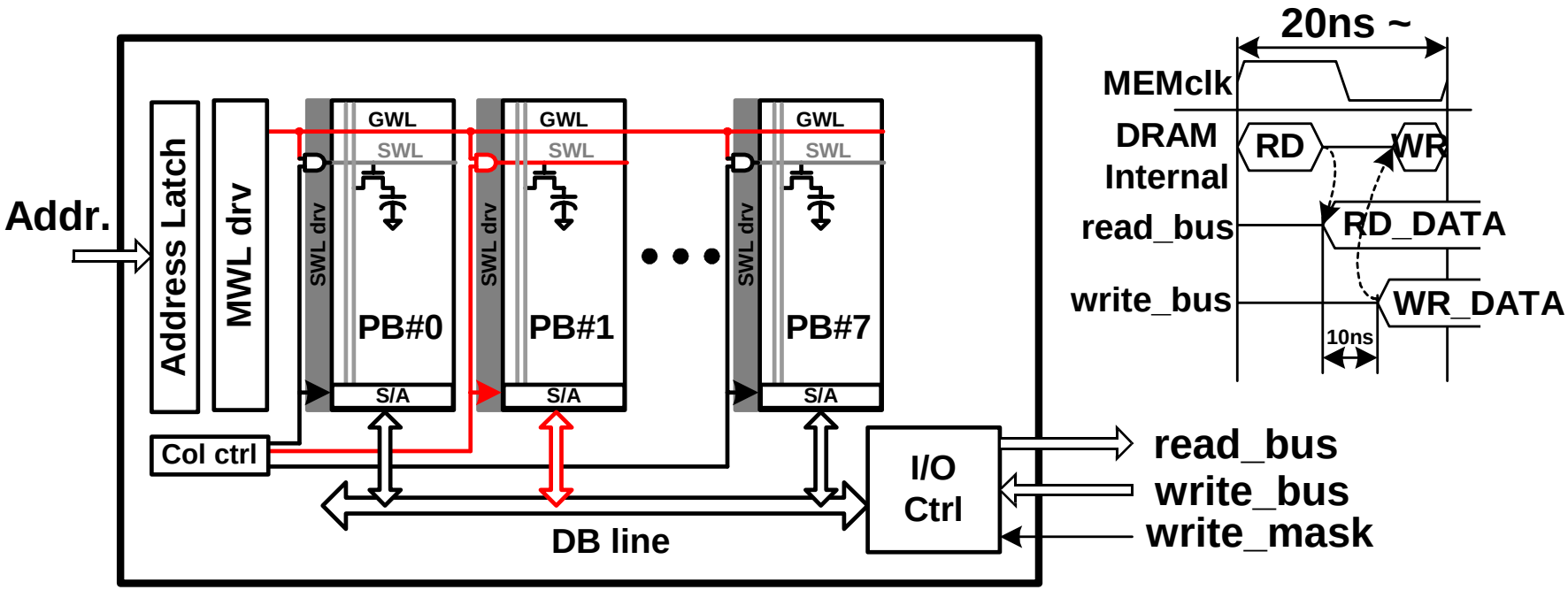
: Low Power Technique (5) – Cont'd



- *SIMD-parallel Datapath*
- *16b Commands*
- *Commands Registers*

3D-Optimized DRAM : FB / ZB

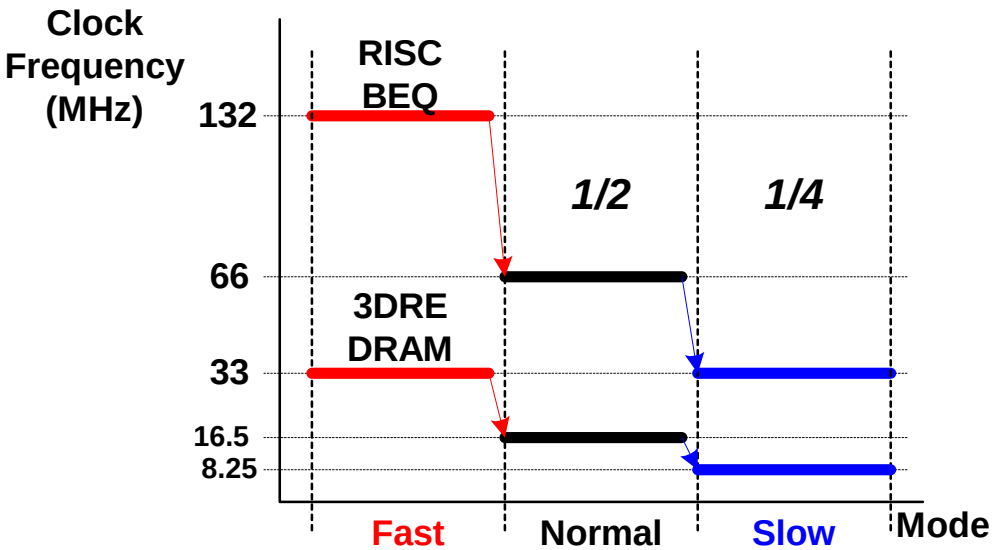
: Low Power Technique (6)



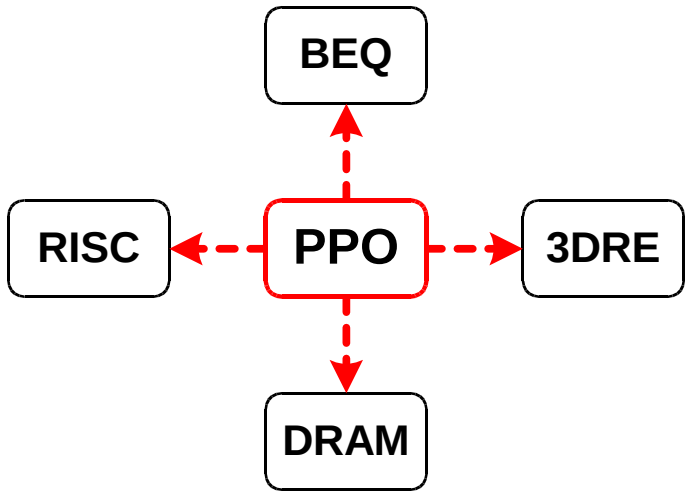
- Read-Modify-Write in a single Cycle < 20ns
- Partial Wordline Activation

Programmable Power Optimizer

: Low Power Technique (7)



Frequency Scaling

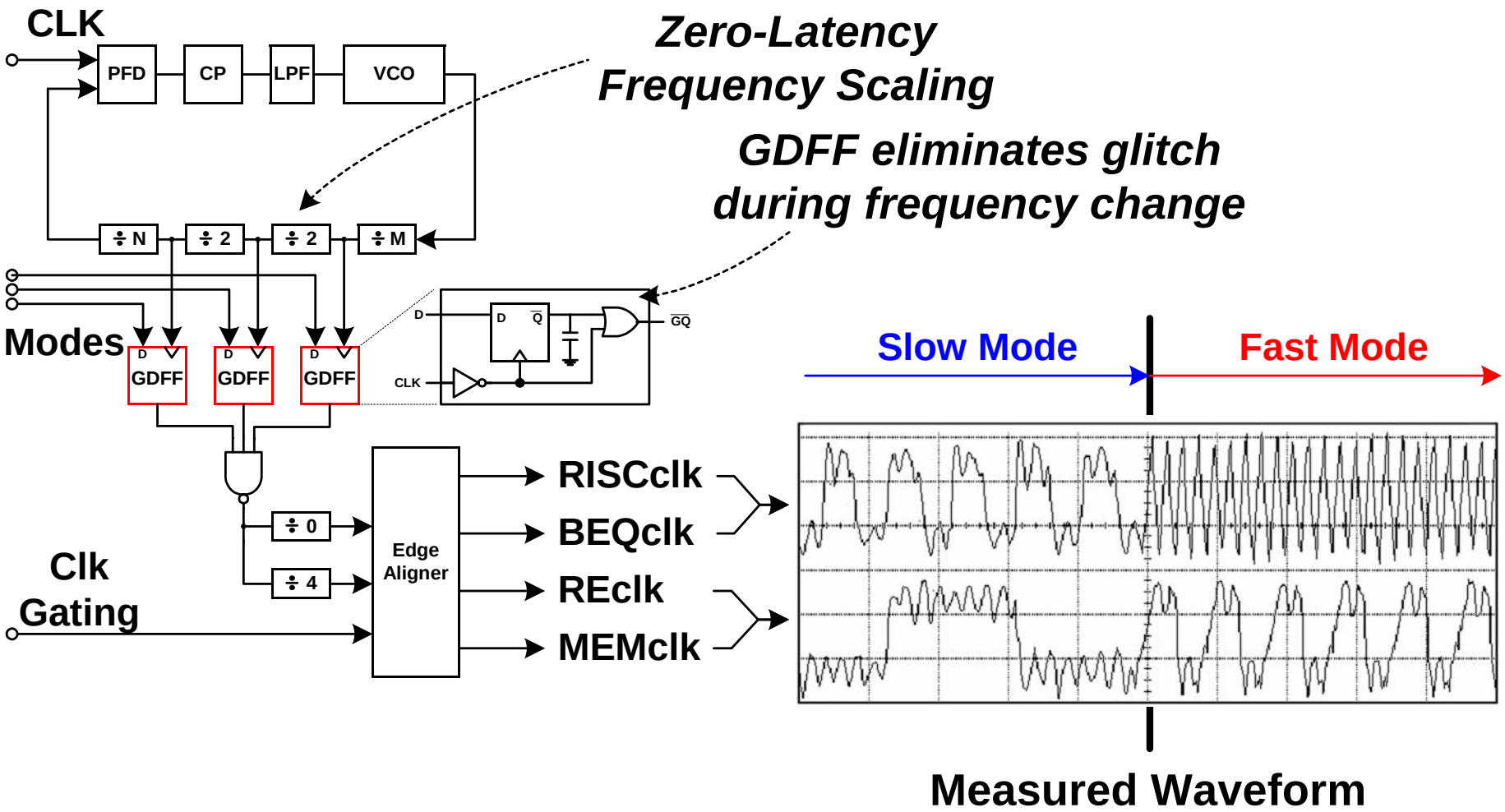


Coarse-Grained CLK Gating

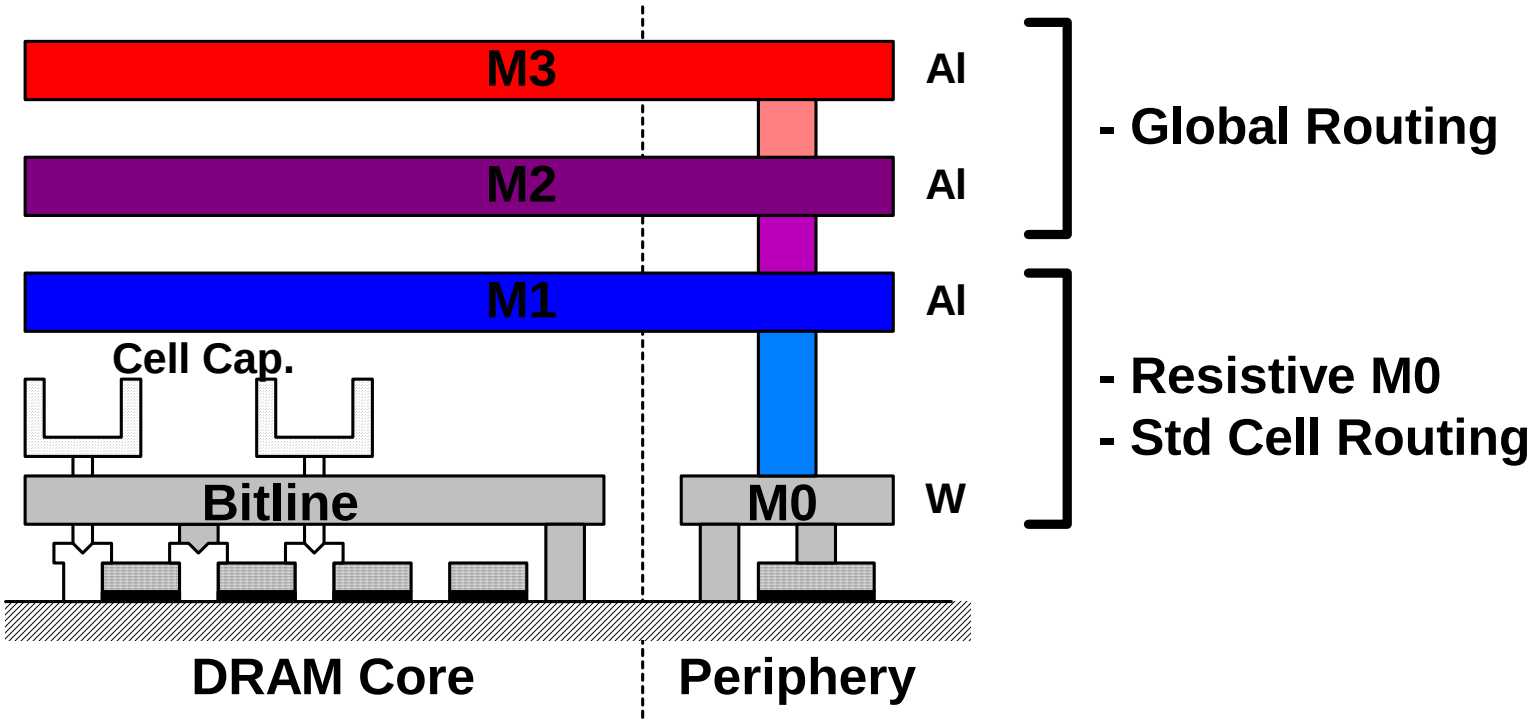
- Fully software controllable
- Adjusting the frame rate during runtime
- Zero-latency frequency change
- PPO with PLL consumes less than 3mW

PPO Circuits and Measurement

: Low Power Technique (7) – Cont'd

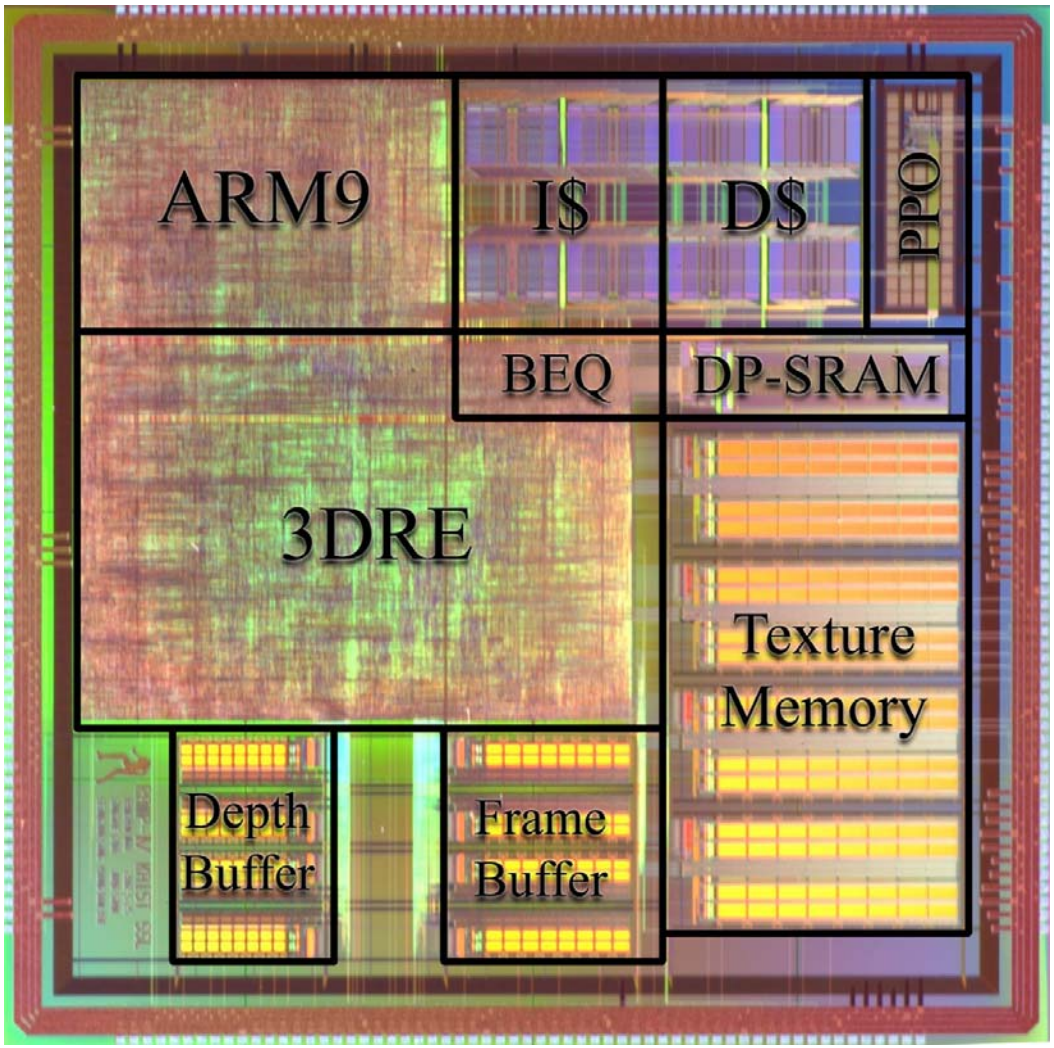


DRAM-based SoC Implementation



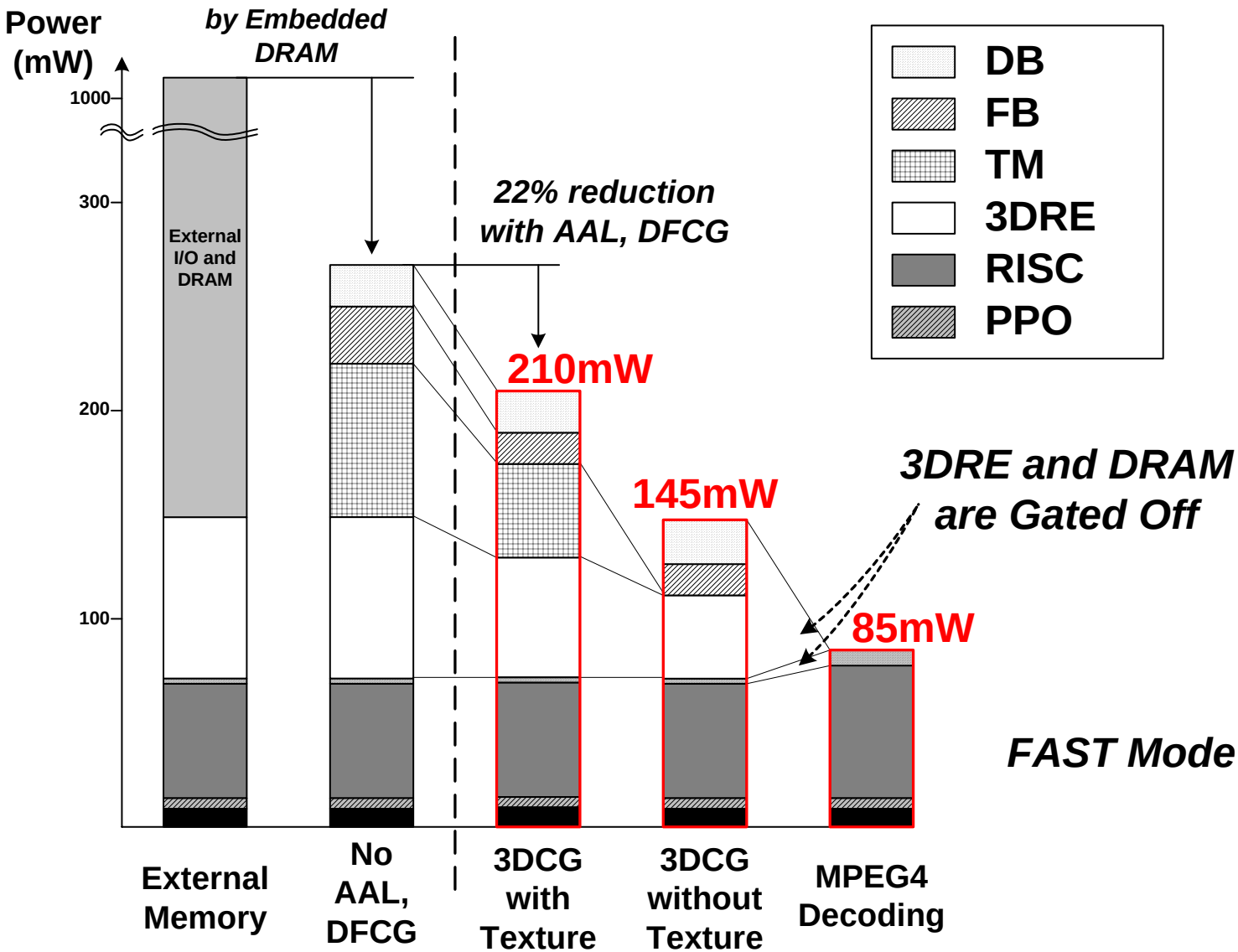
- Low Cost
- Large On-Chip Memory with Little leakage current
- Logic, SRAM, Analog : Periphery Transistors

Die Photograph

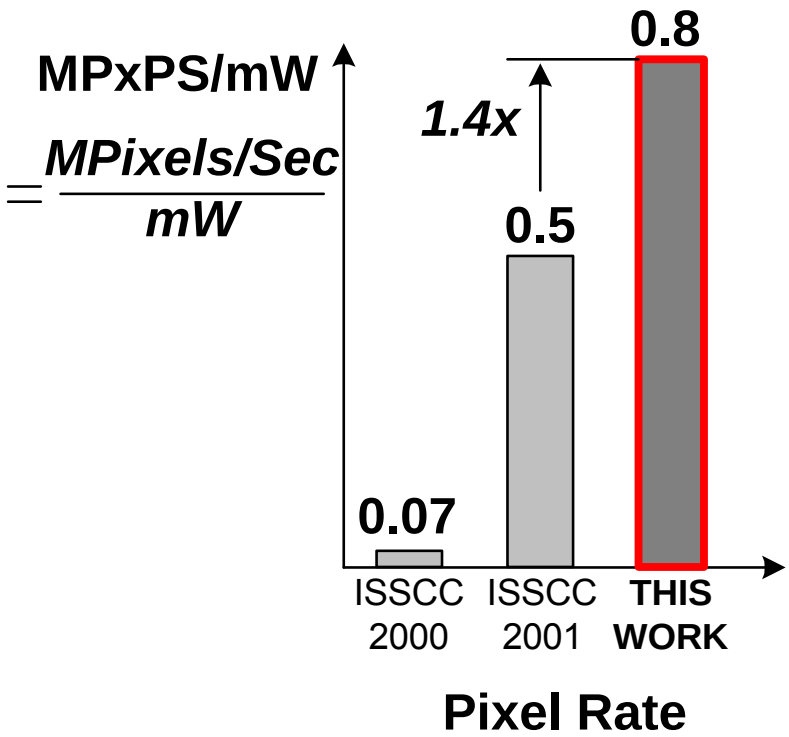


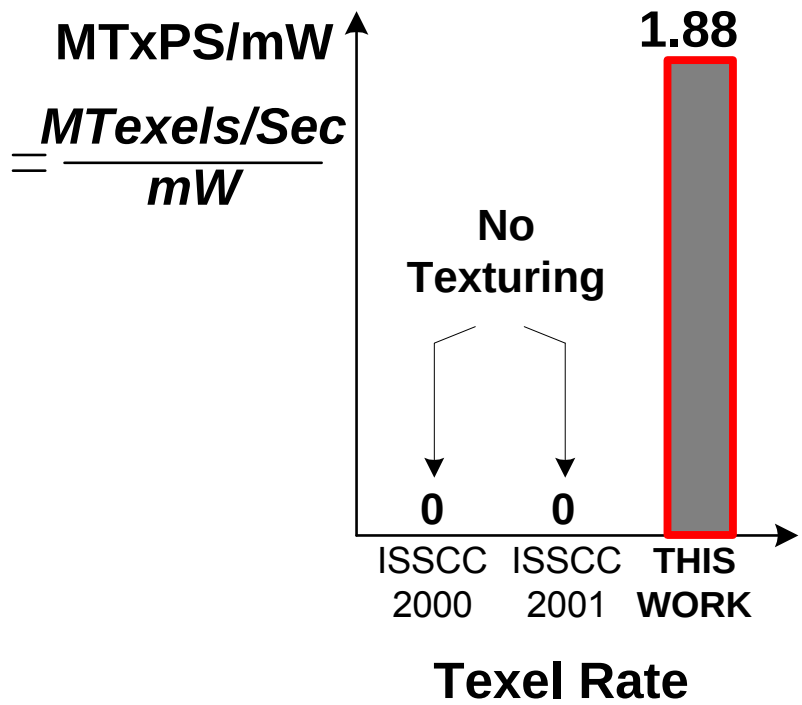
- 0.16µm DRAM
  - 1-W 3-AL
- 11mm x 11mm
- 240pin I/O
- Power Supply
  - 2.0V : DRAM Core
  - 2.5V : Logic/Analog
  - 3.3V : I/O
- Power Consumption
  - Less than 210mW
- Transistors
  - 1M Logic
  - 29Mbits DRAM
  - 72kbits SRAM

System Power Consumption



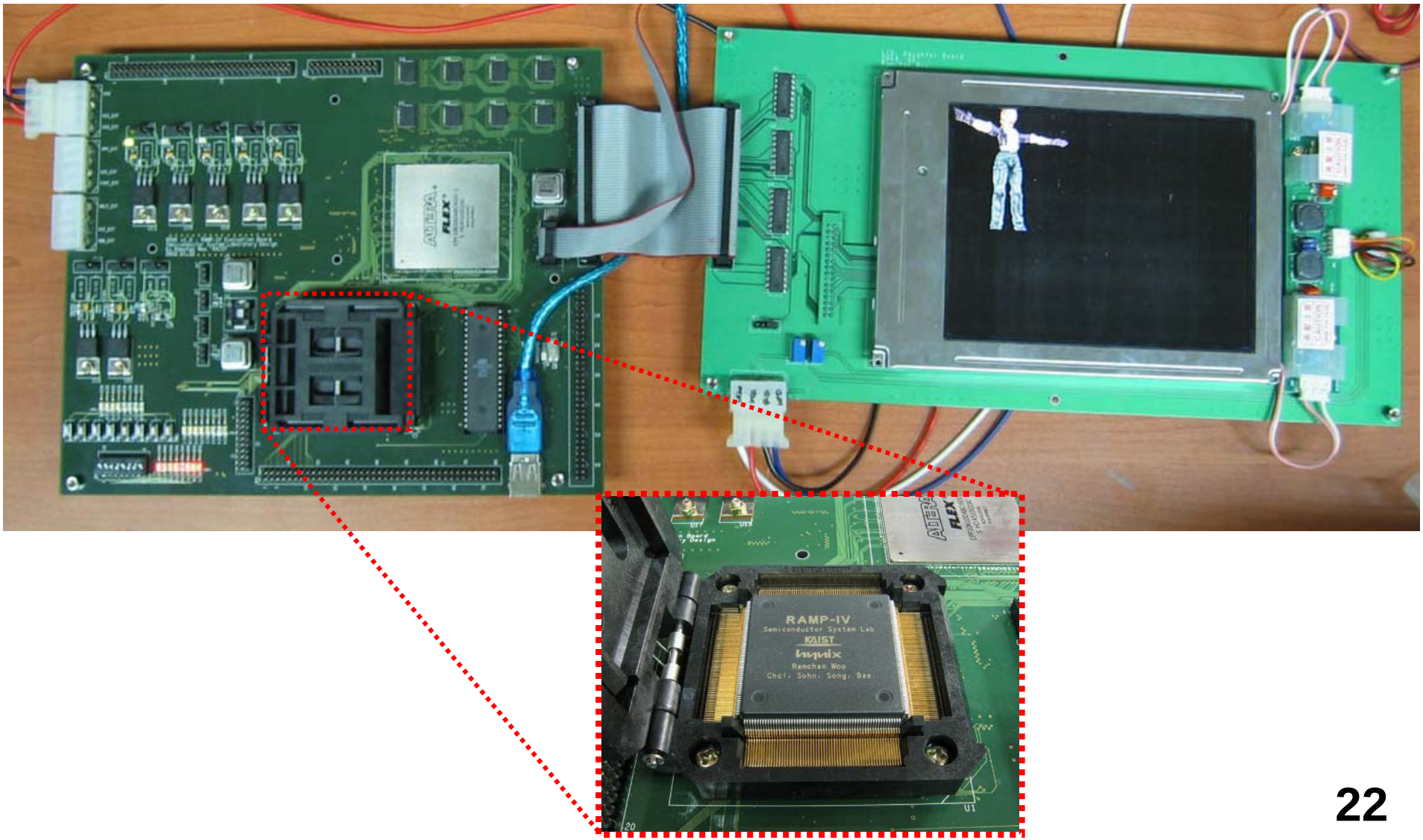
Rendering Performance Comparison





- **Performance Index of Portable 3D**
  - **JSSC Oct. 2002**
  - **Rendering Performance / Rendering Power**
  - **Analogous to MIPS/mW**

System Evaluation Board



Summary

- **Low Power 2D/3D Graphics LSI for Mobile Multimedia Applications**
  - **(1) Highest Integration Level and Performance**
    - **Full 3D Pipeline : RISC + BEQ + 3DRE + DRAM + PPO**
    - **True-Color Pixels at 66Mpixels/s, 264Mtexels/s**
    - **Programmable Special Rendering Effects**
  - **(2) Low Power Techniques**
    - **DFCG, AAL, PPO**
    - **Partial Activation : SRAM, DRAM**
  - **(3) Low Cost Implementation**
    - **0.16μm DRAM Process**
- **<210mW, 121mm^2**
  - **Ready to be on your Hand**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