A 23-GHz Low-Phase-Noise Digital Bang–Bang PLL for Fast Triangular and Sawtooth Chirp Modulation

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Abstract—This paper describes a 23-GHz digital bang–bang phase-locked loop (PLL) fabricated in 65-nm CMOS for millimeter-wave frequency-modulated continuous-wave radars. The presented circuit aims to generate a fast sawtooth chirp signal that grants significant advantages with respect to the more conventional triangular waveform. Such a signal, however, features a very large bandwidth that requires the adoption of a two-point injection scheme. This paper, after intuitively discussing how the nonlinearity of the digitally controlled oscillator affects the accuracy of frequency modulation, presents a novel automatic pre-distortion engine, operating fully in background, which linearizes the tuning characteristic. The 19.7-mA fractional-N PLL having an rms jitter of 213 fs and an in-band fractional spur of −58 dBc is capable of synthesizing fast chirps with 173-MHz/μs maximum slope and an idle time of less than 200 ns after an abrupt frequency step with no over or undershoot.

Index Terms—Bang–bang phase detector, digital phase-locked loop (DPLL), frequency-modulated continuous wave (FMCW), nonlinearity, pre-distortion.

I. Introduction

NEW millimeter-wave (mm-wave) applications, including automotive radars, presence and motion detection, and gesture recognition, are stimulating the development of low-cost radar sensors in CMOS [1]–[4]. The high cutoff frequency of transistors in modern scaled CMOS technologies allows integration of the mm-wave RF transceiver together with a comprehensive digital core required for the sensor DSP. Fig. 1 shows the block diagram of an mm-wave frequency-modulated continuous-wave (FMCW) radar transceiver. Range sensing is based on the measurement of the time-of-flight t_d of the electro-magnetic wave reflected by an object at distance R from the transceiver: $t_d = 2R/c$, where c is the speed of light. In practical applications, direct measurement of t_d is a costly process, because a difference of tens of picoseconds
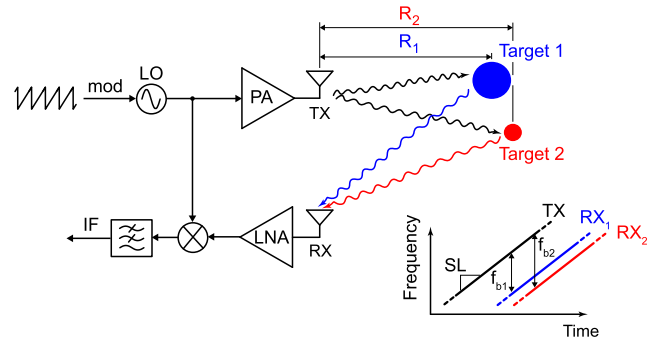
Fig. 1. FMCW radar transceiver architecture.

should be sensed to resolve a centimeter resolution. The typical solution is to use a linearly frequency-modulated signal, i.e., a chirp, and sense the frequency difference, f_b, between transmitted and reflected waves, rather than a time difference, thus significantly reducing the required bandwidth at the baseband (e.g., from 10 GHz to 100 MHz). If the chirp has a slope SL, the receiver detects the beat frequency $f_b = \text{SL} \cdot 2R/c + 2f_v v/c$, where f_v is the carrier frequency and v is the relative velocity. The first term in the above equation is proportional to time-of-flight t_d, while the second term is defined by the Doppler shift. Reducing the period of the chirp T_c allows faster target identification as well as range and velocity sensing. Moreover, it increases the maximum unambiguous velocity $\Delta v_{\max} = c/(4f_v T_c)$ [5]. However, as the chirp period decreases, the impact of the idle time (time between two consecutive chirps as shown in Fig. 2) on the overall power efficiency of the system becomes more important as the power of the RF front-end is wasted during the idle time.

Another advantage of fast chirps is related to the multiple-target scenario depicted in Fig. 1, where two different beat frequencies have to be detected. As the difference in the received power from the two objects depends on their relative radar cross section and can be as large as 60 dB [6], the phase noise of the modulator, up-converted around the most powerful tone, can severely degrade the weaker signal. As it is schematically shown in Fig. 2, if the chirp is faster, then the two beat tones will be more separated in frequency, relaxing phase noise requirements.

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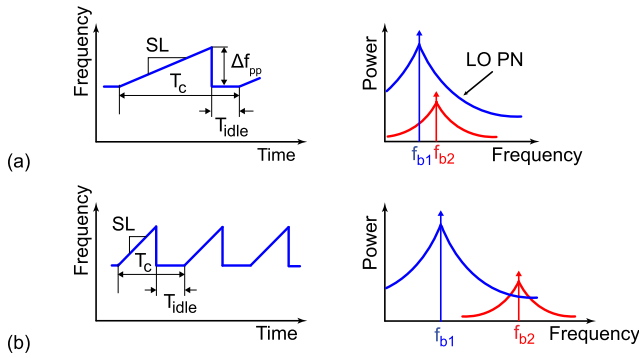
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Fig. 2. Modulation signal and power spectrum at IF output in (a) slow-chirp and (b) fast-chirp cases.

Typically, triangular chirps are preferred to sawtooth ones, because at least two slopes (e.g., SL and −SL) are needed to detect both the range and speed of the target. In practice, $(N + 1)$ different slopes have to be adopted to cope with an N-target scenario. The adoption of several different slopes obviously decreases the radar power efficiency and increases the design complexity [7], [8]. Sawtooth chirps would instead entail the highest power efficiency, as chirp duration can be maximized for the same slope SL. Speed and N-target detection can be solved if the sawtooth chirp is fast enough to make the Doppler shift negligible within the period T_c. The detection of targets and respective distances is done within a single chirp by means of a fast Fourier transform (FFT), so called range FFT. While the relative speed of targets can be detected by tracking the phase progression of a single range-FFT bin over a number of chirps [5].

None of the recently published high-performance chirp generators in CMOS [3], [7]–[9] implemented as frequency-modulated phase-locked loops (PLLs) is able to support fast sawtooth modulations. Because of its sharp drop, a sawtooth chirp requires a much wider bandwidth than a triangular one with the same slope and twice the period. This feature does not allow generating the signal by simply modulating the division factor of the PLL that in other respects would be the optimal solution. The reason is that the low-pass transfer function of the PLL usually shows a bandwidth well below the one required, a fact that causes severe *linear* distortion. The problem can be mitigated by injecting the modulation signal in two different points of the PLL, the so-called two-point injection technique [10], and employing some sort of calibration to match the two paths [11]. This aspect has made attractive the adoption of digital PLLs (DPLLs) as frequency modulators [2], [12]–[14]. Unfortunately, large bandwidth is only one of the requirements to achieve a fast linear sawtooth chirp. *Nonlinear* distortion is the second source of errors in the modulation. For frequency components of the modulation signal lying beyond the PLL bandwidth, the nonlinearity of PLL building blocks generates a distorted modulation even in a PLL with a two-point injection scheme [15]. A fast sawtooth is, clearly, severely affected by this mechanism, since most of its power is typically contained in a spectrum portion well above the PLL bandwidth.

In this paper, we introduce a 23-GHz DPLL for fast chirp generation, in which a wide bandwidth is obtained by
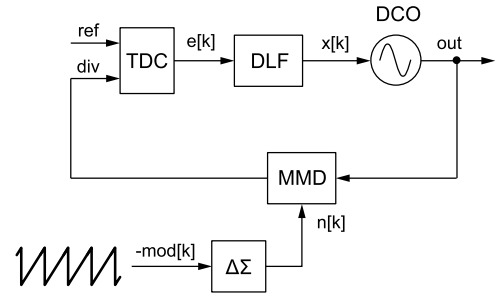

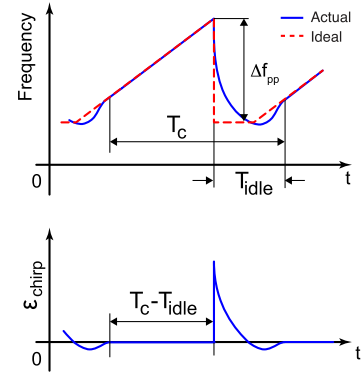Fig. 3. Frequency modulator based on a DPLL.

Fig. 4. Modulation signal and error in the case of finite bandwidth.

adopting the two-point injection technique, while, at the same time, the nonlinear tuning curve of the digitally controlled oscillator (DCO) is calibrated in background by means of a novel digital predistortion (DPD) algorithm running fully in the background [16]. This paper is organized as follows. Section II describes the PLL modulator. Section III introduces the analysis of the impact of DCO nonlinearity on modulation accuracy, while Section IV describes the novel adaptive DPD scheme and Section V the simulation results. Section VI describes the architecture of the DPLL and the design of building blocks, while measurement results are shown in Section VII. Section VIII draws pertinent conclusions.

II. PLL WITH TWO-POINT-INJECTION SCHEME

Fig. 3 shows a DPLL-based FMCW modulator, in which the modulation signal mod[k], sampled at reference rate, changes the fractional-N division factor of the PLL, thus varying its output frequency with fine resolution. The output frequency follows the slow variations of mod[k], only within the PLL bandwidth, while the faster components of mod[k] are low-pass filtered by the PLL transfer function. The (linear) distortion of the chirp due to the finite PLL bandwidth is pictorially sketched in Fig. 4, assuming a sawtooth-like mod[k]. The chirp error ϵ_{chirp} is defined as

$$\epsilon_{\text{chirp}} = \frac{\Delta f_{\text{chirp}}}{\Delta f_{pp}} \tag{1}$$

where Δf_{chirp} if the difference between the ideal and the actual frequency and Δf_{pp} is the peak-to-peak frequency deviation as depicted in Fig. 4. The chirp error changes due to the chirp itself, but an accurate radar systems typically require peak errors below 0.1%.

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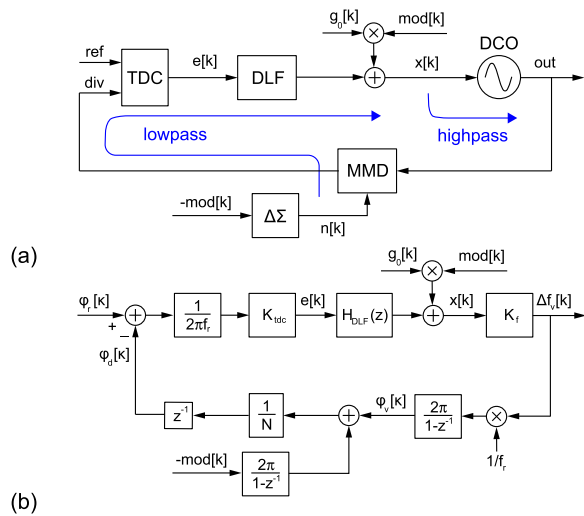CHERNIAK *et al.*: 23-GHz LOW-PHASE-NOISE DIGITAL BANG–BANG PLL

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Fig. 5. DPLL-based FMCW modulator. (a) Architecture with two-point injection. (b) Its linearized model.

Of course, the most critical situation occurs after the abrupt frequency step, where the output frequency variation significantly deviates from the ideal one and the PLL settles with finite time constant. To enable fast sawtooth modulation (e.g., $T_c < 10$ μs), the required PLL bandwidth may range tens or even hundreds of megahertz [15], impossible to achieve with standard crystal references (e.g., at about 40–50-MHz frequency). Not to mention that the PLL is also required to exhibit low phase noise, which is typically achieved at narrow bandwidth. To circumvent this issue and allocate time for PLL settling, a portion of the chirp after the abrupt jump, lasting an idle time T_{idle}, is not exploited for radar detection. In practice, the part of the usable chirp may shrink down to 50% of T_c and the power dissipated during the idle time is wasted.

A solution to decouple loop and modulation bandwidth in a PLL is to inject the modulation signal into two points of the loop [10]. Fig. 5(a) recalls the basic idea, where mod[k] directly modulates the tuning port of the DCO, while $-$mod[k] is injected into the feedback path by modulating the division factor. Fig. 5(b) depicts the linearized model of a PLL with two-point injection technique. Signals ϕ_v, ϕ_d, and ϕ_r represent the phase of the DCO clock, divided-by-N clock, and reference clock f_r, respectively. The gain of DCO and time-to-digital converter (TDC) is denoted as K_f and K_{tdc}, respectively. From Fig. 5(b), it can be seen that the linear superposition of the transfer functions from both modulation inputs to the variation of the output frequency Δf_v (high pass via the DCO and low pass via the divider) is the desired all-pass one over the whole Nyquist band. In the ideal case of perfect matching between the two transfer functions, it is $\Delta f_v = \text{mod}[k] \cdot f_r$ where Δf_v is the variation of the output frequency, and f_r the reference frequency. Moreover, in the two-point topology, mod[k] does not ideally appear at the input of the TDC, because the signal injected into the feedback path cancels out the one injected into the DCO. This property allows the adoption of a single-bit TDC [15].

In practice, the mismatch between the two transfer functions, arising from component spreads, requires some sort of

calibration, which can be achieved by multiplying the modulation signal by a digital gain g_0 [2], [17], as shown in Fig. 5. All-pass transfer from mod[k] to output frequency is obtained when the coefficient g_0 is such that $g_0 \cdot K_f = f_r$, where K_f is the DCO gain (or resolution) in [Hz/bit]. Reference [11] employed a least-mean square (LMS) algorithm running in background to automatically calibrate g_0.

III. NONLINEARITY EFFECTS

Matching between injection paths is mandatory to avoid linear distortion in the two-point modulation scheme. However, the nonlinearity of PLL building blocks, mainly the DCO nonlinear tuning curve, also affects the accuracy of the output frequency modulation. In the presence of nonlinearity, the above-recalled calibration based on a single coefficient, or gain, g_0 is not effective to achieve high accuracy.

A DCO is typically implemented with an LC resonator, whose capacitance C is divided in several unit capacitances, that can be connected or disconnected from the resonator. Nonlinearity in the DCO frequency characteristic mainly arises from two main sources: The first one is the systematic nonlinear link between the tank capacitance C and the output (angular) frequency, i.e., $1/\sqrt{LC}$. The second one is the mismatch among the unit capacitors of the tank, a situation completely equivalent to what happens in digital-to-analog converters (DACs) [18]. In principle, the issue of the $1/\sqrt{LC}$ nonlinearity could be addressed by properly scaling the capacitors in the coarse bank. However, on the one hand, this would not solve the capacitor mismatch issue (or it might even worsen it) and, on the other hand, would complicate the layout of the DCO.

DCO nonlinearity does not play a major role during standard DPLL operation, since the amount of tuning range exploited is small and the impact of nonlinearity is suppressed by the feedback loop. In other words, the tuning input of the DCO varies within a limited range in lock condition. Instead, when a fast and large modulation is applied, the output frequency has to quickly change along a wide range. Therefore, a large portion of the nonlinear tuning curve is exploited and the loop is unable to mitigate nonlinearity because of the fast operation. This behavior is intrinsic to the two-point scheme, since the high-pass injection path practically operates the DCO as it was in the open-loop condition.

Even if the tank capacitance is a linear function of the digital tuning word (in the case of switched capacitors) or of the tuning voltage (in the case of varactors), the systematic nonlinearity $1/\sqrt{LC}$ always occurs. Though the nonlinearity of the $1/\sqrt{(1+x)}$ function is mild and it may be expected to produce negligible errors when the frequency range is a few percent of the center frequency, it becomes problematic in the case of a sawtooth frequency modulation. To get an intuitive picture, let us consider a sawtooth from f_{min} to f_{max} frequency.[1] Let us also denote $K_{f,\text{min}}$ and $K_{f,\text{max}}$ the DCO gain evaluated at f_{min} and f_{max}, respectively. The calibration

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[1]This is obtained with a sawtooth digital waveform mod[k] swinging from 0 to $\Delta f_{pp}/f_r$, where $\Delta f_{pp} = f_{\text{max}} - f_{\text{min}}$, since the PLL output frequency increases by f_r each time mod[k] is incremented by one.
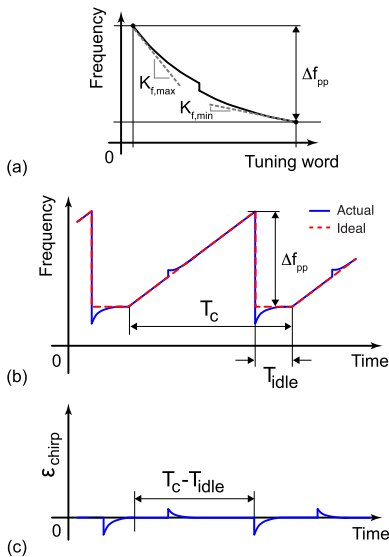
Fig. 6. Impact of DCO nonlinearity. (a) Tuning characteristic. (b) Output frequency. (c) Chirp error.

loop estimates a gain g_0 that matches the average gain of the DCO. Along the ramp of the sawtooth, this inaccurate calibration produces negligible effects, because the low-pass injection path is mainly exploited. However, as soon as the modulation undergoes the step variation from $f_{\max}$ down to $f_{\min}$ and K_f abruptly jumps from $K_{f,\max}$ to $K_{f,\min}$, the PLL is momentarily in a condition where the high-pass path is exploited and a mismatch between the two injection path exists. As shown in Fig. 6, the output frequency deviates from the expected shape, and the error is recovered within some time constants of the PLL.[2] The variation of K_f along the tuning curve is significant. In fact, if x is the tuning word and f the DCO frequency, $K_f = df/dx = (-f/2C) \cdot (dC/dx)$, and if the tank capacitance increment (dC/dx) is constant over the tuning range, we get $K_{f,\max}/K_{f,\min} \approx (f_{\max}/f_{\min})^3$.

It is difficult to mathematically analyze the impact of DCO nonlinearity on chirp error, as the system is nonlinear. Nevertheless, a simplified mathematical model is useful to gain some additional insights. To this purpose, we can consider a perfectly linear DCO featuring a mismatched gain. Let us denote $\epsilon_{K_f} = (K_{f,\max}/K_{f,\min} - 1)$ the relative error. Relying on the linear model of the DPLL with two-point injection depicted in 5(b), we can evaluate the z-transform of the chirp error $\epsilon_{\mathrm{chirp}}[k]$ from (1) as a function of the z-transform of the modulating signal $\mathrm{mod}[k]$. For this analysis, the DCO gain is altered as $K_f(1 + \epsilon_{K_f})$, while the coefficient g_0 is still equal to $g_0 = K_f/f_r$. The resulting chirp error is

$$
\begin{aligned}
\epsilon_{\mathrm{chirp}}(z) &= \frac{\mathrm{mod}(z)[f_r - H_{\mathrm{PLL}}(z)]}{\Delta f_{pp}} \\
&= \frac{\epsilon_{K_f}}{1 + \epsilon_{K_f}} \cdot \frac{\mathrm{mod}(z) \cdot f_r}{\Delta f_{pp}} \cdot \frac{1}{1 + G_{\mathrm{loop}}(z)}
\end{aligned}
\tag{2}
$$

[2]This problem could be avoided if g_0 were adjusted immediately to the new value. This is however impossible, since, to be stable, the LMS loop has to be slower than the PLL response.

where $H_{\mathrm{PLL}}(z)$ is the z-domain transfer function from the modulation signal $\mathrm{mod}[k]$ to the variation of the output frequency Δf_v (ideally a factor f_r), the $G_{\mathrm{loop}}(z)$ is the PLL loop gain, and f_r the reference frequency [15]. Equation (2) quantifies the sensitivity of the chirp error to the DCO gain perturbation ϵ_{K_f}, which models the mismatch between the two injection paths. As the last term in (2) is a frequency response with high-pass shape and bandwidth equal to PLL bandwidth, (2) implies that $\epsilon_{\mathrm{chirp}}[k]$ is obtained after scaling and high-pass shaping $\mathrm{mod}[k]$. In practice, the system is insensitive to the DCO gain mismatch at slow $\mathrm{mod}[k]$ variations (within the PLL bandwidth), but it suffers from it at fast $\mathrm{mod}[k]$ (outside the PLL bandwidth). When the sawtooth signal abruptly changes as a step function, $\mathrm{mod}[k]$ drops from $\Delta f_{pp}/f_r$ to zero and the DCO exhibits a mismatched gain with error ϵ_{K_f}. Therefore, from (2), we can estimate $\epsilon_{\mathrm{chirp}}[k]$ to be a signal with an initial step of height equal to $\epsilon_{K_f}/(1 + \epsilon_{K_f})$, which is about ϵ_{K_f} for small errors, followed by a recovery transient set by the PLL time constant, as schematically shown in Fig. 6. Combining the previous results, the peak error is

$$
\epsilon_{\mathrm{chirp,max}} \approx \epsilon_{K_f} \approx \left(\frac{f_{\max}}{f_{\min}}\right)^3 - 1.
\tag{3}
$$

Thus, an error of about 15% can be estimated for a frequency deviation of 5%.

The second important source of nonlinearity, the element mismatch, is schematically sketched in Fig. 6 as a step in the DCO characteristic. Following the same argument used in the previous discussion, the error $\epsilon_{\mathrm{chirp}}$ induced in the ramp is too fast and is recovered within some PLL time constants. If C_0 is the tank capacitance before the step corresponding to frequency f_v and ΔC_{mm} is the error of the capacitor that is switched ON, the peak $\epsilon_{\mathrm{chirp}}$ can be approximated as follows:

$$
\epsilon_{\mathrm{chirp,max}} \approx \frac{\Delta C_{mm}}{2C_0} \cdot \frac{f_v}{\Delta f_{pp}}.
\tag{4}
$$

For a relative modulation depth $\Delta f_{pp}/f_v$ of 5%, a capacitor mismatch of 0.1% would cause an error of about 2%.

IV. AUTOMATIC DIGITAL PRE-DISTORTION

An adaptive DPD of the modulation signal $\mathrm{mod}[k]$ will be adopted to compensate the DCO nonlinearity. If a non-linear function links the DCO tuning word tw to the output frequency f_v, the DPD should estimate the inverse of this function (which is assumed to be monotonic), and then use it to remap the modulation signal $\mathrm{mod}[k]$ to the tuning word tw. The values of the inverse function are a finite set of numbers, denoted here as $\{c_i\}$. DPD implementations based on polynomial correction or look-up table (LUT) have been presented [2]. Usually, the LUT approach is preferred to the polynomial correction, for its lower hardware complexity and accuracy required in the estimation of the coefficients. However, both the techniques require periodic re-calibration to track temperature and supply fluctuations. An adaptive DPD has been introduced in [19] with the purpose of linearizing the characteristic of the digital-to-time converter (DTC), and then successfully applied to pre-distort the DCO tuning curve
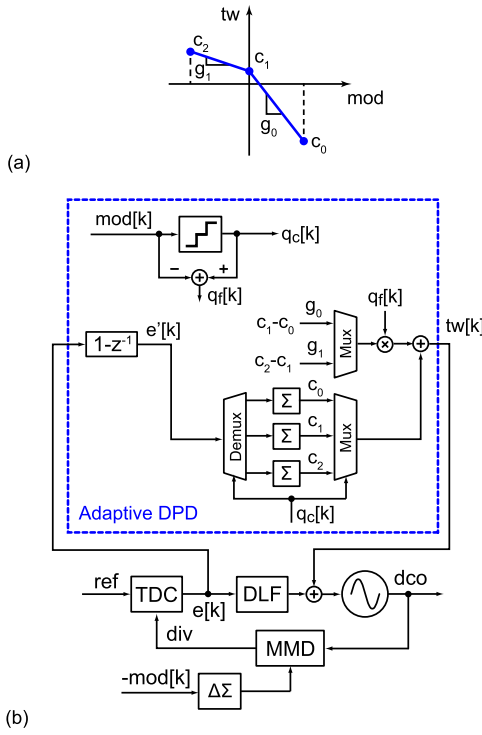
Fig. 7. Adaptive PWL DPD in [11] for the two-gain case. (a) Estimated inverse function. (b) Block diagram.

Fig. 8. Proposed adaptive PWL DPD for the two-gain case. (a) Estimated inverse function. (b) Block diagram.

in [20]. Instead of estimating each point of the inverse curve, which would require large hardware resources, a piecewise linear (PWL) pre-distortion of the nonlinear characteristic is performed, which is only a subset of the c_i points of the inverse characteristic estimated. Then, c_i are linearly interpolated to get the entire characteristic. Of course, the inverse function calculated in this fashion is not exactly the inverse function of the DCO characteristic, even if c_i were accurately evaluated. However, PWL DPD helps mitigate integral nonlinearity with limited hardware resources [19].

The previously reported DPD scheme is schematically shown in Fig. 7, where, for the sake of simplicity, only two sections of the piecewise characteristic are considered. After coarsely quantizing the modulation signal mod[k] into a three-level word $q_c[k]$, the latter is correlated with the first difference $e'[k]$ of the TDC output.[3] In this way, the average correction needed in each of the three regions of mod[k], c_0, c_1, and c_2, is estimated. To properly scale also the least-significant bits of mod[k], $q_f[k]$, the slopes g_0 and g_1 of the PWL curve in Fig. 7(a) are simply obtained by the difference of the c_i coefficients. Unfortunately, in the latter approach, the LMS loops estimating c_i may interact with each other (i.e., c_1 with c_2 and so forth) through the calculation of the slopes g_i (i.e., $g_2 = c_2 - c_1$). To avoid this issue, which slows down the coefficient convergence and in some cases may lead to instability, the g_i gains have to be calculated and used only after the c_i settle and then recalculated cyclically to track variations.

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[3]The first difference is needed to account for the intrinsic integration between mod[k], controlling frequency, and $e[k]$, being proportional to phase error.
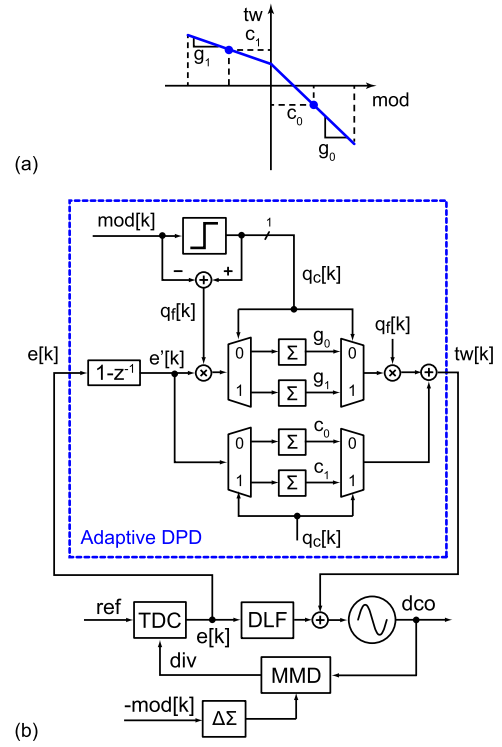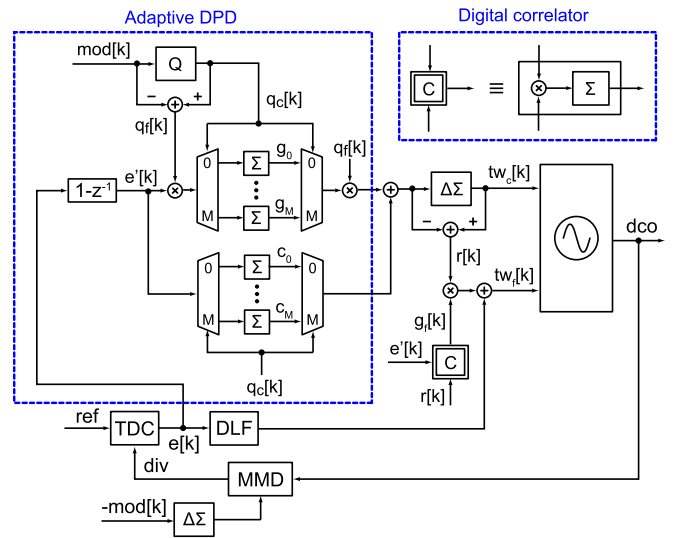

Fig. 9. Practical implementation of the presented adaptive PWL DPD: multi-gain and multi-bank DCO case.

The solution presented here, instead, decouples the estimate of the coefficients c_i from the estimate of the g_i gains. As depicted in Fig. 8, the correlation between the quantization error $q_f[k]$ and $e'[k]$ is exploited to estimate the g_i. In this way, though the number of LMS loops is higher (in general almost doubled), the coefficients within c_i bank no longer interact with each other and the LMS algorithm can operate fully in background. Fig. 9 presents the block diagram of the practical adaptive PWL DPD in the multi-gain case, when a DCO with two capacitor banks is used.
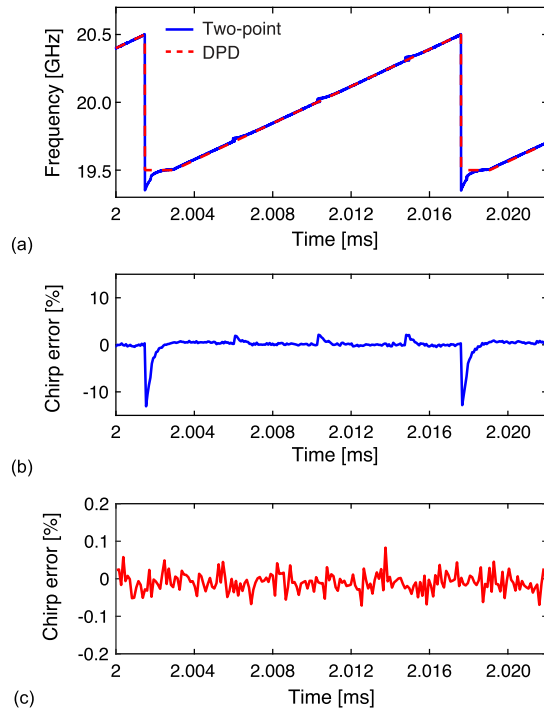
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Fig. 10. Simulation results of the system in Fig. 9. (a) Demodulated output frequency. (b) Chirp error disabling DPD. (c) Chirp error enabling DPD.
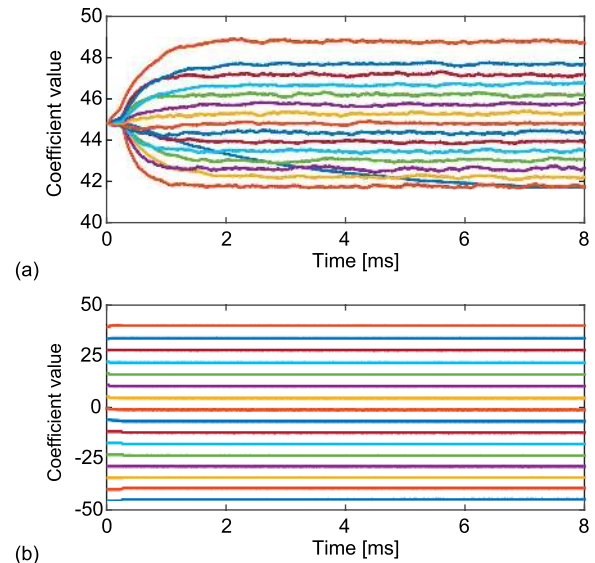

Fig. 11. Simulated convergence of the DPD coefficients for the system in Fig. 9 from start-up to settling. (a) $\{g_i\}$ gains. (b) $\{c_i\}$ coefficients.
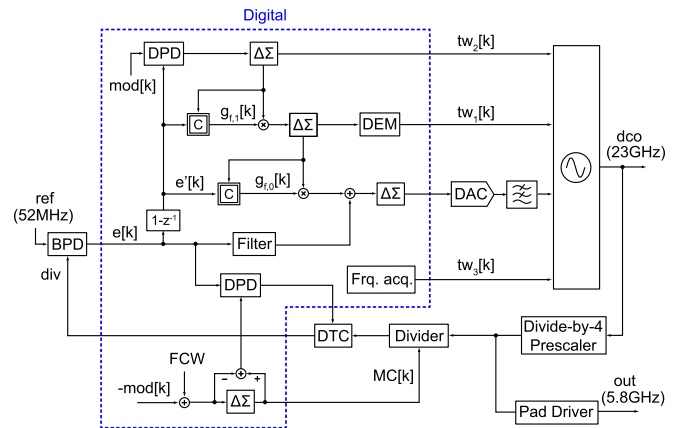

Fig. 12. Block diagram of the implemented FMCW modulator.

An additional g_f gain is estimated to match the coarse and the fine DCO characteristics [11]. Although the gain of the fine bank changes along the DCO coarse characteristic and this would require a multi-gain estimation even in the fine bank, this effect is negligible with the used 5% chirp amplitude.

V. SIMULATION RESULTS

To confirm the intuitive picture provided in Section III and assess the functionality of the presented adapative DPD scheme, the DPLL-based FMCW modulator in Fig. 9 was simulated, where 16 g_i and 16 c_i coefficients are estimated. The DCO was modeled at the behavioral level including both the systematic capacitance-to-frequency nonlinearity and the mismatch-induced nonlinearity. In particular, a 10-bit DCO where every 128th element contains a mismatch of 10 LSBs was accounted for. A sawtooth waveform with a $\Delta f_{pp} = 1$ GHz around a 20-GHz carrier is generated. Fig. 10 presents the simulation results of the DPLL disabling the DPD (in practice, the conventional two-point modulation scheme in Fig. 5) and enabling the presented DPD scheme. The chirp error over time in Fig. 10(b) shows the predicted steps with relatively slow recovery at both the sawtooth abrupt step (because of systematic nonlinearity) and at each random step in the tuning characteristic (because of element mismatch). The chirp error $\epsilon_{chirp,max}$ at the abrupt step predicted from (3) of about 15% is close to the simulated peak error of about 13%. Fig. 10(c) shows the chirp error when DPD is enabled. The obtained results demonstrate that DPD effectively linearizes the DCO characteristic significantly reducing the chirp error. Finally, Fig. 11 reports the transient of the g_i and c_i coefficients from start-up to settling, using the training signal shown

in Fig. 10(a). The DPD requires about 2 ms to bring the chirp error below 0.1%. This is because about 100 periods of the training sequence are needed to achieve the required accuracy of the coefficients estimation [24]. Although one of the g_i coefficients in Fig. 10(a) has a slower convergence, its impact on the chirp error is negligible, as it refers to the boundary of the DCO characteristic.

VI. PLL DESIGN

The implemented PLL-based FMCW modulator is presented in Fig. 12. The DPLL is based on a binary phase detector (BPD) (or single-bit TDC), which operation in random noise regime is enabled by means of a DTC, which is employed to cancel the quantization noise introduced by a second-order digital $\Delta\Sigma$ modulator driving the feedback frequency divider [21]. To ensure low spur and phase noise operation, the DTC is also pre-distorted with DPD [19]. The feedback frequency divider is fed with a prescaled-by-four version of the DCO output clock, which allows a low-power
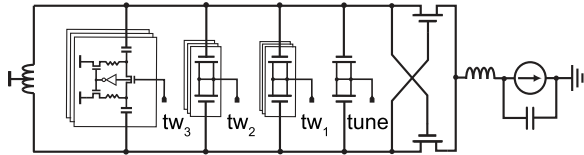
Fig. 13.   DCO circuit schematic.

implementation in CMOS logic. The modulation signal mod[k] is simultaneously added to the frequency control word and applied to the coarse tuning bank of the DCO. The DPD scheme, which was presented in Section V, is applied to the coarse modulation bank, since its mismatch and nonlinearity are the most significant ones. The DPD was implemented with 16 segments as a compromise between the accuracy of the nonlinearity correction and the hardware overhead based on the DCO characteristic from post-layout simulations. The driving scheme of the finer banks is based on cancellation of the quantization error introduced in the coarser bank. A first-order digital $\Delta\Sigma$ modulator is employed as a quantizer at each modulation bank, since its quantization noise can be effectively utilized for the estimation of $g_{f,0}$ and $g_{f,1}$ gains (shown in Fig. 12) required to relate the characteristics of each bank [11].

To achieve fine frequency resolution, the finest bank is implemented as a cascade of a DAC and an analog low-pass RC filter, driving a varactor. A separate bank is dedicated to the frequency-acquisition loop. The PLL is fed with a 52-MHz clock, which is used to clock the digital core. The 5.8-GHz output of the divide-by-four prescaler that feeds a pad driver is used for testing. This relaxes the bandwidth requirements for the signal analyzer, because it scales down by four also the peak-to-peak deviation Δf_{pp} of the frequency modulation.

The circuit schematic of the DCO is depicted in Fig. 13. To ensure robust start-up without additional circuitry, a class-B oscillator topology with an nMOS cross-coupled differential pair has been preferred over a class-C implementation. The main tank inductor is implemented as a single-turn coil with a center-tap connected to the supply voltage and with five turns of a top metal layer connected in parallel. A tail filter made of a 75-pH spiral inductor and a 10-pF capacitor is employed to filter the noise of the tail current source, as well as to provide higher impedance at the second-harmonic frequency similar to the concept proposed in [22]. The oscillator features four different digitally controlled capacitor banks. The coarsest bank, implemented using switched metal–metal capacitors, is dedicated to coarse frequency tuning. The finer banks, dedicated to modulation, are implemented using digitally controlled MOS varactors. The finest tuning bank is implemented using an analog-tuned MOS varactor. DCO frequency is centered at around 22 GHz, which is a couple of GHz away from the center of the 24-GHz FMCW radar band because of some inaccuracy in the parasitic extraction. The achieved tuning range is about 17%.

The DTC is realized in a current-mode logic as a cascade of a buffer with capacitive DAC load followed by a slope regeneration buffer. The capacitive DAC is implemented using digitally controlled MOS varactors segmented in coarse and
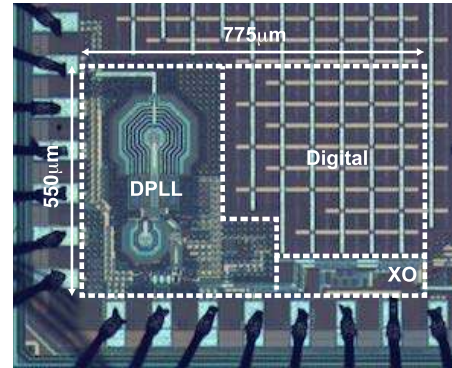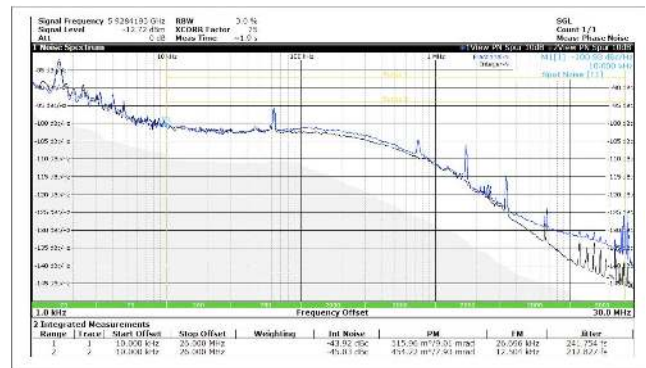

Fig. 14.   Die photograph.

Fig. 15.   Measured phase noise spectra in both integer-N and fractional-N modes at the divider-by-four output.

fine banks. The DTC covers about 150-ps range with a fine resolution of about 300 fs. The fine bank of the DTC is driven by a digital $\Delta\Sigma$ modulator that shapes its quantization noise, which is further filtered by the digital loop filter. This allows keeping DTC quantization noise significantly below other noise contributors.

VII. MEASUREMENT RESULTS

The prototype has been fabricated in a standard 65-nm LP CMOS process with no ultra-thick metal layer option. The analog and the digital portions of the chip whose photograph is shown in Fig. 14 occupy approximately the same share of the total 0.42 mm^2 area. The output of the frequency divider by four is used to carry out all the measurements. The output of the pad driver is wire bonded to the test board and used for testing. This setup reducing the output frequency to around 5.8 GHz simplifies both phase-noise measurement, which does not require external mixers, and modulation-analysis measurement, as it scales down by four the modulation depth.

The phase noise spectra in integer- and fractional-N modes measured by an R&S FSWP phase-noise analyzer are shown in Fig. 15. In both the cases, the in-band noise plateau is at about -102 dBc/Hz and the phase noise at 1 MHz offset from the carrier at 5.928 GHz is about -112 dBc/Hz. The latter corresponds to about -100 dBc/Hz at 1-MHz offset when referred to the actual DCO output at 23.712 GHz. In the fractional-N mode, the far-out phase noise exhibits a slight
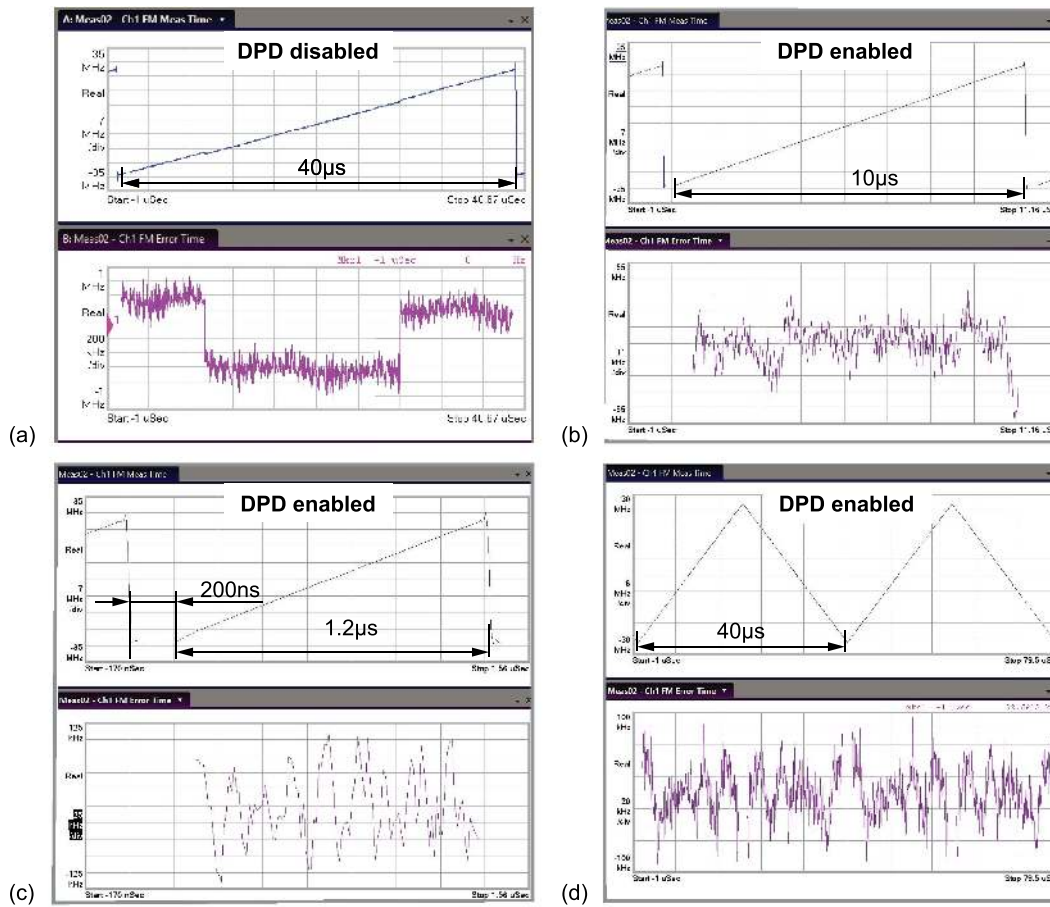
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Fig. 16.   Chirp measurements at divider-by-four output. (a) 40-μs sawtooth with single-gain calibration (no DPD). (b) 10-μs-sawtooth with DPD. (c) 1.2-μs sawtooth with DPD. (d) 40-μs triangular with DPD.

increment, increasing the absolute jitter from 213 fs (in the integer-N mode) to about 242 fs (in the fractional-N mode). In-band fractional spur is below -58 dBc [16].

An Anritsu MS2850A featuring 1-GHz demodulation bandwidth has been employed as a vector signal analyzer (VSA). To assess the efficacy of the DPD, the modulator has been at first tested without enabling the adaptive DPD. A single gain for each bank of the DCO is estimated, which corrects for mismatches between coarse and fine banks, but leaves the mismatches among the elements of the coarse bank and the systematic nonlinearity uncorrected. Fig. 16(a) shows the demodulated frequency signal for a sawtooth chirp with 40-μs period and 52-MHz frequency deviation at the output of the divide-by-four block (equivalent to 208 MHz at the DCO output) and the corresponding frequency error. The effects of DCO nonlinearity are clearly visible in the scope, and the peak chirp error is about 1.058 MHz, which is about 2% with respect to the peak-to-peak chirp deviation.

The following figures [Fig. 16(b) and (c)] present instead the measurements when the adaptive DPD is enabled. The peak-to-peak frequency deviation is 52 MHz in both the cases (equivalent to 208 MHz at the DCO output). In Fig. 16(b), the chirp rise time is 10 μs, the resulting peak frequency error is below 50 kHz (equivalent to 200 kHz at the DCO output), which is less than 0.1% of the maximum frequency
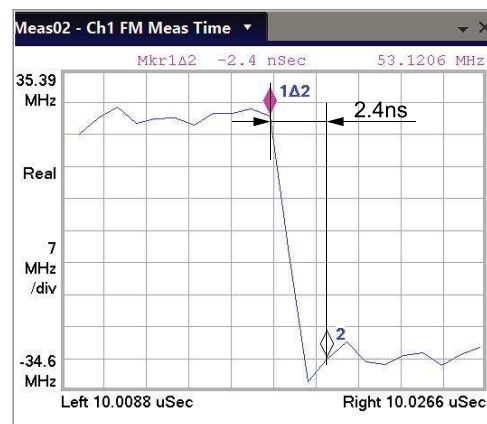
Fig. 17.   Abrupt 52-MHz frequency step at the end of the sawtooth modulation, measured at the divider-by-four output.

deviation, and the rms chirp error is 0.06%. Fig. 16(c) shows the same frequency deviation covered in only 1.2 μs, which results in a state-of-the-art chirp slope of 173 MHz/μs at the DCO output. In this case, the peak error is below 100 kHz (i.e., below 0.2%). The circuit can generate also triangular chirps: Fig. 16(d) shows the demodulated waveform for a 40-μs period. The effectiveness of the proposed technique,

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TABLE I

PERFORMANCE COMPARISON

	This Work	[2]	[14]	[23]	[3]	[9]	[4]
Architecture	BBPLL+TPM	ADPLL+TPM	HPLL+TPM	ADPLL+TPM	Analog PLL	DPLL	Analog cascaded PLL
Freq. range [GHz]	20.4–24.6	56.4–63.4	12.2–26.4	8.4–9.4	75–83	36.3–38.2	76–81
Technology	65nm CMOS	65nm CMOS	32nm SOI-CMOS	65nm CMOS	130nm BiCMOS	40nm CMOS	45nm CMOS
Ref. freq. [MHz]	52	40	133	276.8	125	120	40
Chirp type	Saw-tooth/ Triangular	Triangular	Triangular	Triangular	Saw-tooth	Triangular	Saw-tooth
Chirp duration [μs]	1.2–315	420–8200	1300	5–220	50–225	50–2000	40
Saw-tooth idle time [μs]	0.2	n/a	n/a	n/a	15	n/a	15
Max. chirp Δf_{pp} [MHz]	208	1220	8000	956	8000	500	4000
Max. chirp slope [MHz/μs]	173	4.76	10	32.6	100	9.1	100
RMS freq. error† [kHz]	124/112 (0.06%/0.05%)	384 (0.03%)	n/a	1900 (0.12%)	3200 (0.04%)	820 (0.16%)	n/a
Phase noise* [dBc/Hz]	−90	−87.7	−79.3	−86.2	−97	−73.7	−91
Spur level [dBc]	−58	−62	n/a	n/a	n/a	−55	n/a
Power [mW]	19.7	48	30	14.8	590	68	n/a
Area [mm^2]	0.42	2.2	0.28	0.18	4.42	0.18	n/a

* At 1-MHz offset referred to a 79GHz carrier.
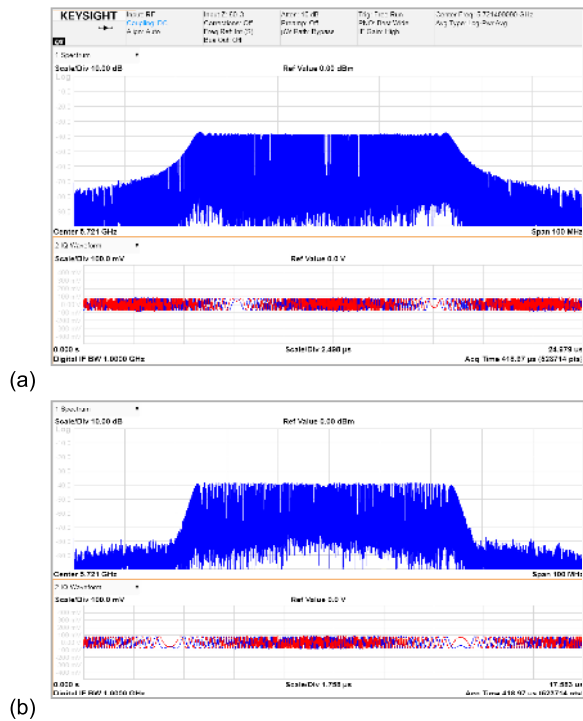† At max. chirp slope.

(a)

(b)

Fig. 18. Spectra of the modulated carrier with 52-MHz peak-to-peak frequency deviation at the divider-by-four output. (a) Sawtooth. (b) Triangular chirp.

to achieve very fast modulation, is probably even better demonstrated in Fig. 17 that highlights the falling edge of the demodulated frequency signal of Fig. 16(c). The idle time required to match the 0.1% error specification is lower than 2.4 ns with no over or undershoot, thanks to the introduced DPD circuit that allows to exploit completely the two-point modulation technique.

Finally, the spectra of the carrier-modulated by sawtooth and triangular signals, with 52-MHz frequency deviation in both the cases, measured with a Keysight PXA spectrum analyzer are shown in Fig. 18. Comparing the presented chirp generator with other state-of-the-art CMOS and BiCMOS implementations in Table I, we can conclude that the presented DPLL with two-point injection and DCO predistortion is able to generate chirps with the largest maximum slope at better than 0.1% linearity, at competitive phase-noise and power consumption levels.

VIII. CONCLUSION

This paper has presented a 23-GHz FMCW modulator based on a DPLL with two-point injection, which is capable of fast sawtooth and triangular chirp generation. The impact of DCO nonlinearity, induced by systematic capacitance-to-frequency nonlinearity and element mismatches, on chirp linearity has been analyzed. A novel DPD algorithm of the DCO has been introduced, which operates fully in background, provides robust convergence, and enables fast sawtooth chirp generation with linearity better than 0.1%, slopes up to 173 MHz/μs, and idle time that can be reduced to just 2.4 ns with no over or undershoot.

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