A 24-GHz, +14.5-dBm Fully Integrated Power Amplifier in 0.18-μm CMOS

Abbas Komijani, *Student Member, IEEE*, Arun Natarajan, *Student Member, IEEE*, and Ali Hajimiri, *Member, IEEE*

***Abstract*—A 24-GHz +14.5-dBm fully integrated power amplifier with on-chip 50-Ω input and output matching is demonstrated in 0.18-μm CMOS. The use of substrate-shielded coplanar waveguide structures for matching networks results in low passive loss and small die size. Simple circuit techniques based on stability criteria derived result in an unconditionally stable amplifier. The power amplifier achieves a power gain of 7 dB and a maximum single-ended output power of +14.5-dBm with a 3-dB bandwidth of 3.1 GHz, while drawing 100 mA from a 2.8-V supply. The chip area is 1.26 mm^2.**

***Index Terms*—Amplifier stability, CMOS integrated circuits, coplanar waveguides, phased arrays, radio transmitters, silicon.**

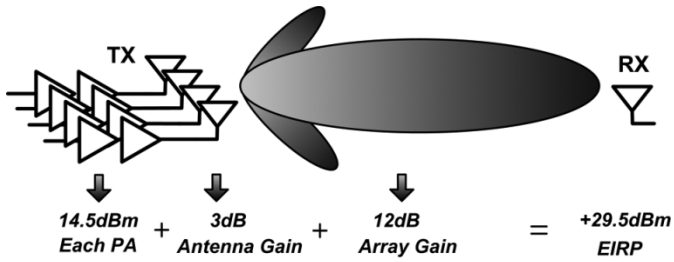

Fig. 1. A four-path phased array transmitter for a 24-GHz point-to-point wireless connection.

I. Introduction

THE quest for multigigabit-per-second data rates in wireless networks has generated interest in the large bandwidth available at high frequencies. The Industrial, Scientific, and Medical (ISM) band at 24 GHz has emerged as a viable candidate for gigabit-per-second wireless network solutions [1]. The allocation of the 22–29-GHz band for wireless vehicular radar applications has added to the attractiveness of the frequency spectrum around 24 GHz [2]. As a result, research on 24-GHz-band wireless technologies has accelerated, with receiver building blocks being demonstrated in GaAs pHEMPT [3] and SiGe BiCMOS [4], [5]. A fully integrated eight-path phased-array receiver in SiGe has also been reported at this frequency [6]. The implementation of these high-frequency systems in CMOS technologies will enable unprecedented levels of integration, making it possible to realize new architectures that combine microwave, analog, and digital circuitry on the same substrate at low cost. While there have been some recent efforts to implement building blocks above 20 GHz on CMOS processes [7]–[10], the power amplifier (PA) reported in this paper, and the fully integrated four-element phased-array transmitter of which it is a part [11], represent the first efforts to integrate a complete multi-element transmitter with on-chip PAs in a CMOS process, at 24 GHz.

An integrated CMOS PA at 24 GHz presents several challenges. The two most important issues are the low unity power gain frequency, $f_{\max}$, of MOS transistors and the loss of on-chip passive elements, such as inductors and transmission lines, required for impedance matching. For narrowband amplifiers, where device capacitance is normally tuned out, $f_{\max}$ is a better metric for device speed than f_T. In MOSFETs, $f_{\max}$ is limited primarily by the series gate resistance [10]. Generally, MOS transistors have lower f_T and $f_{\max}$ as compared to SiGe bipolar transistors fabricated with the same feature size [12]. In the 0.18-μm process used in this design, the NMOS transistors, with an optimum layout, have an $f_{\max}$ of 65 GHz, which is almost a factor of two smaller than the $f_{\max}$ of their SiGe bipolar counterparts.

Lossy on-chip passives present another barrier to the full integration of a high-frequency PA. Skin effect results in larger ohmic losses in inductors and transmission lines at high frequencies. The skin depth in aluminum at 24 GHz is 0.5 μm, which negates some of the advantages of a thick top metal layer, though the lateral sidewalls still help in reducing loss. Although copper has better conductivity, in practice, its performance can be additionally degraded by the cheese and fill rules necessary for stress relief during fabrication. Due to the relatively high conductivity of the substrate in most CMOS processes, the inductors and coplanar waveguide transmission line structures have substrate-induced losses as well. The combination of low active gain at high frequencies and high loss in impedance-matching networks reduces the power gain of a single-stage amplifier. As a result, it becomes necessary to cascade an impractically large number of amplifier stages to achieve desired output power levels.

In this design, a substrate-shielded coplanar waveguide structure is implemented that effectively lowers substrate loss and reduces on-chip wavelength. This is an enhanced version of the slow-wave coplanar structure presented in [13]. This structure is used to design the fully integrated 24-GHz CMOS PA described in this work. In Section II, we calculate the output power required at 24 GHz for two applications, namely wireless point-to-point communication and short-range radar. In Section III, the transmission-line structure is described. The design of the amplifier is also detailed and the stability of a single transistor element and a cascode transistor pair is analyzed. Measurement results for the amplifier are presented in Section IV.

Manuscript received December 8, 2004; revised February 25, 2005.

The authors are with the California Institute of Technology, California Institute of Technology, Pasadena, CA 91125 USA (e-mail: komijani@caltech.edu).

Digital Object Identifier 10.1109/JSSC.2005.848143

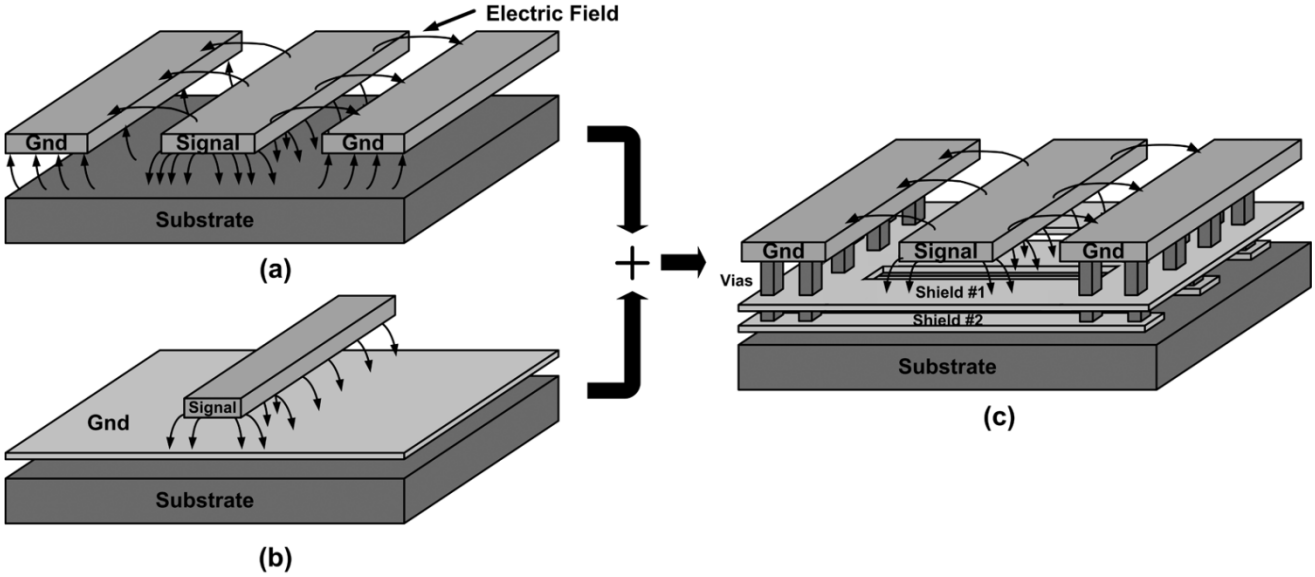

Fig. 2. Combination of (a) CPW and (b) microstrip structures to realize (c) substrate-shielded CPW structure.

II. Power Requirements in the 24-GHz Band

The Federal Communications Commission (FCC) permits point-to-point wireless communication in the 24–24.25-GHz band, subject to limitations on the transmitted power and directionality of the transmitter. At a distance of 3 m from the transmitter, the maximum electric field permitted is 2.5 V/m. This translates to an average effective isotropically radiated power (EIRP) of 29.7 dBm.[1] As shown in Fig. 1, a phased-array transmitter could be employed to achieve the required EIRP and provide electronic beam-steering capability. For an antenna array, the total gain is the product of the gain of each antenna and the array factor. The PA reported in this study is capable of generating up to +14.5-dBm power at 24 GHz. By using this PA in a four-element phased-array system (that provides 12 dB of array gain), with antennas that have at least 3 dB gain, an EIRP of +29.5 dBm can be achieved [11].

The FCC has also opened up 7 GHz of bandwidth from 22 to 29 GHz for vehicular short-range radar applications. In this case, there is an average radiated power limit of −41 dBm/MHz which, if used over the entire 7-GHz bandwidth, corresponds to an EIRP of −2.5 dBm. Therefore, an amplifier designed for this application does not need to generate high output power and must instead be designed to have large bandwidth.

III. Circuit Design

This section describes the design evolution of the amplifier. First, the substrate-shielded coplanar waveguide structure, an important element in the design of the PA, is presented. Next, we discuss amplifier stability and the design techniques used to achieve unconditional stability for all bias points, followed by the design of the amplifier matching networks. Finally, we describe the techniques used to minimize the effect of pad capacitances and wire-bond inductances.

[1] $S = |E|^2/2\eta_o$, where S is power density, $|E|$ is the magnitude of the electric field in space, and $\eta_o = \sqrt{\mu_o/\varepsilon_o} \approx 377\ \Omega$ is the characteristic impedance of free space.

A. Substrate-Shielded Coplanar Waveguide Structure

At 24 GHz, large capacitive coupling to substrate lowers the quality factor of inductors, making inductor-based impedance matching networks lossy. On the other hand, this frequency is not high enough for direct application of standard transmission line structures. For example, in SiO_2 dielectric, the wavelength (λ) at 24 GHz is 6.3 mm. Therefore, the transmission lines required for on-chip matching networks will have high loss because of their long length.

As shown in Fig. 2(a), in coplanar waveguide (CPW) structures designed in CMOS processes with a relatively high substrate conductivity $(\sim 10\ \Omega \cdot \text{cm})$, capacitive coupling to the substrate is often the dominant source of high-frequency loss [14]. On the other hand, in the on-chip microstrip structure, shown in Fig. 2(b), substrate-induced losses are minimal due to the shielding effect of ground plane. However, the close proximity of the ground plane to the signal line results in a narrow signal line for practical impedance levels. This constraint increases ohmic losses in the signal line. Fig. 2(c) shows the substrate-shielded coplanar structure that is a combination of the two structures. Slotting the bottom plate forces the return current to be mostly concentrated in the coplanar ground lines. The large separation between signal and return currents causes more magnetic energy to be stored in space, resulting in a larger distributed inductance per unit length, L_u. However, the proximity of the slotted ground line to the signal line results in high capacitance per unit length, C_u. Simultaneously high values of L_u and C_u lead to slower wave velocity $(v = 1/\sqrt{L_u C_u})$ and hence shorter wavelengths.

Another way to look at this structure is to view it as a CPW structure with periodic capacitive loading. This is similar to the inductive loading concept [15], however, in this case, extra capacitance is added by placing the patterned ground beneath the coplanar structure. Therefore, the capacitance per unit length of the structure is increased, thereby slowing down the wave.

In the implemented structure, the velocity is reduced by more than a factor of two, and as a result the wavelength at 24 GHz in

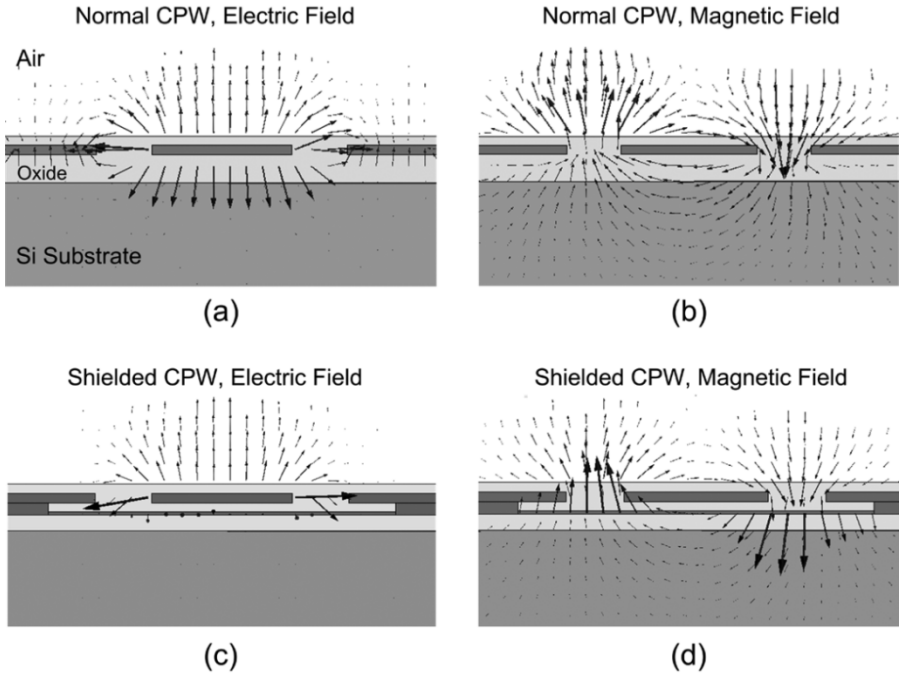

Fig. 3. Electric and magnetic field distributions from 3-D EM simulations of (a), (b) a normal CPW structure and (c), (d) a substrate-shielded CPW structure.

this structure is 3 mm. Furthermore, as opposed to a microstrip structure, reasonable impedance levels are achieved for large signal line widths of 60 μm thereby decreasing ohmic losses. The combination of lower ohmic losses and shorter length of the transmission lines lead to a much lower passive loss in the matching networks. As the MOS transistor gain at high frequencies is low, this reduction in passive loss is critical to achieving desired gain and output power.

As shown in Fig. 2(c), in the implemented structure, the two coplanar ground lines are forced to the same potential with vias to the patterned shield. This acts as an airbridge, allowing only one fundamental TEM mode to propagate. Also, a second shield layer is placed beneath the first shield layer, with metal stripes covering slots of the first layer, thereby completely isolating the coplanar structure from the substrate.

B. Characterization of the Substrate-Shielded CPW Structure

The simulated electric and magnetic fields of a cross section of the substrate-shielded CPW structure with and without slotted shields is shown in Fig. 3. In the shielded structure the electric fields do not penetrate into the substrate, reducing capacitively coupled substrate losses. Though the penetration of the magnetic field into the substrate is not affected by the presence of the shield, EM simulations indicate that this does not contribute significantly to the loss as the eddy currents are limited.

To characterize the substrate-shielded CPW structure, a separate test structure was fabricated in the same process as the amplifier. The test structure was designed for a characteristic impedance of 27.5 Ω, the same impedance used for impedance matching in the PA. This choice of low characteristic impedance, as described in Section III-E, minimizes passive loss. Fig. 4 shows the die photograph of this test structure.

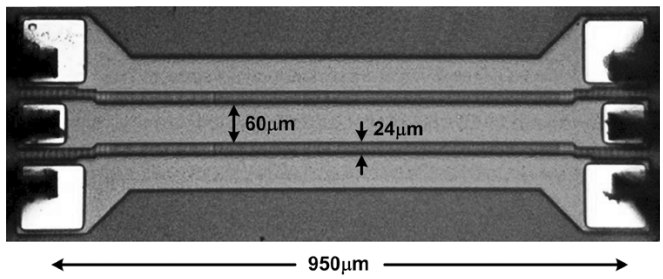

Fig. 4. Die photograph of the substrate-shielded CPW test structure; shield layer consists of 4-μm-wide stripes with 2-μm spacing.

The top three metal layers were used for the transmission-line structure. The top metal layer is 4-μm-thick aluminum and is located 11.7 μm above the substrate. The two shield layers use 1.25-μm aluminum and 0.3-μm copper metal layers placed 5.3 μm and 9.5 μm beneath the bottom of the top metal. Three-dimensional (3-D) electromagnetic simulations with HFSS were performed to accurately simulate a short length of the line, while quasi-planar electromagnetic simulations with IE3D were used as a faster approach to simulate T-junctions and discontinuities [16], [17].

The S-parameters of the line measured in a 50-Ω environment are shown in Fig. 5. A Short-Open-Line-Thru (SOLT) calibration was performed up to the probe tips. A wideband model of the transmission line with parameters shown in Table I was fitted to the measurement results. Compared to a single-frequency fit [18], this is a more physical interpretation of the measured data and is less susceptible to measurement errors at a single frequency. To accommodate the skin effect, the loss of the transmission line, in decibels, was assumed to be proportional to the square root of the frequency [19]. As shown in Fig. 5, this results in a wideband curve fit.

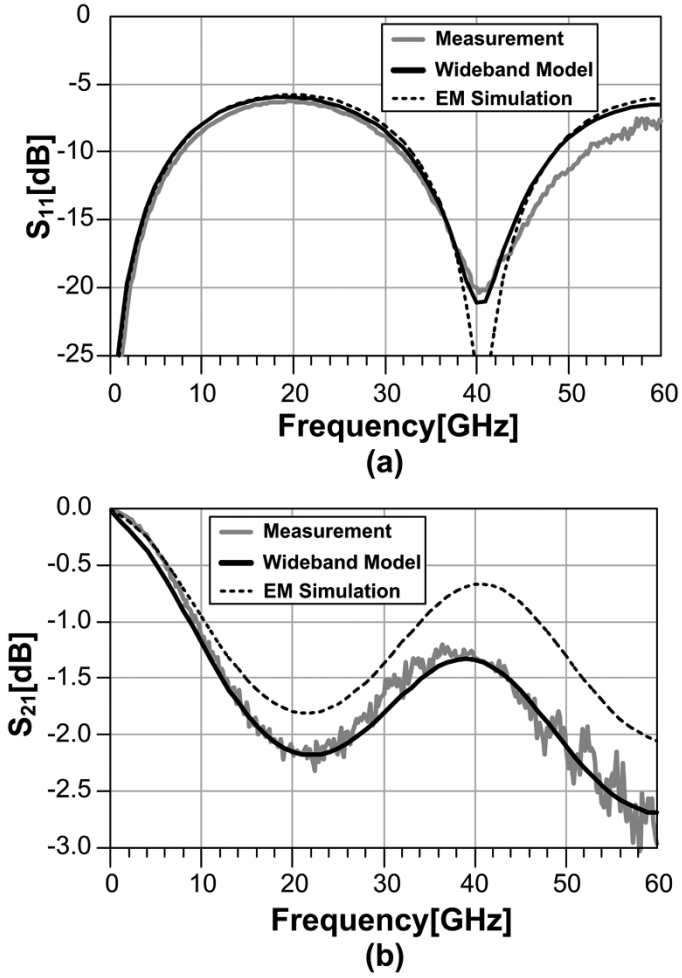

Fig. 5. Simulated and measured S-parameters of the transmission line embedded in a 50-Ω system. (a) Reflection parameters. (b) Transmission parameters.

C. Single-Transistor Power Gain and Stability

The effect of loss elements in a MOS transistor can be better understood by calculating its maximum available power gain which is the maximum gain that can be achieved from the transistor and is realized when both transistor input and output are simultaneously conjugate-matched to the source and load impedances, respectively. Although the power gain can be readily derived from the S-parameters of the transistor [20], the relationship between S-parameters and the transistor's physical parameters (such as $C_{\rm gs}$ and g_m) is often complicated and does not provide good insight into the gain-limiting mechanisms in a MOS transistor.

As shown in Fig. 6, by ignoring the gate–drain capacitance of the transistor (assuming unilaterality), a simple equation for maximum available power gain G_A can be derived.[2] By choosing source and load impedances as in Fig. 6 and setting $L_1 = 1/\left(C_{\rm gs}\omega^2\right)$ and $L_2 = 1/\left(C_{\rm ds}\omega^2\right)$, the reactive parts cancel and the input and output ports of transistor are conjugate matched. Therefore $V_{\rm gs} = V_s/(2jR_gC_{\rm gs}\omega)$ and the resulting (unilateral) power gain is

$$G_{AU} = \frac{\text{Output Available Power}}{\text{Source Available Power}} = \frac{g_m^2 R_{\rm ds}}{4\omega^2 R_g C_{\rm gs}^2} \approx \frac{R_{\rm ds}}{4R_g}\left(\frac{f_T}{f}\right)^2. \quad (1)$$

where

$$f_T = \frac{g_m}{2\pi C_{\rm gs}}.$$

The gain of a conjugate-matched FET drops off as $1/f^2$. To maximize the power gain, the gate resistance should be reduced by having smaller finger gate lengths and increasing number of fingers. However, in practice, the gate-drain capacitance, C_{gd}, cannot be ignored, as it is the source of feedback and can cause instability. A more detailed analysis shows that for small values of R_g the presence of feedback capacitor C_{gd} can make the amplifier unstable [21]. Hence, in order to have a stable amplifier with a conjugate-matched input and output, R_g should be large in which case the power gain of the transistor will be significantly reduced as per (1). This conflict can be resolved by using a cascode design for the amplifying stages.

[2]The ratio of the transducer power gain (G_T) and the unilateral power gain (G_{TU}) (calculated by ignoring C_{gd}) or G_T/G_{TU} is bounded by $(1/(1+U)^2) < (G_T/G_{TU}) < (1/(1-U)^2)$ where $U = ((|S_{12}||S_{21}||S_{11}||S_{22}|)/((1-|S_{11}|^2)(1-|S_{22}|^2)))$ is a metric for unilaterality [20].

TABLE I
SIMULATED AND MEASURED PARAMETERS OF THE TRANSMISSION LINE AT 24 GHZ, WITH WIDEBAND FITTING

Parameter	EM Simulation	Wideband model from Measurement Results
Attenuation constant (α)	0.5dB/mm	1dB/mm
Characteristic impedance (Z_0)	27.5Ω	27.5Ω
Effective relative permittivity ($\varepsilon_{r,\rm eff}$)	18.7	18

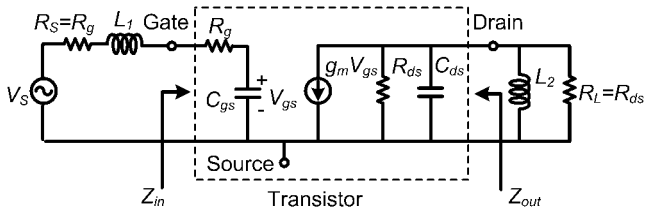

Fig. 6. Unilateral model of MOS transistor with conjugate-matched source and load terminations is used to calculate the maximum unilateral power gain.

D. Stability of the Cascode Amplifier

As discussed in the previous section, a single MOS transistor designed for maximum power gain in a common source configuration and conjugate matched at input and output can be unstable. At 24 GHz, this is true for the 0.18-μm CMOS transistors used in this design. The cascode structure makes the device more unilateral and hence unconditionally stable. Also, as the cascode pair has a higher drain–source breakdown voltage, a 2.8-V supply can be used for 0.18-μm devices that have a drain–source breakdown voltage of 2.5 V.

The output stage cascode pair is shown in more detail in Fig. 7(a). The gate of M_4 is self-biased by R_2 and bypassed by C_1. In [22], a self-biased cascode structure has been proposed in which the gate of the cascode device is not grounded at RF.

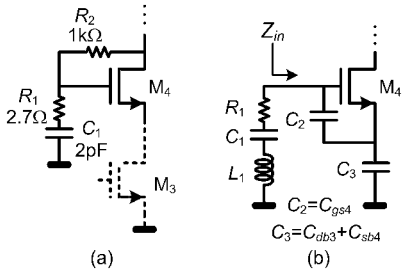

Fig. 7. (a) Self-bias of cascode transistor pair. (b) Equivalent circuit for the analysis of stability.

Although such a structure reduces the stress on the cascode transistor, the amplifier has a nonoptimal gain performance. Due to the limited gain at 24 GHz, the gate of the cascode device in this work was RF grounded with a large bypass capacitor C_1. Careful layout was carried out to minimize L_1, the parasitic series inductance of C_1. When L_1 is large, there remains a potential for high-frequency instability. A simple model for the circuit is shown in Fig. 7(b). Neglecting gate–drain capacitance of M_4, the impedance looking into gate of M_4 is

$$Z_{\text{in}} = \frac{1}{sC_2} + \frac{1}{sC_3} + \frac{g_m}{C_2C_3s^2}. \tag{2}$$

The real part of this impedance has a negative component equal to $-g_m/\left(C_2C_3\omega^2\right)$, indicating that the circuit can oscillate if there is a parasitic inductance between the gate and ground. By introducing the series resistance R_1 the circuit can be stabilized. The value of R_1 is chosen such that the amplifier remains stable for the largest estimated value of L_1. Using (2), the condition for the stability can be expressed as

$$R_1 > \frac{g_m}{C_2C_3\omega_{\text{osc}}^2} \tag{3}$$

$$\omega_{\text{osc}} = \frac{1}{\sqrt{L_1C_{\text{eq}}}}, \quad C_{\text{eq}} = \left(\frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_3}\right)^{-1}.$$

For parasitic inductances up to 100pH, by placing a 2.7 Ω series resistance the amplifier will be unconditionally stable.

E. Amplifier Design

The 24-GHz PA shown in Fig. 8 is a single-ended two-stage design that can directly feed a single-ended 50-Ω antenna, thereby making a Balun or a differential antenna unnecessary. If a differential antenna is available, two amplifiers in parallel can produce 3 dB higher output power similar to [23].

The PA is designed to operate in class AB mode. As the transistor $f_{\max}$ is 65 GHz, the harmonic content at the drain of the transistor for the 24-GHz input signal is low. Therefore harmonic-matching based classes such as class E and class F did not increase efficiency significantly.

To minimize the effect of gate series resistance, R_g, which can be the limiting factor for $f_{\max}$, the finger width of transistors was chosen to be 2 μm with gate contacts at both ends. This also allows substrate contacts to be placed closer to the device, minimizing substrate losses in transistor.

As shown in Fig. 8, the stages are designed such that all the phase shifts provided by transmission lines required for impedance matching are small. The output stage matching is designed to convert the 50 Ω antenna impedance to the proper impedance at the drain of M4, maximizing output power and efficiency. This proper impedance is chosen by the load pull simulations of the cascode pair when the gate of the input transistor is driven by a large-signal source. As shown in Fig. 9, T_s brings down the 50 Ω antenna impedance to achieve higher output power while T_p acts as a shorted-stub inductor to resonate drain-substrate capacitance of M4. Inter-stage matching is designed to achieve optimum impedance at the drain of the cascoded transistor, while input matching is designed to ensure good match for large input signal amplitudes.

For minimum passive loss, the output stage characteristic impedance should be lower than the interstage one, but to simplify the design and test procedures a single characteristic impedance of 27.5 Ω was used for the transmission lines across the chip. A weighted least-mean-square (LMS) optimization with gradient-descent scheme was used to choose this characteristic impedance and all of the transmission-line lengths. All 2-pF MIM capacitors used to short parallel stubs have a high width-to-length ratio to make the electrical length of the shorted stubs more accurate.

F. Low-Frequency Stability of the Amplifier

In addition to the stability analysis discussed in Section III-D, some additional measures have been taken to improve the low-frequency stability of the amplifier. In particular, as shown in Fig. 8, C_{G1} and C_{G3} coupling capacitors are shunted with a series *RC* network designed to introduce resistive loss at low frequencies while maintaining the necessary dc blocking.

The simulated Rollett stability factor [20] K of the amplifier was greater than 30 for all frequencies between dc and 65 GHz. This was done for all gate and drain biases. During measurements, there were no signs of oscillation with any bias condition, drive level, or wirebond inductance.

G. Wirebond and Pad Parasitic Effects

The amplifier is designed to accommodate a large range of wirebond inductances. The change in inductance is caused by variations in the length and curvature of the wirebond. Three-dimensional electromagnetic simulations for the intended test board reveal a range of 0.2–0.5 nH for the inductance, depending on different wirebond curvatures.

Capacitors are placed in series with the input and output pads to resonate out this inductance, as shown in Fig. 8. In the large-inductance mode (wirebond inductance greater than 0.4 nH), the voltage swing across the series capacitance can exceed the breakdown voltage of the MIM capacitors available in the process (∼5 V). A vertical parallel-plate (VPP) capacitor with a breakdown voltage in excess of 100 V is used to prevent capacitor breakdown [24].

The substrate shield of the transmission line structure is extended beneath the bondpads, making the bondpads part of the transmission line structure. Therefore, the pad capacitance no longer needs to be de-embedded or taken into account separately in the design. Furthermore, a large signal width of 60 μm ensures that no tapering is necessary to connect the pads into the structure, eliminating tapering discontinuities.

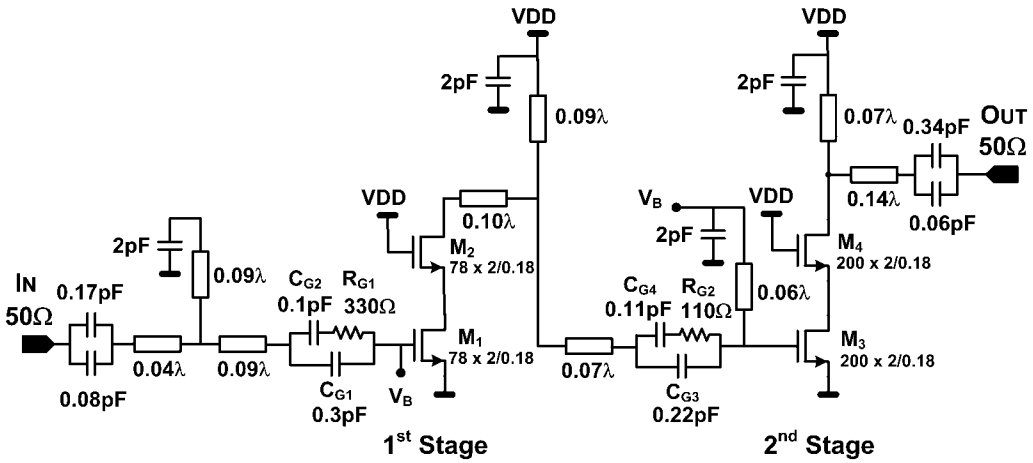

Fig. 8. Schematic of the 24-GHz, 14.5-dBm fully integrated CMOS PA.

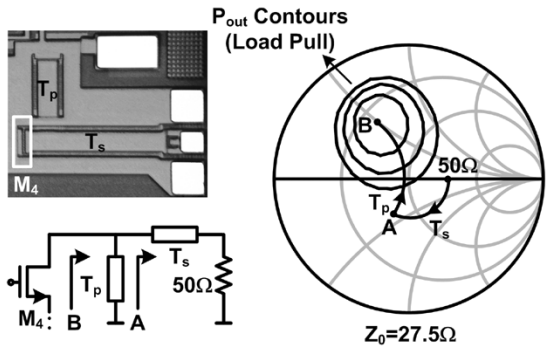

Fig. 9. Design of the output matching network; the Smith chart reference impedance is the characteristic impedance of the transmission lines (27.5 Ω).

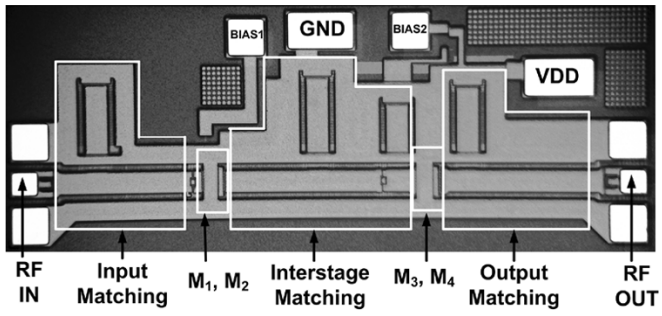

Fig. 10. Die microphotograph of the amplifier. Chip size: 0.7 mm × 1.8 mm.

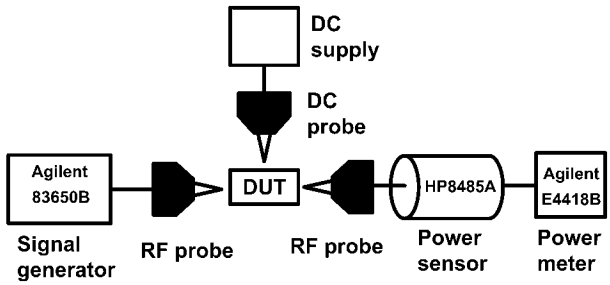

Fig. 11. Large-signal measurement setup.

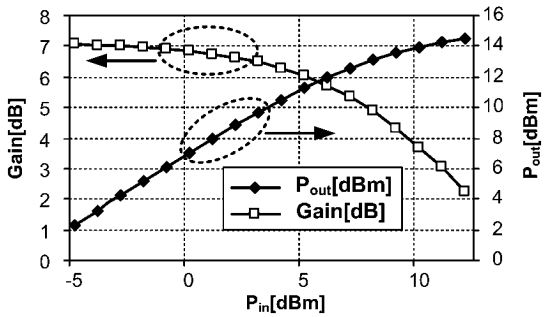

Fig. 12. Output power and amplifier gain versus available input power using a 2.8-V supply.

IV. Experimental Results

The PA was fabricated using 0.18-μm CMOS transistors in a process with a substrate resistivity of 10 $\Omega \cdot$ cm. As shown in Fig. 10, the chip occupies an area of 0.7 mm × 1.8 mm including pads. Quasi-3-D simulations were performed on the complete structure as a part of the design cycle to verify the amplifier's performance. In our measurement, the chip was attached to a gold-plated brass substrate using conductive epoxy to function as a heat sink and mechanical support.

Large-signal measurements were performed using the measurement setup shown in Fig. 11. The output is connected to a power meter with an Agilent HP8485A 26.5 GHz power sensor. The sensor attenuates all harmonic signal power and therefore eliminates the need for a harmonic filter. The power losses in the measurement setup are calibrated out with a thru measurement consisting of two cables and two probes connected in series. With similar cable and probes, loss of a cable/probe pair is half of the total series configuration.

As shown in Fig. 12, at 24 GHz the amplifier has a small-signal gain of 7 dB and can produce +14.5 dBm of output power, while drawing 100 mA from a 2.8 V supply. The corresponding peak drain efficiency is 11%. The output-referred 1 dB compression point is 11 dBm.

To test the linearity of the amplifier, a two-tone test was performed with a tone spacing of 100 MHz. As shown in Fig. 13, the output-referred third-order intercept point (OIP3) is 14 dBm. The measurement was limited by the maximum output power from one of the signal generators used to synthesize the two-tone signal. IMD asymmetries on the order of 10 dB were observed at low output powers. These asymmetries can be explained using a nonlinear dynamical model [25].

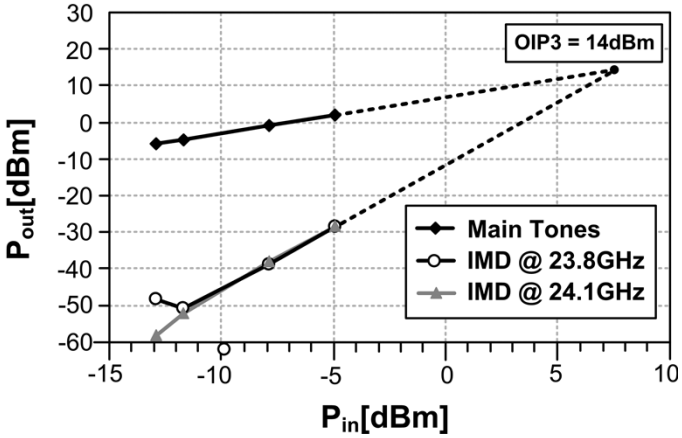

Fig. 13. Two-tone measurement of the amplifier; the two tones are applied at 23.9 and 24 GHz.

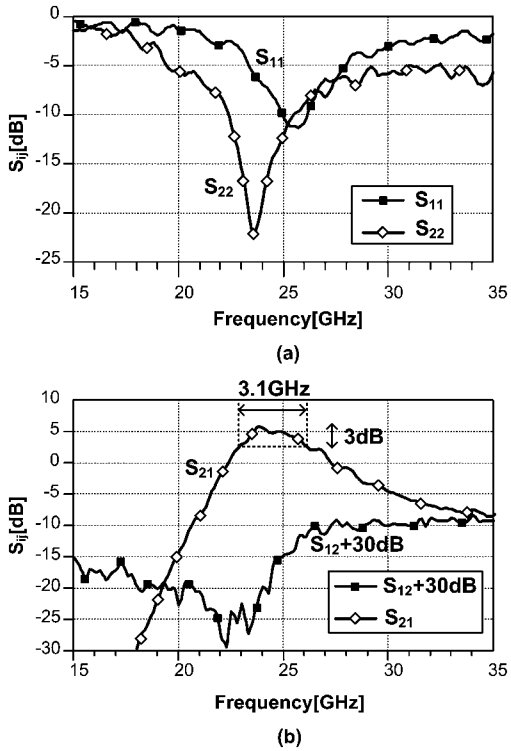

Fig. 14. Measured S-parameters of the amplifier, $V_{G1} = V_{G3} = 1$ V, $V_{DD} = 2.8$ V, and $I_{supply} = 100$ mA. (a) Reflection parameters. (b) Transmission parameters.

Small-signal measurements were also done using the Agilent E8364A 50-GHz network analyzer. A Thru-Reflection-Line (TRL) calibration was performed at the probe tips using CPW calibration standards on an Alumina substrate to measure the S-parameters of the amplifier, shown in Fig. 14. The 3-dB bandwidth is 3.1 GHz from 22.9 to 26 GHz, while the peak gain is at 23.9 GHz and the maximum S_{11} and S_{22} within the ISM band at 24–24.25 GHz are -6.9 and -16 dB, respectively. Measured S_{12} of the amplifier across the 15–35-GHz band is lower than -38 dB. The measured performance of the amplifier is summarized in Table II.

The measured gain of the amplifier using network analyzer and power meter has less than 1 dB difference. Part of this difference (0.3 dB) is due to the measurement uncertainty of the network analyzer at this frequency [26]. The uncertainty in the power meter measurement at this frequency is less than 0.1 dB.

TABLE II
MEASURED PERFORMANCE SUMMARY OF THE PA

Frequency	24GHz
Output 3rd-Order Intercept Point (OIP3)	14dBm
Peak PAE	6.5%
3dB bandwidth	3.1GHz
Small-Signal Gain	7dB
Max. S_{11} @ 24GHz ~ 24.25GHz	-6.9dB
Max. S_{22} @ 24GHz ~ 24.25GHz	-16dB
Max. S_{12} @ 15GHz ~ 35GHz	-40dB
Current Consumption @ 2.8V	100mA

V. CONCLUSION

A substrate-shielded CPW structure has been designed resulting in low passive loss and small impedance transformation network area. The structure enables the design of a fully integrated 24-GHz PA, using 0.18-μm MOSFETs, that is a key element in a integrated phased-array transmitter. This study shows that CMOS technology is a viable candidate for building fully integrated transceivers at frequencies above 20 GHz.

ACKNOWLEDGMENT

The authors would like to thank IBM for chip fabrication, as well as A. Babakhani, H. Hashemi, M. Morgan, E. Afshari, B. Analui, and N. Wadefalk of Caltech, A. Mirzaei of UCLA, and the anonymous reviewers for their assistance and feedback. The technical support for CAD tools from Agilent Technologies, Ansoft Corp., and Zeland Software, Inc., is also appreciated.

REFERENCES

[1] *Federal Communications Commission FCC 02-04*, Section 15.249.
[2] *Federal Communications Commission FCC 02-04*, Section 15.515.
[3] D. Lu, M. Kovacevic, J. Hacker, and D. Rutledge, "A 24 GHz active patch array with a power amplifier/low-noise amplifier in MMIC," *Int. J. Infrared Millimeter Waves*, vol. 23, pp. 693–704, May 2002.
[4] I. Gresham *et al.*, "Ultra wide band 24 GHz automotive radar front-end," in *IEEE MTT-S Int. Microwave Symp. Dig.*, Jun. 2003, pp. 369–372.
[5] E. Sonmez, A. Trasser, K.-B. Schad, P. Abele, and H. Schumacher, "A single-chip 24 GHz receiver front-end using a commercially available SiGe HBT foundry process," in *Proc. IEEE RFIC Symp.*, Jun. 2002, pp. 159–162.
[6] H. Hashemi, X. Guan, and A. Hajimiri, "A fully integrated 24 GHz 8-path phased-array receiver in silicon," in *ISSCC Dig. Tech. Papers*, vol. 47, Feb. 2004, pp. 390–39.
[7] X. Guan and A. Hajimiri, "A 24 GHz CMOS front-end," *IEEE J. Solid-State Circuits*, vol. 39, no. 2, pp. 368–373, Feb. 2004.
[8] H. Shigematsu, T. Hirose, F. Brewer, and M. Rodwell, "Millimeter-wave CMOS circuit design," *IEEE Trans. Microw. Theory Tech.*, vol. 53, no. 2, pp. 472–477, Feb. 2005.
[9] F. Ellinger, "26–42 GHz SOI CMOS low noise amplifier," *IEEE J. Solid-State Circuits*, vol. 39, no. 3, pp. 522–528, Mar. 2004.

[10] C. H. Doan, S. Emami, A. Niknejad, and R. W. Broderson, "Millimeter-wave CMOS design," *IEEE J. Solid-State Circuits*, vol. 40, no. 1, pp. 144–155, Jan. 2005.
[11] A. Natarajan, A. Komijani, and A. Hajimiri, "A 24 GHz phased-array transmitter in 0.18 μm CMOS," in *ISSCC Dig. Tech. Papers*, vol. 48, Feb. 2005, pp. 212–213.
[12] M. Racanelli and P. Kempf, "SiGe BiCMOS technology for communication products," in *Proc. Custom Integrated Circuits Conf.*, Sep. 2003, pp. 331–334.
[13] T. S. D. Cheng *et al.*, "On-chip interconnect for mm-wave applications using an all-copper technology and wavelength reduction," in *ISSCC Dig. Tech. Papers*, vol. 46, Feb. 2003, pp. 396–397.
[14] B. Kleveland, C. H. Diaz, D. Wook, L. Madden, T. H. Lee, and S. S. Wong, "Exploiting CMOS reverse interconnect scaling in multigigahertz amplifier and oscillator design," *IEEE J. Solid-State Circuits*, vol. 36, no. 10, pp. 1480–1488, Oct. 2001.
[15] L. Zhu, "Guided-wave characteristics of periodic coplanar waveguides with inductive loading: Unit-length transmission parameters," *IEEE Trans. Microw. Theory Tech.*, vol. 51, no. 10, pp. 2133–2138, Oct. 2003.
[16] High Frequency Structure Simulator. HFSS. [Online]. Available: http://www.ansoft.com
[17] MoM-Based Electromagnetic Simulator. IE3D. [Online]. Available: http://www.zeland.com
[18] A. Komijani and A. Hajimiri, "A 24 GHz, $+14.5$ dBm fully-integrated power amplifier in 0.18 mm CMOS," in *Proc. Custom Integrated Circuits Conf.*, Oct. 2004, pp. 561–564.
[19] Advanced Design System (ADS), TLINP: 2-Terminal Physical Transmission Line Model. [Online]. Available: http://eesof.tm.agilent.com/products/adsoview.html
[20] D. M. Pozar, *Microwave Engineering*, 2nd ed. New York: Wiley, 1998.
[21] A. Komijani, "Instability in a CMOS transistor," Caltech High-Speed IC group internal report.
[22] T. Sowlati and D. M. W. Leenaerts, "A 2.4 GHz 0.18 μmm CMOS self-biased cascode power amplifier," *IEEE J. Solid-State Circuits*, vol. 38, no. 8, pp. 1318–1324, Aug. 2003.
[23] B. Floyd, S. Reynolds, U. Pfeiffer, T. Zwick, T. Beukema, and B. Gaucher, "SiGe bipolar transceiver circuits operating at 60 GHz," *IEEE J. Solid-State Circuits*, vol. 40, no. 1, pp. 156–167, Jan. 2005.
[24] R. Aparicio and A. Hajimiri, "Capacity limits and matching properties of integrated capacitors," *IEEE J. Solid-State Circuits*, vol. 37, no. 3, pp. 384–393, Mar. 2002.
[25] N. B. Carvalho and J. C. Pedro, "Two-tone IMD asymmetry in microwave power amplifiers," in *IEEE Int. Microwave Symp. Dig.*, 2000, pp. 445–448.
[26] Agilent PNA Series Microwave Network Analyzers. [Online]. Available: http://cp.literature.agilent.com/litweb/pdf/5988-3992EN.pdf

Abbas Komijani (S'98) received the B.S. and M.S. degrees in electronics engineering from the Sharif University of Technology, Tehran, Iran, in 1995 and 1997, respectively. He is currently working toward the Ph.D. degree at the California Institute of Technology (Caltech), Pasadena.

He was a Senior Design Engineer with Emad Semiconductors, Tehran, Iran, where he worked on CMOS chipsets for voiceband applications from 1997 to 1999. He was a Design Engineer with Valence Semiconductors, Irvine, CA, where he worked on data converters for VoIP applications from 1999 to 2000. His research interests include high-frequency power amplifiers, wireless transceivers, phased array architectures, and delta-sigma data converters.

Mr. Komijani was the recipient of the Silver Medal in the National Mathematics Olympiad in 1991. He was also the recipient of the IEEE Custom Integrated Circuits Conference (CICC) 2004 Best Student Paper Award, the Caltech Atwood Fellowship in 2000, and the Analog Devices Outstanding Student Designer Award in 2005.

Arun Natarajan (S'02) received the B.Tech. degree from the Indian Institute of Technology, Madras, in electrical engineering and the M.S. degree from the California Institute of Technology (Caltech), Pasadena, in 2001 and 2003, respectively. He is currently working toward the Ph.D. degree at Caltech.

He was a Design Engineer at the IBM T. J. Watson Research Center, Yorktown Heights, NY, in the summer of 2005, where he worked on integrated circuits for high-frequency wireless receivers. His research interests include design of integrated high-frequency circuits, wireless transceivers, and modeling of parasitic coupling in integrated circuits.

Mr. Natarajan received the Caltech Atwood Fellowship in 2001, the Analog Devices Outstanding Student IC Designer Award in 2004, and the IBM Research Fellowship in 2005.

Ali Hajimiri (S'95–M'99) received the B.S. degree in electronics engineering from the Sharif University of Technology, Tehran, Iran, and the M.S. and Ph.D. degrees in electrical engineering from Stanford University, Stanford, CA, in 1996 and 1998, respectively.

He was a Design Engineer with Philips Semiconductors, Sunnyvale, CA, where he was involved with a BiCMOS chipset for GSM and cellular units from 1993 to 1994. In 1995, he was with Sun Microsystems, where he worked on the UltraSPARC microprocessor's cache RAM design methodology. During the summer of 1997, he was with Lucent Technologies, Bell Laboratories, Murray Hill, NJ, where he investigated low-phase-noise integrated oscillators. In 1998, he joined the Faculty of the California Institute of Technology (Caltech), Pasadena, where he is an Associate Professor of Electrical Engineering and the Director of Microelectronics and Noise Laboratories. His research interests are high-speed and RF integrated circuits. He is a coauthor of *The Design of Low Noise Oscillators* (Boston, MA: Kluwer, 1999) and holds several U.S. and European patents. He is a cofounder of Axiom Microdevices, Inc., Irvine, CA.

Dr. Hajimiri is an Associate Editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS (JSSC) and a member of the Technical Program Committee of the International Solid-State Circuits Conference (ISSCC). He has also served as an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS (TCAS): Part II, a member of the Technical Program Committees of the International Conference on Computer Aided Design (ICCAD), Guest Editor of the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES, and a member of the Guest Editorial Board of the *Transactions of Institute of Electronics, Information and Communication Engineers of Japan* (IEICE). He is on the Top 100 Innovators (TR100) list. He was the recipient of the Gold Medal of the National Physics Competition and the Bronze Medal of the 21st International Physics Olympiad, Groningen, Netherlands. He was a corecipient of the International Solid-State Circuits Conference (ISSCC) 1998 Jack Kilby Outstanding Paper Award and a three-times recipient of the IBM Faculty Partnership Award as well as the National Science Foundation CAREER award.