A 25-MHz Self-Referenced Solid-State Frequency Source Suitable for XO-Replacement

Michael S. McCorquodale, *Member, IEEE*, Gordon A. Carichner, *Member, IEEE*, Justin D. O'Day, Scott M. Pernia, *Member, IEEE*, Sundus Kubba, Eric D. Marsman, *Member, IEEE*, Jonathan J. Kuhn, and Richard B. Brown, *Senior Member, IEEE*

***Abstract*—Recent trends in the development of integrated silicon frequency sources are discussed. Within that context, a 25-MHz self-referenced solid-state frequency source is presented and demonstrated where measured performance makes it suitable for replacement of crystal oscillators (XOs) in data interface applications. The frequency source is referenced to a frequency-trimmed and temperature-compensated 800-MHz free-running LC oscillator (LCO) that is implemented in a standard logic CMOS process and with no specialized analog process options. Mechanisms giving rise to frequency drift in integrated LCOs are discussed and supported by analytical expressions. Design objectives and a compensation technique are presented where several implementation challenges are uncovered. Fabricated in a 0.25-μm 1P5M CMOS process, and with no external components, the prototype frequency source dissipates 59.4 mW while maintaining ± 152 ppm frequency inaccuracy over process, $\pm 10\%$ variation in the power supply voltage, and from $-10\,^{\circ}$C to 80 °C. Variation against other environmental factors is also presented. Nominal period jitter and power-on start-up latency are 2.75 $\mathrm{ps_{rms}}$ and 268 μs, respectively. These performance metrics are compared with an XO at the same frequency.**

***Index Terms*—Clocks, CMOSFET oscillators, piezoelectric resonator oscillators, voltage-controlled oscillators (VCOs).**

I. Introduction

AS EARLY as 1968, the concept of a self-referenced silicon frequency references was explored, when a temperature-compensated Wien-type *RC* oscillator (RCO) was demonstrated [1]. The motivation has been to eliminate macroscopic piezoelectric quartz crystal (XTAL) or ceramic frequency references in microelectronic systems to reduce component count, form-factor, and cost while increasing reliability.

The challenge has been to achieve sufficiently high frequency stability and accuracy over variations in process, voltage, and temperature (PVT) along with other environmental variables.

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M. S. McCorquodale, G. A. Carichner, J. D. O'Day, S. M. Pernia, E. D. Marsman, and J. J. Kuhn are with Mobius Microsystems, Ann Arbor, MI 48108 USA (e-mail: mccorquodale@mobiusmicro.com; carichner@mobiusmicro.com; oday@mobiusmicro.com; pernia@mobiusmicro.com; marsman@mobiusmicro.com; kuhn@mobiusmicro.com).

S. Kubba was with Mobius Microsystems, Design Center, Detroit, MI 48226 USA. She is now with the University of Michigan, Ross School of Business, Ann Arbor, MI 48109 USA (e-mail: skubba@umich.edu).

R. B. Brown is with the University of Utah, Salt Lake City, UT 84112 USA (e-mail: brown@utah.edu).

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In [1], the frequency inaccuracy due to temperature alone was over 2%, while in several recent efforts, including [2] and [3], similar results were obtained. In [3], a 7-MHz compensated ring oscillator was reported to achieve 2.6% total frequency inaccuracy over PVT without frequency trimming. Monolithic temperature-compensated relaxation oscillators have been explored in [4] and [5], where the reported total frequency inaccuracy was in excess of 2% over voltage and temperature. None of these approaches have achieved sufficient frequency accuracy to become a viable frequency source for most applications. Further, the short-term frequency stability, specifically phase noise and jitter, has not been explored in most of this prior work.

In contrast, XTALs possess an intrinsically high quality (Q) factor that exhibits an inverse-square relationship with phase noise [6]. Further, XTALs achieve a very low-frequency temperature coefficient f_{TC} if cut at the appropriate lattice angle (e.g., AT). Typical f_{TC} for an AT-cut XTAL is below ± 50 ppm over a range of 125 °C. For these reasons, XTAL oscillators (XOs) have served as frequency references in electronic platforms since as early as 1919 [7]. In particular, bulk acoustic wave (BAW) XTALs have become the *de facto* frequency source. However, it is difficult to reliably manufacture fundamental-mode BAW XTALs above approximately 50 MHz. Thus, single-frequency XOs from approximately 1 to 50 MHz typically serve as the reference frequency source for channel-rate and multiclock-domain phase-locked loops (PLLs) where synthesized frequencies span a bandwidth from the low megahertz to over 1 GHz. This is particularly common for data interface protocols such as USB, S-ATA, and 10/100/1000 Ethernet (IEEE 802.3), where the reference clock rates are commonly 12, 40, and 25 MHz, respectively, while the channel rates are 480 MHz for HS-USB [8], 3 GHz for S-ATA Gen. 2 [9], and up to 1 Gbps for Ethernet [10].

The limitations of XTALs have spawned exploration into the development of MEMS technology for frequency synthesis. In 1967, the resonant gate transistor was presented as a micromachined integrated frequency source [11]. Since then, and particularly recently, there has been a plethora of academic reports on silicon MEMS microresonators for frequency synthesis, including [12]–[19]. Further, nanoscale resonators are now being explored such as those in [20]. However, several challenges have been encountered in the development of these microresonator oscillators (MROs), including high motional impedance [13], limited power handling [14], large f_{TC} [15], and frequency variation across the wafer. Recent work has aimed to overcome these challenges, including the temperature compensation work in [15], and many challenges have been addressed or contained.

Consequently, literature associated with the successful commercialization of MROs has appeared recently from industry, including, for example, [21]–[24].

The work presented herein has been motivated by the same objectives as the former. Further, in this work, it is noted that many applications have frequency accuracy requirements that are not as tight as ± 50 ppm. For example, data interface protocols, such as HS-USB, S-ATA, and 10/100/1000 Ethernet, require the reference frequency source to maintain an accuracy of ± 500 [8], ± 350 [9] and ± 100 ppm, respectively [10]. Next, and referring to the historical literature, this work has been inspired in part by the work in [25], where techniques to develop precise and environmentally stable LC vacuum tube oscillators were reported in 1964. However, in contrast to [25], an opportunity to reinvestigate the viability of self-referenced solid-state oscillators has emerged recently with the advent of RF CMOS in the 1990s and the related availability of high-Q inductors and devices with low flicker noise [26]. Furthermore, this work is differentiated by the application of the principles in [25] to integrated LC oscillators (LCOs).

Considering these motivations collectively, the authors have reported recently on frequency-trimmed and temperature-compensated solid-state LCOs as self-reference frequency sources in [27]–[32]. It was shown in [27] that RF LCOs could serve as low-jitter self-referenced frequency sources by exploiting the effects of frequency division from RF to typical fundamental-mode BAW XTAL frequencies (i.e., 1–50 MHz, as described previously). Further, the low far-from-carrier (FFC) phase noise intrinsic to LCOs enables low period jitter. In [27], it was shown that such an approach enables solid-state frequency sources to be realized with period jitter as low as XOs despite the substantial difference in Q-factor between LC and XTAL resonators.

In [28], a discrete self-referenced LCO frequency source was reported by the authors where the total untrimmed frequency inaccuracy over PVT was less than $\pm 1\%$, including $\pm 10\%$ variation in the power supply and over 70 °C. Subsequent work focused on achieving higher frequency accuracy. In [29], an embedded, self-referenced, trimmed, and compensated LCO was demonstrated in an HS-USB PHY where ± 400-ppm frequency accuracy was achieved over PVT including $\pm 10\%$ variation in the power supply and over 95 °C. In [30], a discrete LCO frequency source was demonstrated where sub-± 100-ppm frequency inaccuracy was achieved over PVT. In [31], the performance of the device in [30] was compared with both XOs and MROs. The LCO-referenced frequency source was shown to achieve over six times lower period jitter than commercial MROs while maintaining frequency accuracy comparable to both MROs and XOs.

This study reports the details of the discrete LCO-referenced solid-state frequency source presented in [32]. In contrast to the work in [27]–[32], a detailed discussion of the mechanisms which give rise to frequency drift in integrated LCOs is presented where useful relationships are derived and/or bounded. Design objectives for developing accurate self-referenced solid-state oscillators are presented by employing these relationships. Furthermore, this work is delineated from that in [29]. First, the frequency-trimming and temperature-compensation resolution in this work marks a 20-fold advance over that in [29].

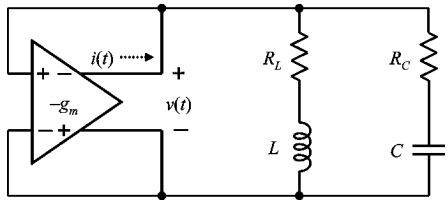


Fig. 1. Schematic of a generalized LCO including the transconductor and the coil and capacitor losses, R_L and R_C, respectively.

Second, the net f_{TC} achieved in this work is less than one half of that in [29]. Third, the complete measurement results for the frequency-trimming and temperature-compensation analog circuitry are presented, where several challenges are uncovered. Fourth, preliminary data from other environmental influences on frequency are presented including load- and moisture-induced frequency drift as well as aging. Finally, measurements from frequency-trimmed and temperature-compensated devices are compared directly with a 25-MHz commercial-off-the-shelf (COTS) XO.

II. LCO Background and Theory

A. Temperature- and Bias-Induced Frequency Drift

The natural resonant frequency of an LC tank is given by $\omega_o = \sqrt{LC}^{-1}$, where L is the net tank inductance and C is the net tank capacitance. Referring to Fig. 1, both the coil and the capacitor exhibit finite losses, denoted by R_L and R_C, respectively. Considering these losses, the oscillation frequency is given by the zero-phase solution to the network

$$\omega_1 = \omega_o \sqrt{\frac{L - \mathrm{CR}_L^2}{L - \mathrm{CR}_C^2}}. \tag{1}$$

The actual resonant frequency depends on the sustaining transconductance amplifier which is required to overcome the loss in the tank. The transconductance amplifier injects a current $i(t)$ with high harmonic content into the LC network. The capacitor absorbs the majority of this sustaining current because the inductor current cannot change instantaneously. Consequently, there exists an imbalance in the work done in the capacitor and the inductor. This harmonic work imbalance (HWI) is reconciled by depressing the oscillation frequency.

The closed-form solution for the frequency including the effects of HWI has been determined via a method of reactive power balance of harmonics [25] and is given by

$$\omega = \omega_1 \left(1 - \frac{1}{2Q^2} \sum_{n=2}^{\infty} \frac{n^2}{n^2 - 1} h_{i(n)}^2\right) = \omega_1 (1 - \varepsilon) \tag{2}$$

where $Q = \omega_o L/(R_L + R_C), h_{i(n)} = I_n/I_1$, where I_n is the nth Fourier coefficient of $i(t)$ and ε represents the net fractional frequency deflection due to HWI. The term ε can be bounded. Consider the limiting case where the transconductor delivers $i(t)$ as a square wave and I_n is given by

$$I_n = \frac{1}{T} \int_0^T i(t) \sin\left(\frac{2\pi n t}{T}\right) dt = \frac{4}{\pi n} \tag{3}$$

for all odd n where T is the period of the oscillation. By substitution, $\max(h_{i(n)}) = 1/n$ for all odd n (and 0 otherwise), thus

$$\lim_{h_{i(n)} \to 1/n} \varepsilon = \frac{1}{2Q^2} \sum_{n \in \{3,5,\ldots\}}^{\infty} \frac{1}{n^2 - 1} = \frac{1/4}{2Q^2} = \varepsilon_{\max} \quad (4)$$

where $\varepsilon_{\max}$ is the asymptotic bound of frequency deflection due to HWI. From (4), as $Q \to \infty$, $\varepsilon_{\max} \to 0$. Consequently, high-Q oscillators are much less sensitive to HWI than lower Q oscillators, such as LCOs.

The natural frequency and (1) and (2) are the *only* expressions that govern the noise-free oscillation frequency. It has been shown that colored noise in oscillators can induce a frequency perturbation in [33], but mitigation of these effects is considered only within the generalized notion of low-noise analog circuit design. Thus, frequency drift can originate only through modulation of one or more of the following:

1) net tank inductance, L, or capacitance, C;
2) net loss in the net tank inductance or capacitance, R_L or R_C, respectively;
3) harmonic content of $i(t)$.

The net tank inductance is determined nearly exclusively by the coil. Furthermore, it has been shown that integrated inductors exhibit a low temperature coefficient (TC) [34]. Thus, the net tank inductance varies little unless the field lines are modulated by a change in magnetic permeability or an eddy current is induced in a conductive material in close proximity to the coil. The net tank capacitance is largely determined by the designed capacitance, but a substantial portion originates from the transconductor and fringing capacitance from interconnect. Integrated thin-film capacitors exhibit relatively low TCs, of the order of -50 ppm/°C [35]. However, in CMOS, the transconductor presents an inversion-mode MOS (I-MOS) capacitor to the tank, and it exhibits a nonnegligible TC [36] and bias sensitivity. Thus, a portion of the net tank capacitance contributes to the $f_{\rm TC}$ of the LCO. This sensitivity arises from the I-MOS c–v response of the transconductor devices. In the transition region of the c–v response, these devices exhibit a high TC. As the devices are biased away from this region, the TC decreases significantly. Though dependent on transconductor topology, $f_{\rm TC}$ generally decreases as bias current in the LCO increases because the devices are biased away from this transition region.

Typically, the coil loss is substantially larger than the loss in the capacitor, so (1) can be approximated by $\omega_1 \approx \omega_o\sqrt{1 - CR_L^2/L}$. The coil loss is a real resistive loss and exhibits a TC dependent on the material species. Ignoring the TC due to the I-MOS capacitance in the transconductor, the temperature-dependent frequency can be approximated by

$$\omega_1(T) \approx \omega_o\sqrt{1 - CR_L^2(T)/L} \quad (5)$$

where T is temperature and $R_L(T)$ exhibits a nearly linear positive TC for any metal species. The $f_{\rm TC}$ is then given by

$$f_{\rm TC} = \frac{1}{\omega_1}\frac{\partial \omega_1}{\partial T} = -\frac{CR_L}{L}\left(\frac{\omega_o}{\omega_1}\right)^2 \frac{\partial R_L}{\partial T}. \quad (6)$$

$f_{\rm TC}$ is temperature-dependent and (6) exhibits a concave-down, negative TC which increases in sensitivity at high temperatures because the ratio ω_o/ω_1 diverges. For an LCO at 1 GHz with $L = 4$ nH, $C = 6.33$ pF, $R_L(25\ ^\circ\text{C}) = 5\ \Omega$ and $\partial R_L/\partial T = 0.004$ (i.e., aluminum) the intrinsic $f_{\rm TC}$ is -33 ppm/°C. In practice, $f_{\rm TC}$ is larger due to the TC of the transconductor capacitance. Finally, the expression (5) can be written as a function of the inductor quality factor such that $\omega_1(T) \approx \omega_o\sqrt{1 - Q^{-2}}$. Thus, (6) becomes

$$f_{\rm TC} = \frac{1}{\omega_1}\frac{\partial \omega_1}{\partial T} = -\frac{1}{Q^2 R_L}\left(\frac{\omega_o}{\omega_1}\right)^2 \frac{\partial R_L}{\partial T} \quad (7)$$

and $f_{\rm TC}$ decreases with the inverse of Q^2.

The harmonic content of $i(t)$ is subject to changes in the transconductor. These changes can originate from a decrease in headroom through variation in the power supply and effects which modulate the transconductance gain including variation in the bias current and temperature. For a CMOS transconductor, the device transconductance g_m is proportional to $\mu^{1/2}$ and μ is proportional to $T^{-3/2}$, where μ is carrier mobility and T is temperature. As T increases, μ and g_m decrease. By (2), HWI will exhibit a positive $f_{\rm TC}$ which, to a limited extent, serves to cancel the negative $f_{\rm TC}$ due to the coil loss. However, this effect is typically comparatively small.

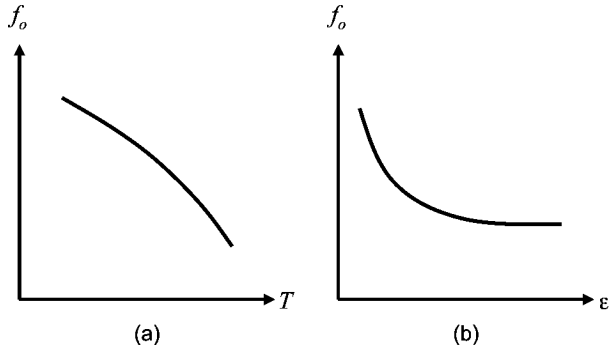


Fig. 2. (a) Theoretical native $f_{\rm TC}$ of an LCO exhibiting a negative concave-down response. (b) Theoretical native frequency drift due to HWI in an LCO exhibiting asymptotic saturation.

Fig. 2 illustrates the expected frequency drift behavior against temperature and HWI. Considering these effects, the following objectives reduce these native drift mechanisms.

1) The transconductor should be designed to achieve start-up over all operating conditions. However, start-up should be achieved at minimum device size to avoid modulation of the net tank capacitance through the TC and bias-dependence of the devices comprising the transconductor.
2) Considering (6), R_L should be minimized via process (e.g., metal thickness or species) and inductor design (e.g., by minimizing the coil loss). Though increasing L reduces $f_{\rm TC}$, it also increases R_L. Further, for a fixed frequency, decreasing C will reduce $f_{\rm TC}$, but a corresponding decrease in L will be required to achieve the same frequency, yielding the same $f_{\rm TC}$.
3) Considering (2), the LCO should be biased such that the harmonic content of $i(t)$ does not change or it should be biased toward the asymptote such that the harmonic content is always maximized. The latter strategy comes with a clear power penalty. The former can be achieved with

a filtering technique [25] or, to a limited extent, through power supply regulation and supply-independent biasing. For example, amplitude control can be employed to limit harmonic content as shown in [37]. However, the native TC through device carrier mobility will remain.

Once these techniques have been employed, the LCO will still exhibit a native negative f_{TC}. Thus, a compensating technique is required. A method of reactive compensation can be employed in which a varactor is modulated against temperature to cancel this native f_{TC}. With this approach, (5) can be rewritten as (8), shown at the bottom of the page, where C_f is a fixed capacitance, C_v is a variable capacitance, and v_{ctrl} is a temperature-dependent voltage. This temperature compensation technique was first presented by the authors in [29] and is advanced herein.

B. Q-Factor and Start-Up Latency

In many applications, it is desirable to *cold-start* frequency sources with low start-up latency to minimize idle power consumption. LCOs exhibit very low start-up latency as compared to XOs or MROs. The start-up envelope for any harmonic oscillator is given by

$$\frac{V_n}{V_o} = 1 - e^{\frac{-n\pi}{Q}} \tag{9}$$

where V_n is the amplitude of the nth cycle and V_o is the final steady-state amplitude. Rearranging and substituting $n = t/T_o$ yields

$$t = -\frac{Q}{\pi} \ln\left(1 - \frac{V_n}{V_o}\right) T_o. \tag{10}$$

Using (9), $t = nT_o$ and assuming a component Q of 10, 10 cycles are required for the oscillation amplitude to reach 95% of the steady-state level. For a reference oscillator at 1 GHz, the start-up latency is 7 ns. In contrast, an XO at 10 MHz with a Q of 10 000 requires over 9.5 kcycles to reach 95% of the steady-state level which corresponds to nearly 1 ms start-up latency. Practical circuits are limited by bias start-up latency, which can be of the order of μs or more. Despite that, the lower Q LC reference will exhibit a substantial reduction in start-up latency when compared with an XO at the same frequency, as will be demonstrated.

C. Phase Noise and Period Jitter

In [6] it was shown that Q exhibits an inverse-square relationship with phase noise. Consequently, it is expected that the close-to-carrier (CTC) phase noise of the LCO will be substantially higher than for a comparable XO. This makes the LCO poorly suited to RF applications due to concern over reciprocal mixing and the associated degradation in receiver sensitivity [38].

However, it has been shown in [31], [39], and [40] that the relationship between phase noise and period jitter is given by

$$\sigma_{\mathrm{rms}} = \sqrt{\frac{8}{\omega_o^2} \int_0^\infty S_\varphi(f_m) h(f_m) \sin^2(\pi f_m T_o) df_m} \tag{11}$$

where ω_o is the oscillation frequency, $S_\varphi(f_m)$ is the single sideband (SSB) phase noise power spectral density (PSD) at frequency offset f_m from the carrier frequency, $h(f_m)$ is the transfer function of the system with equivalent cut-off frequency f_h, and $T_o = 2\pi/\omega_o$. As shown in [27] and [31], the trigonometric function in (11) serves to mask the CTC phase noise and amplify the FFC phase noise. Both LCOs and XOs will exhibit similar FFC phase noise. Consequently, period jitter is expected to be comparable between an LCO and XO despite the large difference in Q. This observation motivated the original work in [27] and suggests that LCOs may be suitable frequency sources for data interface applications where period jitter leads to eye-closure and ultimately increased BER [31]. However, because the CTC phase noise in the LCO remains much higher than in a comparable XO, the approach presented here is not suited to RF applications.

D. Implementation and Design Challenges

Analog frequency-trimming and temperature-compensation techniques can be employed to counteract process variation and the intrinsic frequency drift of the LCO respectively. Neither is trivial. The center frequency of an LCO may vary by up to $\pm 5\%$ due to process variation, though trimming to 100 ppm or higher accuracy is desired. Thus, linear frequency trimming in 100 ppm steps or less for up to $\pm 10\%$ is desired. It is possible to accomplish this with a switched-capacitor array, as shown in [29] and [30]. However, not only is a monotonic response required, but the change in capacitance between each code is on the order of fractions of femtofarads. Further, some form of automatic test circuitry is required for rapid trimming of the nominal frequency. Such a technique was first presented in [29], but this work presents more than a 20-fold improvement in trimming resolution. Finally, once the nominal frequency is trimmed, the compensating TC must be determined. In this study, the authors take an exhaustive approach to exploring the compensation design space.

III. Solid-State Frequency Source Architecture

The reference oscillator is shown in Fig. 3, where the topology is cross-coupled and complementary. The target center frequency is 800 MHz, thus enabling division by 32 to generate 25 MHz, which is a typical reference frequency for Ethernet and similar protocols. The aspect ratios of the devices comprising the transconductor were purposely oversized such

$$\omega(T) = \sqrt{\frac{1}{L(C_f + C_v(v_{\mathrm{ctrl}}))} \left(1 - \frac{C_f R_L^2(T) + C_v(v_{\mathrm{ctrl}}) R_L^2(T)}{L}\right)} \tag{8}$$

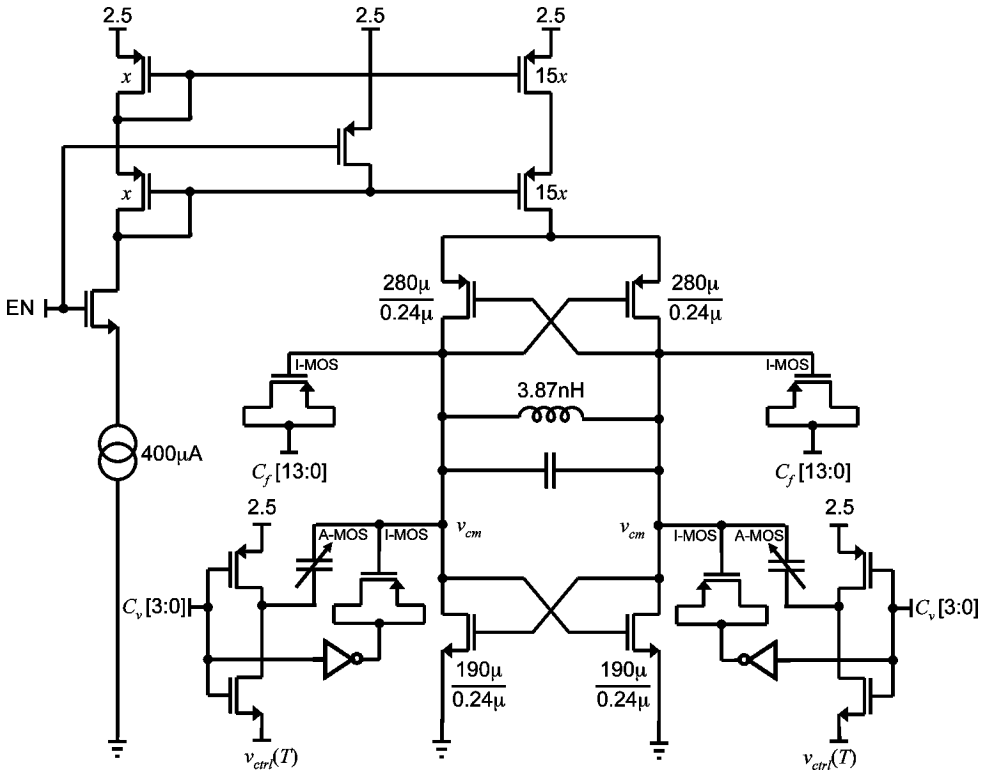


Fig. 3. 800-MHz reference oscillator. The I-MOS varactors serve to trim the nominal frequency. The accumulation-mode (A-MOS) varactors provide temperature-compensation when switched to $v_{\rm ctrl}(T)$. Disabled varactors are switched to the power supply.

that start-up could be achieved over PVT. In future revisions, device size could scale by 50% or more, thus reducing the contribution that the transconductor makes to $f_{\rm TC}$.

The coil is a 3.5-turn device with inner and outer radii of 72 and 142 μm, respectively. It is constructed of a stack of the last metal and the previous metal layer, both of which are 1 μm thick and 15 μm wide. Using a field solver, the series loss and component Q were determined to be 5 Ω and 3.9, respectively, the latter of which is low due to the lack of a thick last metal option and the selected resonant frequency. Q would be increased at higher frequencies, but possibly with a power penalty.

The LCO is biased via a programmable temperature-independent current through a cascode mirror. Eight bias levels are available. A 14-b binary-weighted programmable array of p-type I-MOS varactors serve as C_f in (8) and serve to trim the nominal frequency. The voltage on the backgate $(v_{\rm bg})$ of these varactors is biased by the bit-line. Fig. 4(a) illustrates the bias-dependent response of these devices. When the bit-line is high, the minimum capacitance is realized and vice versa. Δv represents the voltage across the device. The array is designed to realize -20 ppm frequency steps between codes. This technique was employed to realize the design in a logic CMOS process. However, the I-MOS capacitors contribute bias- and temperature-induced frequency drift.

Temperature compensation is achieved with a programmable 4-b binary-weighted array of accumulation-mode pMOS (A-MOS) varactors which serve as C_v in (8) and exhibit the response shown in Fig. 4(b). The varactor is disabled by biasing its back-gate to the power supply, which minimizes its capacitance, and switching in an I-MOS varactor to maintain

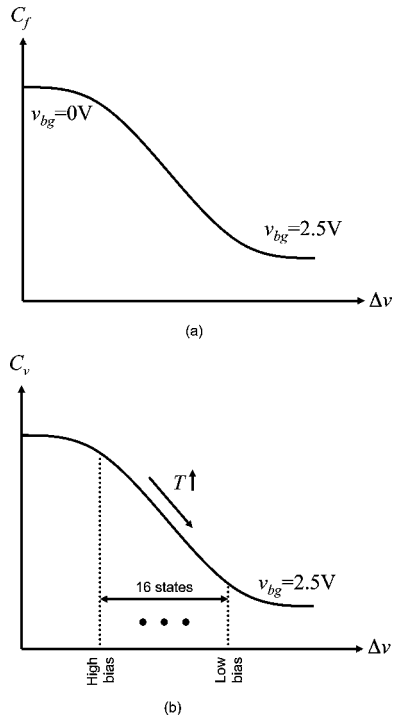


Fig. 4. Varactor $c-v$ responses. (a) Fixed I-MOS capacitor array, C_f, for frequency-trimming. (b) Variable A-MOS capacitors, C_v, to compensate $f_{\rm TC}$.

the net tank capacitance. Conversely, the varactor is activated by switching its backgate to the temperature-dependent compensating voltage $v_{\rm ctrl}(T)$, which is proportional to absolute temperature. As $v_{\rm ctrl}(T)$ increases, C_v decreases as shown,

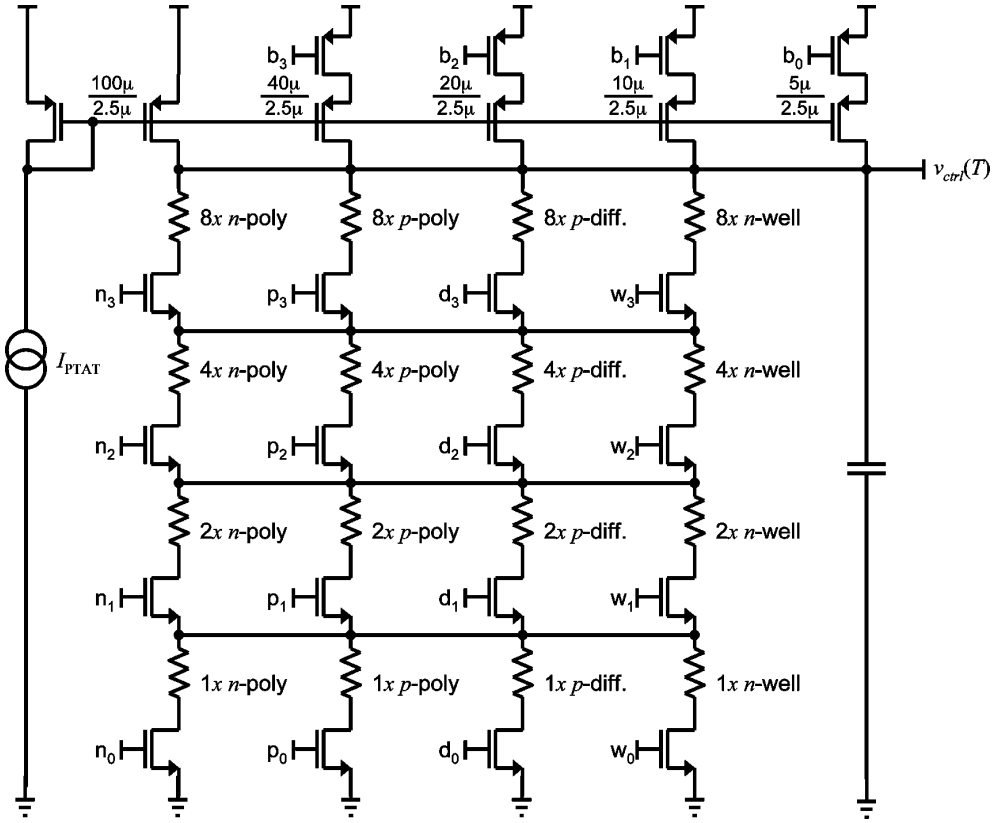


Fig. 5. Architecture of the temperature-dependent compensating voltage $v_{\rm ctrl}(T)$. The unit resistor size is 1.36 kΩ. The network enables both the TC and the level of $v_{\rm ctrl}$ to be programmed.

thus increasing the oscillation frequency and compensating for the native negative $f_{\rm TC}$. Considering phase noise up-conversion, certainly better topologies exist for the varactor, as demonstrated in [41]. However, this single-ended topology was selected for its flexibility and simplicity in deriving the temperature-compensating voltage. Considering $f_{\rm TC}$, this topology also contributes to temperature-induced frequency drift. For a fixed bias current, the common-mode voltage rises against temperature because it is set by the nMOS devices in the cross-coupled pair. That rise counters the effect of $v_{\rm ctrl}(T)$. Thus, the temperature-slope of $v_{\rm ctrl}(T)$ must be increased further.

The temperature-dependent control voltage $v_{\rm ctrl}(T)$ is derived by sourcing a ΔV_{BE} junction-referenced PTAT current source into a programmable array of resistors, as shown in Fig. 5. The four different resistor species exhibit increasing TCs and include n-type poly-Si, p-type poly-Si, p-type diffusion, and n-type well. The poly-Si resistors do not include silicide to maximize sheet resistance and minimize physical area. The network in Fig. 5 enables the TC of $v_{\rm ctrl}$ to be programmed by combining any combination of the binary-weighted resistors where the unit resistor size x is 1.36 kΩ. Further, the level of $v_{\rm ctrl}$ can be programmed via the binary-weighted current mirrors atop the structure. Due to process variation, the $v_{\rm ctrl}$ signal must be centered in the c–v response, as illustrated in Fig. 4(b).

The chip architecture is shown in Fig. 6. A bandgap-referenced and load-compensated low drop-out (LDO) regulator steps 3.3 V to the 2.5-V core voltage. The requirements for the LDO are very loose as its primary purpose is to limit supply variation which would induce frequency drift due to HWI.

The output of the LCO is frequency-divided first by a current-mode logic stage including a level shifter, CML divider and CML-to-CMOS converter. The remaining divide-by-16 is implemented with asynchronous CMOS-level flip-flops. Certainly, in an integrated, or SoC, implementation, this frequency division would not be necessary. In fact, the channel-rate frequencies could be derived directly from the LCO. However, the purpose of this work is to demonstrate a device that is functionally equivalent to BAW XOs and present a comparison of performance. The possibility of directly generating the channel-rate frequency without a PLL would clearly be interesting to explore.

Trimming coefficients for the LDO, bias currents $v_{\rm ctrl}$ and the fixed and variable capacitors are stored in an 88-b multi-time programmable (MTP) NVM. Custom logic was synthesized to support the NVM interface, a simple serial communication interface, and a digital frequency-locked loop (FLL) for automatic nominal frequency calibration.

The FLL implementation has been demonstrated in [29] and resembles the calibration technique for VCOs presented in [42]. The FLL determines the trimming coefficient for the I-MOS capacitor array which centers the LCO frequency by counting deep races between the LCO and a precision off-chip oven-controlled crystal oscillator (OCXO) such that the frequency discrepancy can be resolved. Once the FLL converges (typically within 100 ms), the coefficient is stored in NVM, loaded upon

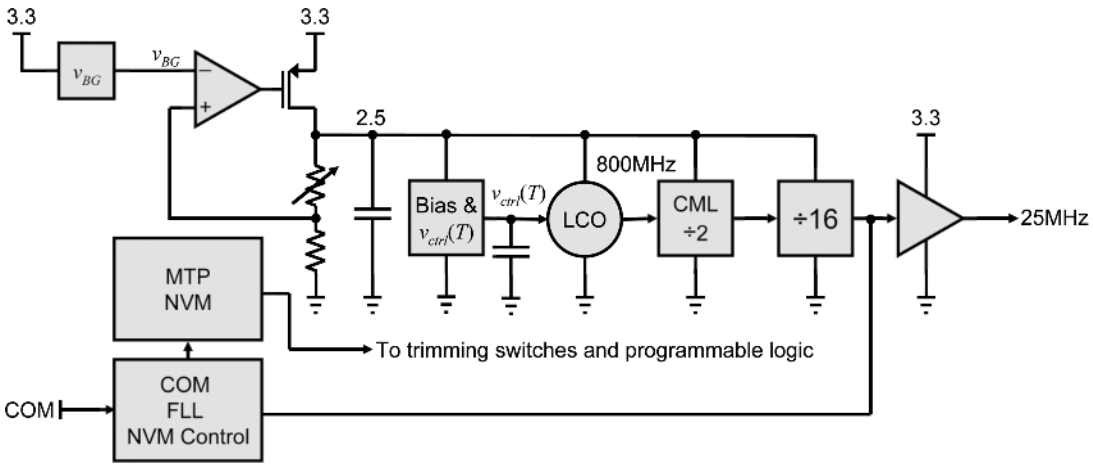


Fig. 6. Chip architecture of the 25-MHz self-referenced solid-state frequency source.

TABLE I
SIMULATED POWER BUDGET SUMMARY

Functional Block	Current (mA)
Band-gap voltage reference	0.050
LDO	0.125
Bias generation (I_{PTAT} and $v_{ctrl}(T)$)	0.225
LCO (including reference mirror)	6.4
CML divide-by-2 (including CML-to-CMOS stage)	2.05
CMOS divide-by-16	0.650
Output driver (10pF || 50Ω load)	8.8
Total	**18**

power-on reset thereafter, and the reference signal is never again required.

A power budget for the device is presented in Table I. Reported figures are for the nominal bias on the true process corner at 25 °C. The LCO and first divider consume over one-half of the total budget, not including the output driver. This was a deliberate design decision to ensure that the LCO and first divider stage would operate reliably against voltage and temperature over all trimming codes as the focus of this work is to determine performance against these variables. It is certainly expected that, in revisions of the device, the power dissipation can be reduced dramatically.

IV. EXPERIMENTAL RESULTS

The prototype 25-MHz frequency source was fabricated in a 0.25-μm 1P5M logic CMOS process, with no specialized analog process options. The die micrograph is shown in Fig. 7. Multiple test points were incorporated into the design permitting access to each individual macro. Thus, the design is pad-limited. The die was packaged in a 48-pin ceramic DIP and mounted on an FR4 PCB for characterization. Trimming and configuration bits in the NVM were set via the serial communication interface which was accessed through a custom software interface. Frequency measurements were captured with a universal frequency counter and analog signals were measured with a 6 1/2 digit DMM. Temperature measurements were performed in a programmable thermal chamber. Critical performance metrics were benchmarked against a 25-MHz COTS XO.

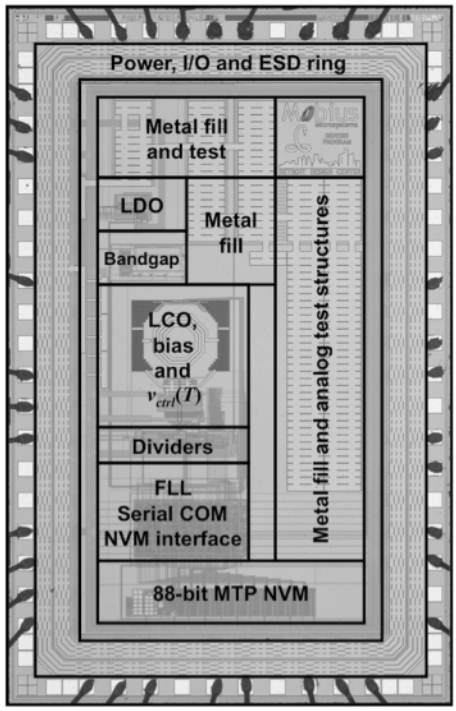


Fig. 7. Die micrograph of prototype 25-MHz self-reference solid-state frequency source fabricated in a 0.25-μm 1P5M logic CMOS process. The die is pad-limited due to analog and digital test points.

A. Nominal Frequency Trim and Native f_{TC}

The solid-state frequency source was configured such that temperature compensation was disabled (i.e., the A-MOS varactors were switched to the supply and not v_{ctrl}). All 2^{14} nominal frequency-trimming codes for the I-MOS array were swept, and results are shown in Fig. 8. The MSB of the I-MOS array caused an undesired -2.6% void in the trimming response. This was determined to be due to parasitics which were not properly

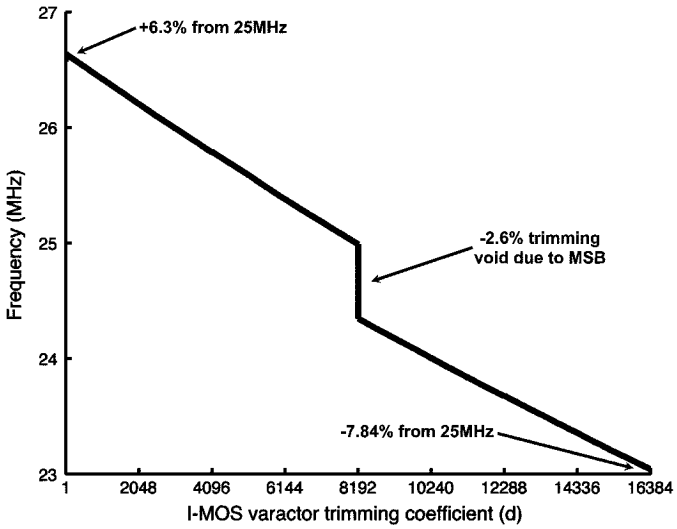


Fig. 8. Measured response for all 2^{14} I-MOS codes for frequency-trimming. Errors in modeling the MSB caused a -2.6% void in the response.

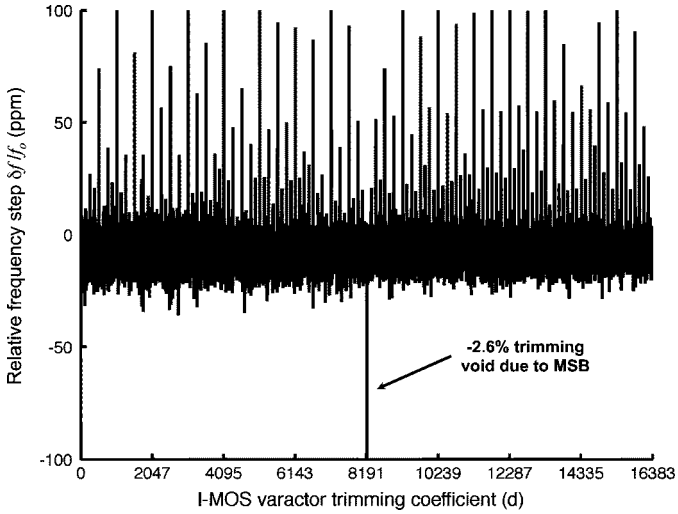


Fig. 9. Measured relative fractional frequency steps of all adjacent 2^{14} I-MOS frequency trimming codes in Fig. 8. Positive codes are non-monotonic. The MSB caused a -2.6% void in the response.

modeled in the tank network. Fig. 9 shows the relative fractional frequency step for adjacent codes. Most codes achieve the designed step size of -20 ppm. Positive codes are nonmonotonic. Of the 16 384 codes, 1348 codes are positive.

The nominal frequency was trimmed automatically to 25 MHz at 30 °C using the FLL, which resolves timing races in comparison to an OCXO as described previously. The uncompensated $f_{\rm TC}$ was measured for the eight different available tail current levels in the LCO. Results are shown in Fig. 10 where the highest tail current exhibits the lowest $f_{\rm TC}$ as expected. Further, and as predicted by (5), the $f_{\rm TC}$ is negative and concave-down. However, the $f_{\rm TC}$ is much greater than that predicted by (6) due to the TC on the transconductor, the A-MOS temperature compensation circuitry and the I-MOS capacitor array.

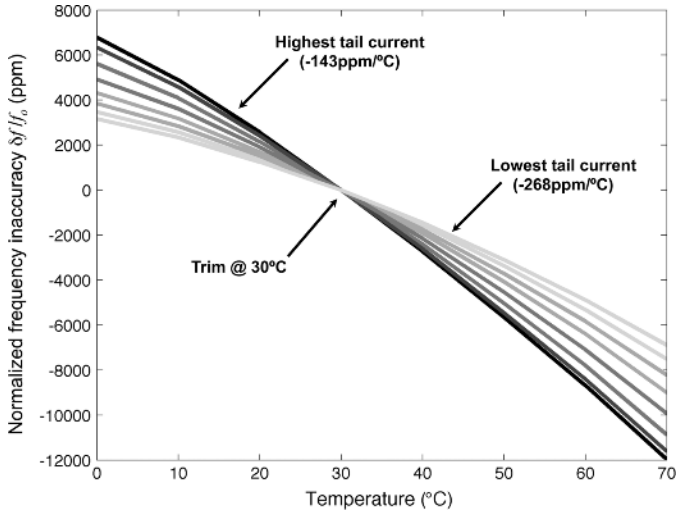


Fig. 10. Measured native $f_{\rm TC}$, post frequency-trimming at 30 °C, for eight different LCO tail current levels.

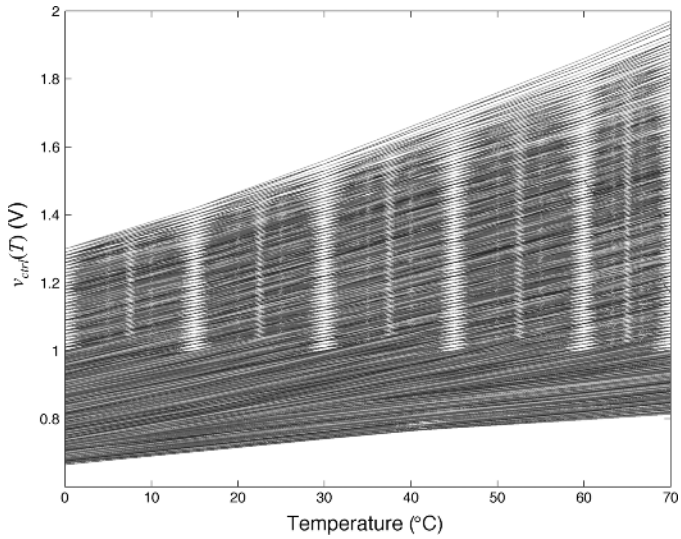


Fig. 11. Measured temperature response for all 16 bias levels and 256 TC codes for $v_{\rm ctrl}(T)$.

B. Temperature-Compensation and PVT $f_{\rm TC}$ Response

The $v_{\rm ctrl}(T)$ circuit was tested for all 16 bias levels and all 256 TC codes at each level. Fig. 11 shows the temperature response for all codes. From these data, the TC was computed for each code and is shown in Fig. 12. The highest bias state yields codes with the highest TC while the lowest bias state exhibits codes with the lowest TC. Further, the TC is significantly nonmonotonic, thus presenting a challenge in properly trimming $f_{\rm TC}$. This nonmonotonic response originates from resistor mismatch in the $v_{\rm ctrl}(T)$ network between both similar and different resistor species. Addressing this, the authors have demonstrated a significantly revised circuit topology for generating a monotonic $v_{\rm ctrl}(T)$ in [30].

The trimming range for the $v_{\rm ctrl}(T)$ circuit is purposely broad due to uncertainty in the TC of the native devices and associated limitations of the models. Once the uncompensated $f_{\rm TC}$ was determined, only a small subset of the codes for $v_{\rm ctrl}(T)$ were explored. Within that portion of the design space, all $v_{\rm ctrl}(T)$

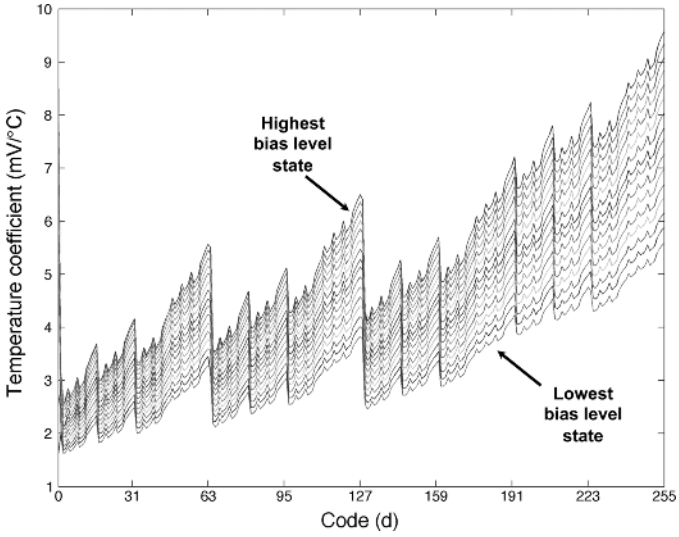


Fig. 12. TC for all 256 TC codes and 16 bias levels for $v_{\rm ctrl}(T)$. Nonmonotonicity originates from resistor mismatch.

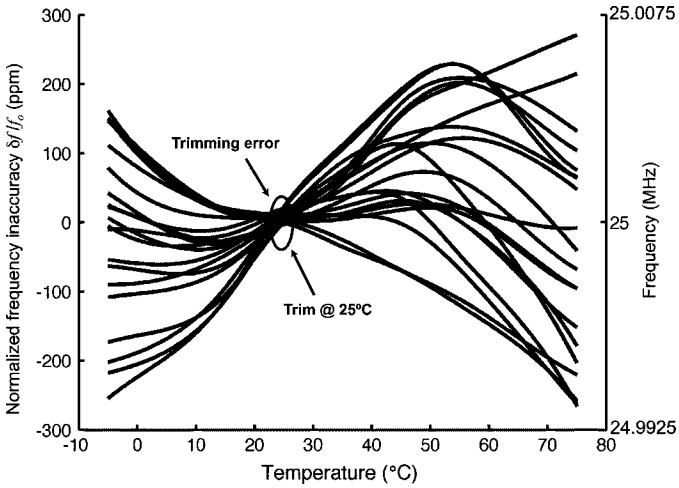


Fig. 13. Density of states concept demonstrated. Twenty different measured temperature-compensation states where the $f_{\rm TC}$ is below $\pm$250 ppm. Eight states exhibit less than $\pm$200 ppm, the best of which is shown in Fig. 14.

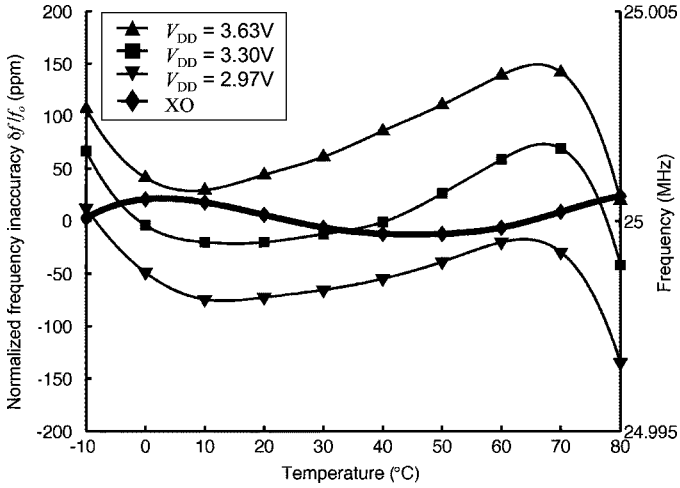


Fig. 14. Measured total frequency inaccuracy for the solid-state frequency source including error due to process (P), voltage 3.3 V $\pm$ 10%, and temperature (-10 °C to 80 °C). Maximum total PVT inaccuracy is $\pm$152 ppm. XO total frequency inaccuracy is $\pm$25 ppm. The polarity of the $f_{\rm TC}$ in [32] was inverted erroneously.

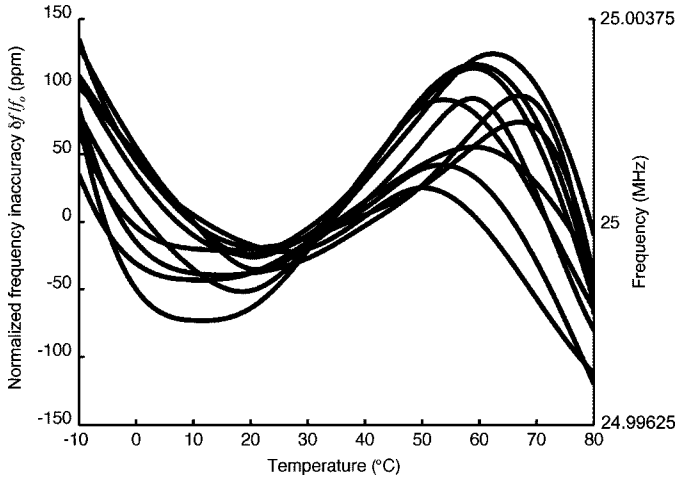


Fig. 15. Measured $f_{\rm TC}$ for 10 trimmed and compensated devices. Average maximum error is 103 ppm while the standard deviation is 26 ppm.

codes were swept and the temperature-compensated frequency response was measured. The objective was to achieve a sufficiently high *density of states* that any one of a set of codes would yield acceptable frequency accuracy, thus reducing the complexity of the trimming algorithm for automatic test equipment.

Fig. 13 shows twenty states which exhibit an $f_{\rm TC}$ below $\pm$250 ppm for -5 °C to 75 °C. The best compensated performance is shown in Fig. 14 where the maximum frequency inaccuracy is $\pm$152 ppm over process, $\pm$10% variation in the power supply and from -10 °C to 80 °C. At the nominal supply, the device meets the requirements for 10/100/1000 Ethernet ($\pm$100 ppm). These results are compared with an XO at the same frequency where the inaccuracy is at most $\pm$25 ppm over the same temperature excursion. The second-order curvature of the $f_{\rm TC}$ for the LCO indicates that the residual TC includes a combination of the concave-down $f_{\rm TC}$ induced by the coil and concave-up $f_{\rm TC}$ set by the reactive compensation through the A-MOS varactors and $v_{\rm ctrl}(T)$. A second-order correction factor could improve the frequency accuracy. At the temperature extremes, the native negative $f_{\rm TC}$ is observed where the LCO is no longer compensated. In these regions, $v_{\rm ctrl}$ operates in the bias-independent regions of the c–v response in Fig. 4(b).

Nine additional devices were trimmed, compensated and measured along with the device in Fig. 14. Results are shown in Fig. 15. The average maximum frequency error over temperature was 103 ppm, with a standard deviation of 26 ppm. As shown, all devices exhibited similar responses against temperature.

C. Other Environmental Sensitivities

Once frequency trimmed and temperature-compensated, the devices were tested for frequency-sensitivity to load. The universal frequency counter supports four conditions: 50-Ω ac- and dc-coupled and 1-MΩ ac- and dc-coupled. Frequency measurements were made for all four loads and a maximum drift of 10 ppm was recorded between the 1-MΩ ac-coupled load and

50-Ω dc-coupled. It was determined that this frequency drift was due to the net power dissipated on the die rising for the 50-Ω case because the current draw from the output driver increased substantially as compared to the 1-MΩ case. Thus, the frequency response follows the TC in Fig. 14 due to the thermal resistance of the package. These results were confirmed first by calculation and further by considering uncompensated devices. Fig. 10 shows that the uncompensated f_{TC} can be up to -268 ppm/°C. Uncompensated devices exhibit up to 400-ppm frequency deflection due to load variation.

Four devices were sealed in a ceramic package and exposed in an autoclave at 25 psi, 100%RH, and 114 °C for 1 h and measured immediately after exposure. No measurable frequency drift was observed. However, 30 of the same devices were packaged in injection-molded 8-TSSOP. Under the same exposure conditions described previously, the average frequency drift across the set was -225 ppm. The root cause of this shift remains under investigation. Recent results indicate piezoresistive and/or piezojunction effects due to residual stress in the packaging and assembly process. Similar effects have been reported previously in [43]–[45]. Further, diffusion of water vapor molecules may induce a change in the net capacitance as presented in [46]. The authors intend to report on their findings thoroughly in an upcoming manuscript.

Finally, long-term frequency drift (commonly referred to as aging) was believed to be possible. The likely mechanism was considered to be device parameter shift due to hot carrier injection (HCI) and/or oxide breakdown (BD). However, the devices that comprise and compensate the LCO do not experience high electrical fields as signal levels are low. Further, it is well known that HCI is accelerated at low temperature as mobility is inversely proportional to temperature and proportional to carrier energy. Considering these factors, a simple experiment was conducted where a device was left powered and at room temperature for 50 days. Measurements were taken every 6 h, and no measurable frequency deviation was observed over the course of the experiment.

D. Frequency- and Time-Domain Measurements

Frequency-domain measurements were captured with a signal source analyzer and are shown in Fig. 16. The FFC SSB phase noise PSD for the solid-state frequency source was superior to that of the XO by up to 6 dB for offset frequencies in excess of 1 MHz. This difference is due to limited power in the XO which determines the FFC phase noise. However, the XO exhibited significantly lower CTC phase noise, as expected due to the higher Q-factor as compared with the LCO. The LCO also exhibited a flicker noise corner near 20 kHz, where the slope transitions from 20 to 30 dB/dec. These results differ from those originally reported in [32], where measurements were captured with a spectrum analyzer and device performance was below the noise floor of the measurement instrument. The signal source analyzer used in these measurements achieves a significantly lower noise floor.

Further considering the comparatively lower Q of the LCO, frequency wander measurements were performed to determine the magnitude of inaccuracy due to the random walk of the oscillation frequency. A spectrum analyzer was centered at 25 MHz

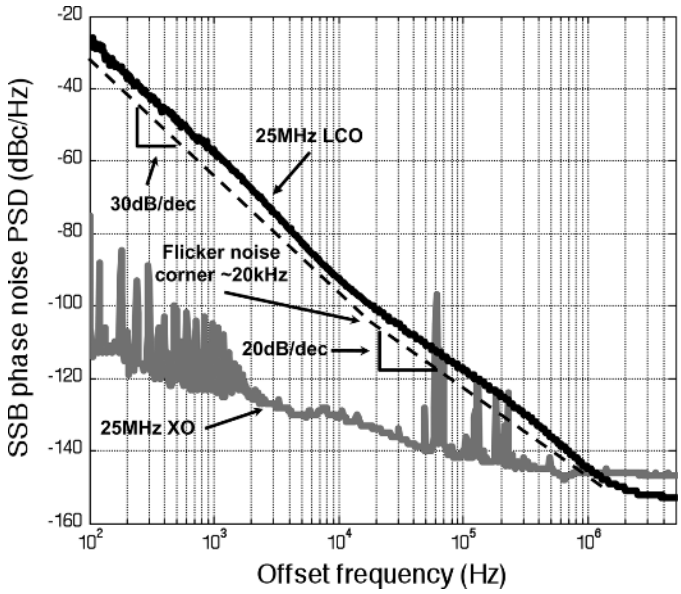


Fig. 16. Measured SSB phase noise PSD for the 25-MHz solid-state frequency source compared with a 25-MHz COTS XO.

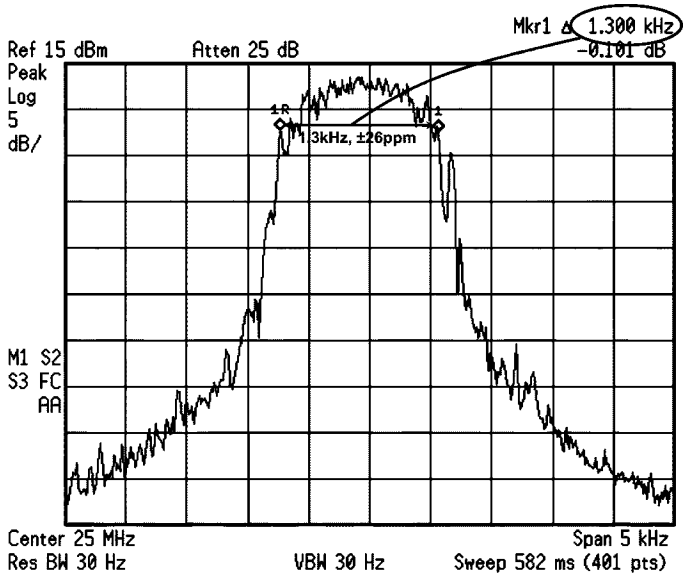


Fig. 17. Measured frequency wander for the 25-MHz solid-state frequency source over a 5-min observation window. The wander is ± 26 $\mathrm{ppm_{pp}}$.

with a resolution bandwidth of 30 Hz and configured to capture the envelope of all measurement sweeps over a 5-min observation period. Results are shown in Fig. 17, where the maximum measured wander is ± 26 $\mathrm{ppm_{pp}}$. These results likely capture some finite temperature instability as they were performed on the bench top at room temperature. Under such conditions, and referring to Fig. 14, the f_{TC} of the solid-state frequency source is nonzero. Further, in many applications this wander is irrelevant. Consider 10/100/1000 Ethernet, where the serializer–deserializer effectively performs the function of a high-pass filter with a 3-dB frequency of 637 kHz [10]. The measurement protocol [10] specifically calls for timing jitter measurements to be performed far-from-carrier and beyond 637 kHz.

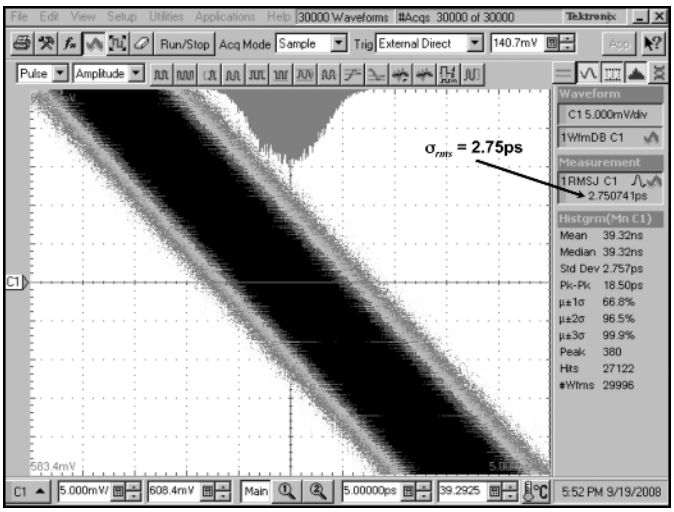


Fig. 18. Measured period jitter for the 25-MHz solid-state frequency source. For approximately 30 k waveforms the period jitter is 2.75 ps_{rms}.

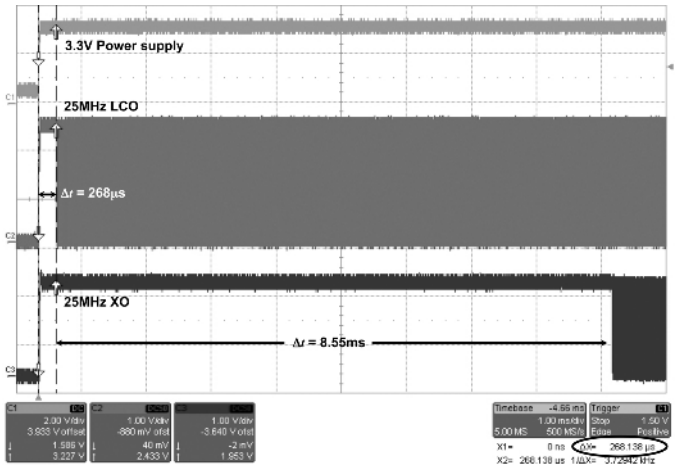


Fig. 19. Measured start-up latency from power-on for the 25-MHz solid-state frequency source and COTS XO. The solid-state oscillator exhibits 268 μs start-up latency while the XO exhibits 8.55 ms.

Period jitter was measured with a digital sampling oscilloscope (DSO). The measurement was performed using the self-triggered technique described in [29], where a power-splitter is utilized to divide the signal from the device under test to trigger the instrument. The measurement is captured on the first falling edge after the trigger event as shown in Fig. 18. An ensemble of approximately 30 k waveforms was collected, from which statistics are computed by the test instrument. The 25-MHz solid-state frequency source exhibited 2.75 ps_{rms} jitter as shown. This result corresponds to less than 38.78 ps_{pp} jitter over 10^{12} clock cycles [29]. The XO at the same frequency exhibited 7.56 ps_{rms} period jitter (not shown), which is due to the fact that the XO exhibits higher FFC phase noise than the solid-state frequency source, as shown in Fig. 15. These results are predicted by (11) and demonstrate that the comparatively poor CTC phase noise in the LCO does not affect the period jitter. On the contrary, the period jitter is determined predominately by the FFC phase noise.

The measurement described previously is a wideband measurement. In practice, the reference drives a channel-rate PLL with a BW from several hundred kilohertz to over 1 MHz. Thus, an argument could be made that the FFC phase noise and associated jitter is not as relevant at the channel rate. However, recall that the phase-noise PSD is represented commonly on a logarithmic scale of frequency. When shown linearly and projected onto the trigonometric function in (11), as in [31], it becomes clear that the jitter remains dominated by the phase noise several hundred kilohertz from the carrier. The authors have confirmed this by measuring performance, including BER, in USB and S-ATA links and intend to report on the results in a forthcoming manuscript.

Finally, the power-on start-up latency was measured for both the solid-state frequency source and the XO using a 20-GSa/s real-time oscilloscope (RTO). Results are shown in Fig. 19. The start-up latency for the solid-state frequency source is 268 μs and is 8.55 ms for the XO. The latency in the solid-state oscillator is not dominated by the start-up latency of the LCO, but the start-up latency associated with the bias and LDO. Nevertheless, the solid-state oscillator is capable of achieving start-up latency which is 30 times less than the XO.

TABLE II
SUMMARY OF MEASURED PERFORMANCE

Parameter	LCO	COTS XO
Output frequency (MHz)	25.00	25.00
Power supply (V)	3.3	3.3
Supply current (mA)	18	14
Power dissipation (mW)	59.4	46.2
Total frequency inaccuracy for 3.3V±10% and –10 to 80°C (ppm)	±152	±25
Total timing error (ppm@10^{12} cycles)	±1125	±2672
SSB phase noise PSD @		
100Hz (dBc/Hz)	-28.2	-75.3
1kHz (dBc/Hz)	-56.9	-123
10kHz (dBc/Hz)	-92.4	-131
100kHz (dBc/Hz)	-118	-141
1MHz (dBc/Hz)	-142	-146
5MHz (dBc/Hz)	-153	-147
Frequency wander over 5 minute observation window (ppm)	±26	<±1
Period jitter		
(ps_{rms})	2.75	7.56
(ps_{pp}@10^{12} cycles)	38.78	106.6
Power-on start-up latency (ms)	0.268	8.55

E. Summary of Experimental Results

Table II summarizes all experimental results. Power dissipation in the solid-state frequency source and the XO is comparable. The solid-state oscillator exhibits ±152 ppm frequency inaccuracy over ±10% variation in the power supply and 90 °C while the XO frequency inaccuracy does not exceed ±25 ppm over the same temperature excursion. Nevertheless, the frequency inaccuracy specifications for data interface protocols such as USB and S-ATA are ±500 ppm and ±350 ppm

respectively. Consequently, the presented solid-state frequency source is well within the requirements for these and related applications.

However, the solid-state oscillator is not well-suited to RF applications because the CTC phase noise is significantly higher than it is for the XO. As described previously, CTC phase noise reduces receiver sensitivity and increases BER in narrowband RF applications [38]. Nevertheless, and as (11) predicts, that has little bearing on the period jitter where the solid-state oscillator achieves performance superior to the XO.

Further consider that the solid-state oscillator demonstrates lower total dynamic frequency inaccuracy once period jitter is considered as the period jitter of the XO is over three times that of the solid-state oscillator. At 25 MHz, 7.56 $\mathrm{ps_{rms}}$ period jitter corresponds to ± 189 ppm frequency or period inaccuracy, while 2.75 $\mathrm{ps_{rms}}$ period jitter corresponds to ± 69 ppm inaccuracy.

Consider the 1σ, or RMS, boundary in the distribution of the periods for these frequency sources where the XO will have an additional ± 120 ppm error as compared to the solid-state oscillator. This concept is captured by quantifying the total timing error in the period of the frequency source. The maximum fractional period error, $\max(\delta T/T_o)$, for a given number of cycles can be determined by considering the inaccuracy in the nominal period, δT_o, and the period jitter together and given by $\max(\delta T/T_o) = |\delta T_o + \alpha\sigma_j|/T_o$, where σ_j is the RMS period jitter, α is the scale factor corresponding to a given cycle count, or observation interval of the signal, and T_o is the ideal period. For example, for 10^{12} cycles, it can be shown that $\alpha = 14.1$ [29]. At this boundary, the total timing error for the solid-state oscillator is ± 1125 ppm and it is ± 2672 ppm for the XO. As shown, $\max(\delta T/T_o)$ is dominated by σ_j and not the nominal frequency inaccuracy.

The total timing error concept is particularly relevant to synchronous data interfaces where the maximum period excursion over a packet determines the eye-closure and ultimately sets the BER [31]. Thus, the presented solid-state frequency source is not only well within the specification for frequency accuracy for applications such as USB and S-ATA, but it also enables lower BER via reduced eye-closure for the channel-rate link by virtue of achieving lower total timing error.

Finally, the start-up latency of the solid-state frequency source is over 30 times lower than it is for the XO. Low start-up latency may enable system power management opportunities in microelectronic systems or in embedded applications, particularly at deep submicron technology nodes where leakage current is significant.

V. Conclusion

A discussion of frequency control and synthesis was presented within the context of historic and recent efforts toward realizing silicon frequency sources. Against that backdrop, the concept of self-referenced LCOs as monolithic frequency sources was presented. The native performance of integrated LCOs was discussed theoretically including frequency drift mechanisms, start-up latency, and period jitter. Design considerations, implementation challenges, and a compensation technique were presented. Within this framework, a frequency-trimmed and temperature-compensated 800 MHz LCO was demonstrated as a 25-MHz self-referenced solid-state frequency source and compared to a COTS XO at the same frequency. The device was realized in a 0.25-μm 1P5M CMOS technology and without any specialized analog process options.

Performance of the frequency-trimming and temperature-compensation circuitry was reported where certain challenges were encountered including a void and nonmonotonic steps in the trimming response as well as non-monotonic steps in the temperature-compensation circuitry. Nevertheless, with no external components, the presented frequency source maintains ± 152 ppm frequency inaccuracy over $\pm 10\%$ variation in the power supply and over 90 °C. Further, when compared to a COTS XO at the same frequency, superior period jitter was demonstrated by virtue of the low FFC phase noise. The results presented herein provide existing proof that the demonstrated approach to developing accurate solid-state frequency sources is feasible by design and achieves the performance requirements for a broad range of data interfaces.

Reported data further suggest ATE production techniques and define design objectives to ensure minimal frequency inaccuracy due to the required analog trimming by maximizing the density of states within a target specification. The authors intend to extend this latest work with a focus toward efficient ATE algorithm development and demonstrate production-worthy solid-state frequency sources well below ± 50 ppm over PVT as well as other environmental conditions including high-humidity environments. Furthermore, the authors intend to present results where these solid-state frequency sources are employed as the reference in data interfaces.

References

[1] R. F. Adams and D. O. Pederson, "Temperature sensitivity of frequency of integrated oscillators," *IEEE J. Solid-State Circuits*, vol. SC-3, no. 4, pp. 391–396, Dec. 1968.

[2] C. Ghidini, J. G. Aranda, D. Gerna, K. Kelliher, and C. Baumhof, "A digitally programmable on-chip RC-oscillator in 0.25 μm CMOS logic process," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, 2005, pp. 400–403.

[3] K. Sundaresan, P. E. Allen, and F. Ayazi, "Process and temperature compensation in a 7-MHz CMOS clock oscillator," *IEEE J. Solid-State Circuits*, vol. 41, no. 2, pp. 433–442, Feb. 2006.

[4] J. F. Kukielka and R. G. Meyer, "A high-frequency temperature-stable monolithic VCO," *IEEE J. Solid-State Circuits*, vol. SC-16, no. 6, pp. 639–647, Dec. 1981.

[5] T.-P. Liu and R. G. Meyer, "A 250-MHz monolithic voltage-controlled oscillator with low temperature coefficient," *IEEE J. Solid-State Circuits*, vol. 25, no. 2, pp. 555–561, Apr. 1990.

[6] D. B. Leeson, "A simple model of feedback oscillator noise spectrum," *Proc. IEEE*, vol. 54, no. 2, pp. 329–330, Feb. 1966.

[7] V. E. Bottom, "A history of the quartz crystal industry in the USA," in *Proc. Annual Frequency Control Symp.*, 1981, pp. 3–12.

[8] *Universal Serial Bus Specification, Rev. 2.0,* Apr. 27, 2000.

[9] *Serial ATA Specification, Rev. 2.5 Gold*, Oct. 27, 2005.

[10] IEEE Standard 802.3, 1998 Edition.

[11] H. C. Nathanson, W. E. Newell, R. A. Wickstrom, and J. R. Davis, Jr., "The resonant gate transistor," *IEEE Trans. Electron Devices*, vol. ED-14, no. 3, pp. 117–133, Mar. 1967.

[12] C. T.-C. Nguyen and R. T. Howe, "An integrated CMOS micromechanical resonator high-Q oscillator," *IEEE J. Solid-State Circuits*, vol. 34, no. 4, pp. 440–455, Apr. 1999.

[13] K. Wang, A.-C. Wong, and C. T.-C. Nguyen, "VHF free-free beam high-Q micromechanical resonators," *IEEE/ASME J. Microelectromech. Syst.*, vol. 9, no. 3, pp. 347–360, Sep. 2000.

[14] S. Lee, M. U. Demirci, and C. T.-C. Nguyen, "A 10-MHz micromechanical resonator Pierce reference oscillator for communications," in *11th Int. Conf. Solid-State Sensors & Actuators Dig. Tech. Papers*, Jun. 2001, pp. 1094–1097.

[15] W.-T. Hsu and C. T.-C. Nguyen, "Stiffness-compensated temperature insensitive micromechanical resonators," in *IEEE Int. Micro Electro Mechanical Syst. Conf. Dig. Tech. Papers*, Jan. 2002, pp. 731–734.
[16] Y.-W. Lin, S. Lee, S.-S. Li, Y. Xie, Z. Ren, and C. T.-C. Nguyen, "60-MHz wine glass micromechanical disk reference oscillator," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2004, pp. 322–323.
[17] Y.-W. Lin, S. Lee, S.-S. Li, Y. Xie, Z. Ren, and C. T.-C. Nguyen, "Series resonant VHF micromechanical resonator reference oscillators," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2477–2491, Dec. 2004.
[18] C. T.-C. Nguyen, "MEMS technology for timing and frequency control," *IEEE Trans. Ultrason., Ferroelectr., Freq. Control*, vol. 54, no. 2, pp. 251–270, Feb. 2007.
[19] K. Sundaresan, G. K. Ho, S. Pourkamali, and F. Ayazi, "Electronically temperature compensated silicon bulk acoustic resonator reference oscillators," *IEEE J. Solid-State Circuits*, vol. 42, no. 6, pp. 1425–1434, Jun. 2007.
[20] J. Arcamone, B. Misischi, F. Serra-Graells, M. A. F. van der Boogaart, J. Brugger, F. Torres, G. Abadal, N. Barniol, and F. Pérez-Murano, "A compact and low-power CMOS circuit for fully integrated NEMS resonators," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 54, no. 5, pp. 377–381, May 2007.
[21] W.-T. Hsu, "Vibrating RF MEMS for timing and frequency references," in *IEEE MTT-S Microw. Symp. Dig. Tech. Papers*, Jun. 2006, pp. 672–675.
[22] W.-T. Hsu and M. Pai, "The new heart beat of electronics—Silicon MEMS oscillators," in *Proc. Electron. Compon. Technol. Conf.*, May 2007, pp. 1895–1899.
[23] W.-T. Hsu, "Low cost packages for MEMS oscillators," in *Proc. Int. Electron. Manufacturing Technol. Symp.*, Oct. 2007, pp. 273–277.
[24] M. Lutz, A. Partridge, P. Gupta, N. Buchan, E. Klaassen, J. McDonald, and K. Petersen, "MEMS oscillators for high volume commercial applications," in *Solid-State Sensors, Actuators and Microsystems Conf. Dig. Tech. Papers*, Jun. 2007, pp. 49–52.
[25] J. Groszkowski, *Frequency of Self-Oscillations*. Oxford, U.K.: Pergamon, 1964.
[26] A. A. Abidi, "RF CMOS comes of age," *IEEE J. Solid-State Circuits*, vol. 39, no. 4, pp. 549–561, Apr. 2004.
[27] M. S. McCorquodale, "Monolithic and top-down clock synthesis with micromachined radio-frequency reference," Ph.D. dissertation, Dept. Elect. Eng. and Comput. Sci., Univ. of Michigan, Ann Arbor, 2004.
[28] M. S. McCorquodale, S. M. Pernia, J. D. O'Day, G. Carichner, and S. Kubba, "A 9.2 mW 528/66/50 MHz monolithic clock synthesizer for mobile μP platforms," in *Proc. IEEE Custom Integrated Circuits Conf. (CICC)*, Sep. 2005, pp. 523–526.
[29] M. S. McCorquodale, J. D. O'Day, S. M. Pernia, G. A. Carichner, S. Kubba, and R. B. Brown, "A monolithic and self-referenced RF LC clock generator compliant with USB 2.0," *IEEE J. Solid-State Circuits*, no. 2, pp. 385–399, Feb. 2007.
[30] M. S. McCorquodale, S. M. Pernia, J. D. O'Day, G. Carichner, E. Marsman, N. Nguyen, S. Kubba, S. Nguyen, J. Kuhn, and R. B. Brown, "A 0.5–480 MHz self-referenced CMOS clock generator with 90 ppm total frequency error and spread spectrum capability," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2008, pp. 350–351, 619.
[31] M. S. McCorquodale, "Self-referenced, trimmed and compensated RF CMOS harmonic oscillators as monolithic frequency generators," in *Proc. of IEEE Int. Frequency Control Symp. (IFCS)*, May 2008, pp. 408–413.
[32] M. S. McCorquodale, S. M. Pernia, S. Kubba, G. Carichner, J. D. O'Day, E. Marsman, J. Kuhn, and R. B. Brown, "A 25 MHz all-CMOS reference clock generator for XO-replacement in serial wire interfaces," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2008, pp. 2837–2840.
[33] P. Maffezzoni, "Frequency-shift induced by colored noise in nonlinear oscillators," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 54, no. 10, pp. 887–891, Oct. 2007.
[34] R. Groves, D. L. Harame, and D. Jadus, "Temperature dependence of Q and inductance in spiral inductors fabricated in a silicon-germanium/BiCMOS technology," *IEEE J. Solid-State Circuits*, vol. 32, no. 9, pp. 1455–1459, Sep. 1997.
[35] *TSMC 0.25 μm Mixed-Signal 2P5M PiP or 1P5M+ MiM Salicide 2.5 V/5.0 V or 2.5 V/3.3 V Design Guide, Rev. 1.0,*, , Mar. 31, 2000.
[36] K.-M. Chen, G.-W. Huang, S.-C. Wang, W.-K. Yeh, Y.-K. Fang, and F.-L. Yang, "Characterization and modeling of SOI varactors at various temperatures," *IEEE Trans. Electron Devices*, vol. 51, no. 3, pp. 427–433, Mar. 2004.
[37] C. A. Marquart, T. Zourntos, S. Magierowski, and N. J. Mathai, "Sliding-mode amplitude control techniques for harmonic oscillators," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 54, no. 11, pp. 1014–1018, Nov. 2007.
[38] B. Razavi, *RF Microelectronics*. Upper Saddle River, NJ: Prentice-Hall, 1998.
[39] I. Zamek and S. Zamek, "Crystal oscillators' jitter measurements and its estimation of phase noise," in *Proc. IEEE Int. Frequency Control Symp. PDA Exhibition*, May 2003, pp. 547–555.
[40] W. P. Robins, *Phase Noise in Signal Sources*. London, U.K.: Peter Peregrinus, Ltd., 1982.
[41] A. Bonfanti, S. Levantino, C. Samori, and A. L. Lacaita, "A varactor configuration minimizing the amplitude-to-phase noise conversion in VCOs," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 53, no. 3, pp. 481–488, Mar. 2006.
[42] P. Väänänen, N. Mikkola, and P. Heliö, "VCO design with on-chip calibration system," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 53, no. 10, pp. 2157–2166, Oct. 2006.
[43] B. Abesingha, G. A. Rincón-Mora, and D. Briggs, "Voltage shift in plastic-packaged bandgap references," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process*, vol. 49, no. 10, pp. 681–685, Oct. 2002.
[44] F. Fruett, G. C. M. Meijer, and A. Bakker, "Minimization of the mechanical-stress-induced inaccuracy in bandgap voltage references," *IEEE J. Solid-State Circuits*, vol. 38, no. 7, pp. 1288–1291, Jul. 2003.
[45] H. Ali, "Stress-induced parametric shift in plastic packaged devices," *IEEE Trans. Comp., Packag., Manufact. Technol. B.*, vol. 20, no. 4, pp. 458–462, Nov. 1997.
[46] A. A. O. Tay and T. Lin, "Moisture diffusion and heat transfer in plastic IC packages," *IEEE Trans. Comp., Packag., Manufact. Technol. A.*, vol. 19, no. 2, pp. 186–193, Jun. 1996.

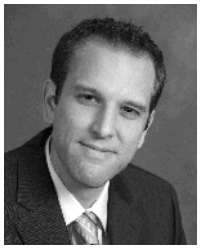
Michael S. McCorquodale (S'95–M'04) was born in Richardson, TX, in 1974. He received the B.S.E. degree with honors from the University of Illinois, Urbana-Champaign, in 1997 and the M.S.E. and Ph.D. degrees from the University of Michigan, Ann Arbor, in 2000 and 2004, respectively, all in electrical engineering. His doctoral work was performed at the National Science Foundation's Engineering Research Center in Wireless Integrated Microsystems,

He was a Member of Technical Staff with Hughes Space and Communications Company, El Segundo, CA, from 1997 to 1998, where he developed GHz InP and SiGe digital integrated circuits including self-referenced oscillators. In 2004, he founded Mobius Microsystems, a venture-backed start-up with headquarters in Sunnyvale, CA, and a design center in Ann Arbor, MI, where he is currently the Chief Technical Officer. He also served as an Adjunct Lecturer with the University of Michigan in 2007, where he instructed a course on process technology and device physics. He has conducted over 12 years of research and development in solid-state and MEMS oscillator technologies. He has published over 20 refereed conference and journal manuscripts and is an inventor on over 25 issued and pending patents.

Dr. McCorquodale is a member of Eta Kappa Nu, ASEE, and AAAS. He was the sole national recipient of the Armed Forces Communications and Electronics Association (AFCEA) Doctoral Fellowship in 2002. He was the recipient of the University of Michigan, College of Engineering, Harry B. Benford Entrepreneurial Leadership Award and the Distinguished University of Michigan Electrical Engineer Award. Governor Jennifer Granholm awarded him for Innovation of the Year and the Largest Potential High-Tech Job Creation in the State of Michigan.

Gordon A. Carichner (M'95) received the B.S.E. and M.S.E. degrees in electrical engineering from the University of Michigan, Ann Arbor, in 1989 and 1991, respectively.

He joined Motorola, Inc., Austin, TX, in 1991, designing circuits for 16-b digital signal processors. He returned to the University of Michigan in 1998 to teach VLSI design and to support EDA software. In 2004, he joined Mobius Microsystems, Inc., Ann Arbor, where he designs digital and analog circuits for monolithic RF LC clock generators. He holds three U.S. patents with others pending.



Justin D. O'Day received the B.S. and M.S. degrees in electrical engineering from the University of Illinois, Urbana-Champaign, in 1998 and 2000 respectively.

He joined the VCAD Group, Cadence Design Systems, Munich, Germany, in 2001, where he specialized in analog/mixed-signal design and methodology. In 2004, he joined Mobius Microsystems, Ann Arbor, MI, as its first employee and currently focuses on analog design and design for test of monolithic LC oscillators. He currently serves as Director of Design Engineering. He has six patents issued or pending.

Mr O'Day is a member of Eta Kappa Nu.

Scott M. Pernia (M'05) was born in Ypsilanti, MI, in 1979. He received the B.S.E. degree (with highest honors) and the M.S.E. degree in electrical engineering from the University of Michigan, Ann Arbor, in 2002 and 2003, respectively.

While an undergraduate and a graduate student at the University of Michigan, he conducted research on low-power pipelined and successive approximation register ADCs. From 2002 to 2004, he worked at Motorola, Inc., Farmington Hills, MI, as a Senior Analog Design Engineer focused on the development of solenoid and motor control ASICs for automotive powertrain. In 2004, he joined Mobius Microsystems, Inc., Ann Arbor, MI, as its second employee and began concentrating on the development and commercialization of monolithic LC-based timing. He holds 22 issued and pending U.S. patents.

Mr. Pernia is a member of Tau Beta Pi and the Golden Key National Honor Society.

Sundus Kubba received the B.S.E. and M.S.E. degrees in electrical engineering from Carleton University, Ottawa, ON, Canada, in 1999 and 2002, respectively. She is currently working toward the M.B.A. degree at the Ross School of Business, University of Michigan, Ann Arbor.

Her graduate research was focused on the design of fully integrated RF CMOS voltage-controlled oscillators. She joined Asahi Glass Automotive Research Center, Ypsilanti, MI, designing antennas for Satellite Digital Audio Radio Systems (SDARS). She joined Mobius Microsystems, Inc., Ann Arbor, MI, from 2005 to 2007, where she designed monolithic RF LC clock generators.

Eric D. Marsman (M'01) was born in Grand Rapids, MI, in 1978. He received the B.S.E. degree (*magna cum laude*) in electrical engineering and the M.S.E. degree in VLSI from the University of Michigan, Ann Arbor, in 2000 and 2002, respectively, where he is currently working toward the Ph.D. degree in VLSI systems focusing on digital signal processing for cochlear implants.

He has held internships with Motorola in the Test Engineering department of World Wide Accessories Division, with Advanced Micro Devices in the CAD Department for the Hammer family of products, and with Agilent Technologies in the ASIC Design Lab on high-speed communication chips. He is currently with Mobius Microsystems Inc., Ann Arbor, as a Senior IC Design Engineer.

Mr. Marsman is a member of Eta Kappa Nu. During his graduate career, he was a Graduate Student Instructor for Introduction to VLSI class for three semesters, for which he won the EECS Outstanding GSI and the ASEE Outstanding GSI awards in 2001 and the Rackham Outstanding GSI for 2002.

Jonathan J. Kuhn was born in 1985. He received the B.S. degree in electrical engineering from Wayne State University, Detroit, MI, in 2007.

He joined Mobius Microsystems Inc., Ann Arbor, MI, as an Intern in integrated circuit design in February 2006 and worked on automation of silicon characterization. He became a full-time Integrated Circuit Design Engineer with Mobius Microsystems in January 2007 and is currently working on production trimming algorithms for monolithic RF LC clock oscillators.

Richard B. Brown (S'74–M'76–SM'91) received the B.S.E. and M.S.E. degrees from Brigham Young University, Provo, UT, in 1976, and the Ph.D. degree from the University of Utah, Salt Lake City, UT, in 1985, all in electrical engineering.

From 1976 to 1981, he worked in computer design as Vice-President of Engineering with Holman Industries, Oakdale, CA, and then as Manager of Computer Development, Cardinal Industries, Webb City, MO. He joined the faculty of the Department of Electrical Engineering and Computer Science, University of Michigan, Ann Arbor, in 1985, where he served as Associate Chair and Interim Chair. He became the Dean of Engineering at the University of Utah in 2004. He has conducted major research projects in the areas of solid-state sensors, mixed-signal circuits, GaAs and silicon-on-insulator circuits, and high-performance and low-power microprocessors.

Prof. Brown is a member of ACM. He serves as chairman of the MOSIS Advisory Council for Education. He was Chair of the 1997 Conference on Advanced Research in VLSI and the 2001 Microelectronic System Education Conference. He has served as Guest Editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS and PROCEEDINGS OF THE IEEE and as Associate Editor of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATED (VLSI) SYSTEMS.