A 25MHz All-CMOS Reference Clock Generator for XO-Replacement in Serial Wire Interfaces

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***Abstract*—A 25MHz all-CMOS clock generator is demonstrated where measured performance makes it suitable for direct replacement of the reference crystal oscillator (XO) for serial wire interfaces. Fabricated in a 0.25μm 1P5M logic CMOS process, and with no external components, the developed clock generator dissipates 59.4mW while exhibiting ±152ppm frequency error over process, ±10% variation in the power supply voltage and from –5–75°C. Nominal period jitter and power-on start-up latency are 3.93ps$_{rms}$ and 268μs respectively.**

I. Introduction

Quartz crystal (XTAL) resonator and crystal oscillator (XO) functionality remain as one of the few device functions that have not been integrated into a microelectronic process technology such as CMOS. Benefits of integration would include reductions in form factor, power and cost as well as improved reliability. However, integration of these devices remains elusive as XTALs are excellent frequency references owing to intrinsic high quality (Q) factor, high frequency accuracy and low frequency temperature coefficient (f_{TC}).

Recently, viable XTAL replacement approaches have been introduced including high-Q MEMS resonators which have been demonstrated for frequency synthesis [1]–[3]. These efforts have focused on the development of a high-Q micromechanically equivalent device that can directly replace XTALs while being integrated in a microelectronic process technology. This previously reported work, though increasingly viable, remains challenging due to difficulties in packaging and process integration, poor power handling [3], high motional impedance [4], limited frequency trimming and large f_{TC} [5]. Some, though not all, of these challenges have been addressed including f_{TC} compensation as shown in [5].

Considering these challenges, the authors have recently demonstrated an XO-replacement clock generation approach in [6] and [7]. The clock generator is referenced to a trimmed and temperature-compensated RF LC oscillator and is implemented in CMOS without any external components and using only standard CMOS devices [6]. The authors have shown in [6] that despite the relatively low-Q of CMOS LC resonators, low jitter and phase noise can be achieved due to low far-from-carrier phase noise and a high frequency division factor from the RF reference. The remaining challenge has been to achieve sufficiently low frequency error. In [7] ±1.8% error was demonstrated over all operating conditions while in [6] ±400ppm was demonstrated. In this work, a new prototype of this class of CMOS harmonic oscillators (CHOs) is demonstrated to achieve ±152ppm total frequency error, thus making the approach suitable for direct replacement of the reference XO for serial wire interfaces including: USB (±500ppm), SATA (±350ppm) and PCIe (±350ppm).

II. Background

LC oscillators (LCOs) are qualitatively stable oscillators, despite exhibiting lower Q as compared to XOs. The far-from-carrier phase noise of an LCO is low because it is tuned, thus enabling low period jitter [6]. Further, CMOS implementations of LCOs favor RF due to area constraints. Thus frequency division to typical frequencies for reference clock generation (10–100MHz) can further enhance the phase noise and jitter as linear frequency division reduces phase noise power quadratically [6]. Confirming these concepts, low-jitter and low phase noise CMOS LCOs were demonstrated as clock generators in [7]. Also shown in [7] was the fact that LCOs exhibit substantial frequency drift over process, voltage and temperature variation.

Frequency error due to process variation can be trimmed with a fixed-capacitor bank. In [6], such an approach was demonstrated along with calibration circuitry. The frequency error is limited by the resolution and the linearity of the capacitor bank. Once the optimal trimming coefficient is determined, it can be stored in nonvolatile memory (NVM). Voltage-, or bias-, induced frequency drift arises from harmonic work imbalance between the inductor and capacitor [8]. The sustaining signal in an LCO is typically driven from a transconductor which overdrives the LC network with a current exhibiting non-zero Fourier coefficients. The capacitor absorbs these harmonics because its impedance is substantially less than that of the inductor. This creates a work imbalance between the inductor and capacitor which is reconciled by a decrease in the frequency. This phenomena can be addressed with supply- and temperature-independent biasing.

Lastly, f_{TC} must be considered. If the zero-phase radian frequency of an LC network is determined while considering the coil loss, R_L, the solution is

$$\omega_o = \sqrt{\frac{1}{LC}\left(1 - \frac{CR_L^2}{L}\right)}. \quad (1)$$

R_L is a real loss; thus the shape of f_{TC} for an LCO is negative and concave-down, though nearly linear. In [6], a reactive compensation approach was introduced where a varactor is driven by a temperature-dependent voltage, thus (1) becomes

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$$\omega_o = \sqrt{\frac{1}{L[C_f+C_v(v_{ctrl}(T))]}\left(1-\frac{[C_f+C_v(v_{ctrl}(T))]R_L^2(T)}{L}\right)} \quad (2)$$

where C_f is fixed capacitance, C_v is variable capacitance and $v_{ctrl}(T)$ is a temperature-dependent linear voltage. An LCO, or CHO, employing this TC compensation approach was presented by the authors in [6] and is enhanced substantially in this work.

III. CHO and Chip Architecture

The CHO is a cross-coupled complementary LCO where the target center frequency is 900MHz, thus enabling division by 36 to generate 25MHz, a typical reference frequency for SATA and other wireline interface standards. A binary-weighted programmable bank of accumulation-mode MOS (A-MOS) varactors serves as C_v in (2). These varactors are biased by a temperature-dependent control voltage, $v_{ctrl}(T)$, which is derived by driving a ΔV_{BE} PTAT current source into a resistor of known TC. A 14-bit binary-weighted array of inversion-mode MOS (I-MOS) varactors serves as C_f in (2). These varactors act as fixed and switchable capacitors through the back-gate bias. The back-gate is biased to the power supply to minimize the fixed capacitance while it is biased to ground to maximize the capacitance presented to the tank. The frequency step size is approximately 20ppm, thus realizing a maximum trimming error of 10ppm.

The chip architecture is shown in Fig. 1. A band-gap referenced low drop-out (LDO) regulator steps 3.3V to a 2.5V core voltage. Trimming coefficients for the LDO, bias currents, v_{ctrl} and the fixed and variable capacitors are stored in a multi-time programmable (MTP) NVM. Custom logic was synthesized to support an NVM interface, serial communications and a digital frequency-locked loop (FLL) for automatic nominal frequency calibration. The FLL implementation has been presented in [6] and determines the fixed capacitor trimming coefficient that centers the CHO frequency due to process variation by running deep counter races between the CHO and an off-chip reference. Once the FLL converges (typically within 100ms), the coefficient is stored in NVM, loaded upon power-on reset thereafter and the reference signal is never again required.

IV. Experimental Results

The prototype clock generator was fabricated in a 0.25µm 1P5M logic CMOS process and is shown in Fig. 2. Because of the prototype nature of this die, numerous pads and test points were incorporated into the design permitting access to each

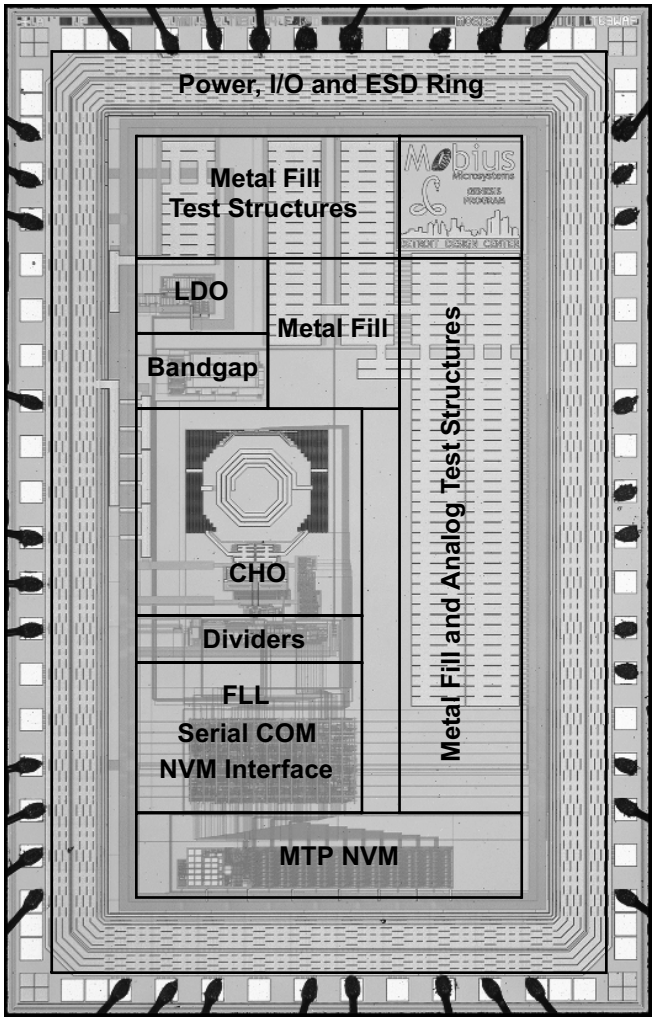


Fig. 2. Die micrograph of prototype XO-replacement 25MHz all-CMOS clock generator fabricated in a 0.25µm 1P5M logic CMOS process. The die is pad-limited due to analog and digital test points.

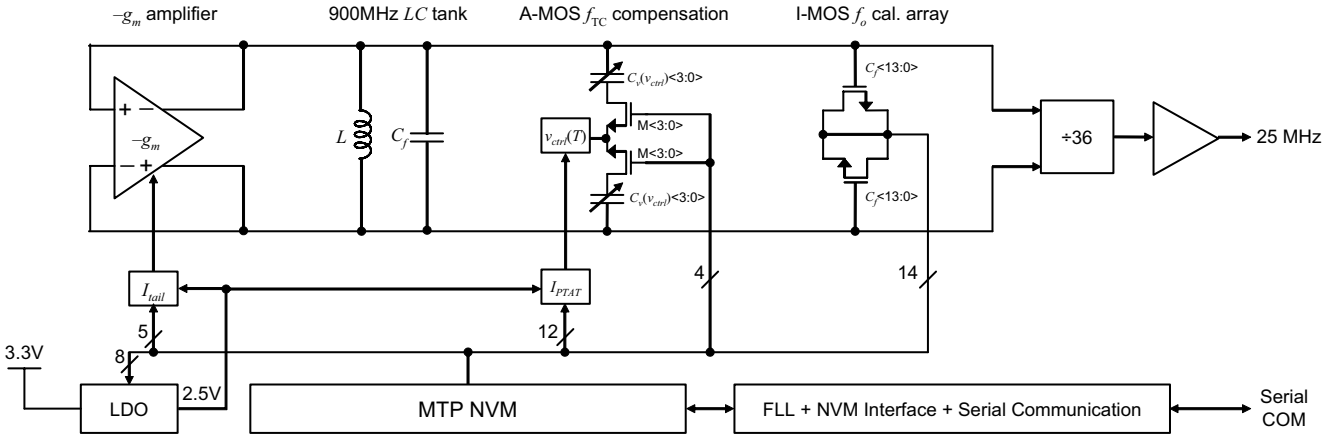
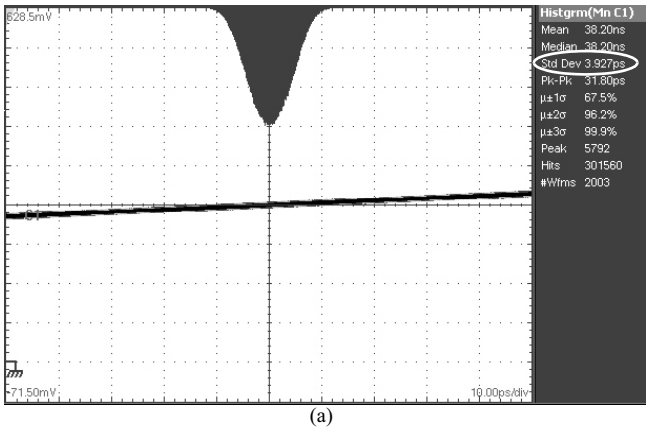


Fig. 1. Schematic of the CHO chip architecture including LCO detail. The buses from the MTP NVM are for analog trimming coefficients.

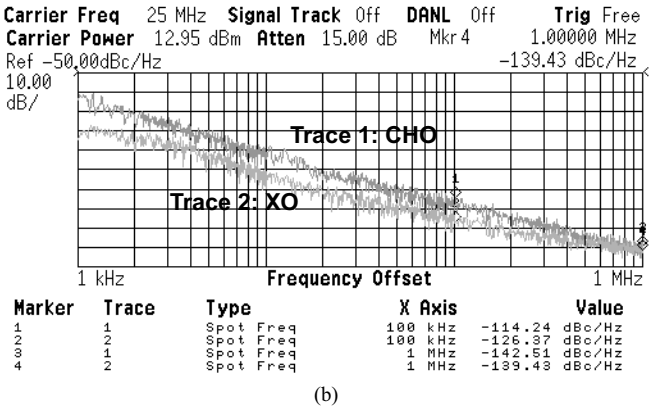
individual circuit block. The die was packaged in a 48-pin ceramic DIP and mounted on an FR4 PCB for characterization. The nominal, room temperature frequency was trimmed automatically using the FLL described in the previous section. Subsequent performance measurements have been compared to a standard commercial off-the-shelf (COTS) XO at 25MHz.

Period jitter was measured using a 20GHz digital sampling oscilloscope where 3.927ps$_{rms}$ jitter was measured as shown in Fig. 3. This measurement corresponds to less than 56ps$_{pp}$ jitter over 10^{12} clock cycles [6]. Frequency-domain measurements were captured with a spectrum analyzer where the SSB phase noise PSD was –114dBc/Hz and –143dBc/Hz at 100kHz and 1MHz offset from carrier respectively. The XO exhibited slightly lower close-to-carrier phase noise. However, both of these measurements are very near the noise floor of the phase noise instrument which was confirmed by measuring a very low phase noise source. Further, the far-from-carrier floor is near –140dBc/Hz. Nevertheless, the close-to-carrier phase noise of the CHO was as expected, where up-converted flicker noise is observed at offsets below 10kHz; thus, the slope is 30dB/decade. Lastly, start-up latency of the clock signal was measured and is shown in Fig. 4 where it is 8.55ms for the XO and 268µs for the CHO, the latter of which is dominated by the voltage regulator start-up latency.

The programmable f_{TC} compensation was determined with an exhaustive approach. Specifically, the f_{TC} compensation coefficient space is explored via test to determine the proper magnitude of the A-MOS varactors and the proper TC of



(a)



(b)

Fig. 3. Measured noise performance: (a) CHO period jitter (b) SSB phase noise PSD for CHO (Trace 1) and COTS XO (Trace 2).

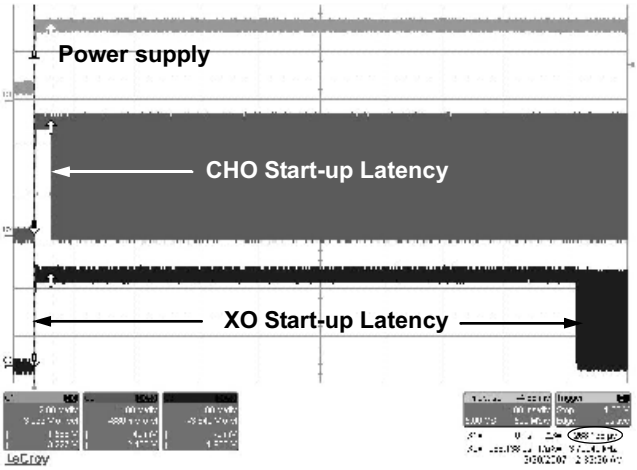


Fig. 4. Measured start-up latency from power-on for the 25MHz CHO (268µs) and the 25MHz COTS XO (8.55ms).

$v_{ctrl}(T)$ such that the f_{TC} induced by the coil loss is cancelled. Once determined, the correct coefficient is stored in NVM and loaded thereafter upon power-on reset. The best frequency response over temperature, from –5º–75ºC and for V_{DD}±10% is shown in Fig. 5 where the maximum frequency error is 152ppm. The maximum frequency error for the XO was 78ppm. The second-order curvature of the f_{TC} response for the CHO indicates that the residual TC includes a combination of the concave-down f_{TC} induced by the coil and concave-up f_{TC} set by the reactive compensation through the A-MOS varactors and $v_{ctrl}(T)$.

For the proposed clock generation approach to be viable, this exhaustive f_{TC} compensation search algorithm must be migrated to automatic test equipment (ATE) and preferably suited to trimming at a single temperature. Due to process variation, it is nearly certain that an ATE algorithm will be unable to select the optimal f_{TC} for each device, as was done in the exhaustive approach. However, the critical analog signals including the band-gap voltage, the regulator voltage and v_{ctrl}. Once these analog parameters are trimmed, the f_{TC} variation is low from device to device. Consequently, the primary design objective becomes to ensure that a sufficient density of

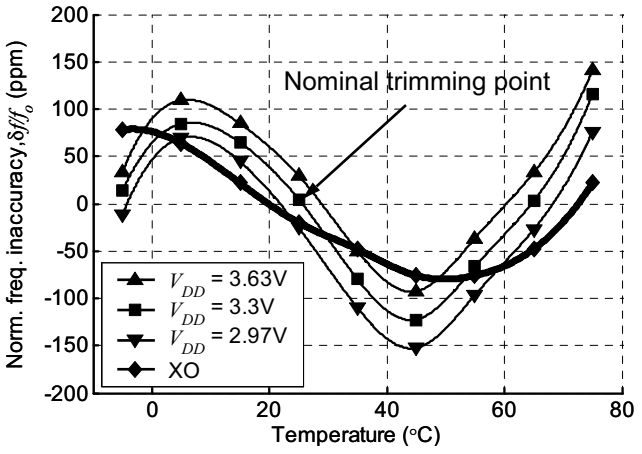


Fig. 5. Measured total frequency error of the CHO normalized to 25MHz and including error due to: process (P) trimming, voltage (V) variation for V_{DD}±10% and temperature (T) variation from –5–75°C. Measured total PVT frequency error is ±152ppm. XO total frequency error is ±78ppm.

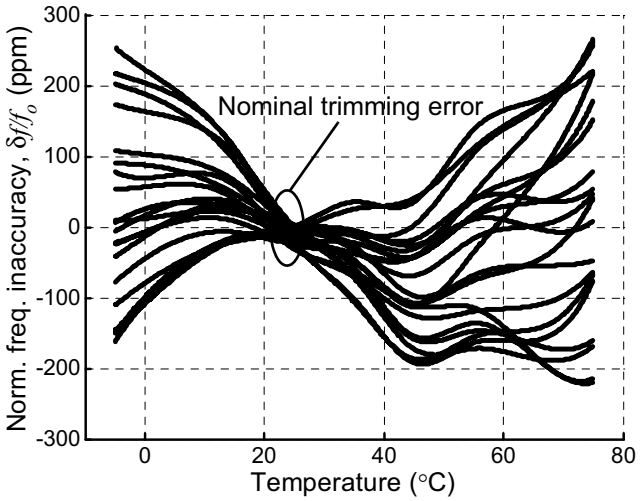


Fig. 6. Density of states concept demonstrated: Measurement of 20 different trimmed TC states where total *PVT* frequency inaccuracy is less than ±250ppm over the total temperature excursion. Eight states exhibit less than ±200ppm total frequency inaccuracy, one of which is shown in Fig. 5.

states for the f_{TC} compensation exists given a frequency error boundary condition. This f_{TC} density of states concept is demonstrated by the measured data for the given device in Fig. 6. Here, 20 f_{TC} states are shown where 8 states exhibit less than ±200ppm frequency error and all 20 exhibit less than ±250ppm. The best state is shown in Fig. 5 where error due to V_{DD} variation is included. Given an error bound of ±200ppm, and for this device, the ATE algorithm must select 1 of the 8 states that exist in the design space. A future design objective is to increase the density of states around the lowest possible frequency error boundary condition. This can be achieved by considering alternative topologies for the v_{ctrl} signal where higher resolution can be achieved. Lastly, the nominal trimming error for each state is shown in Fig. 6 where the trimming temperature is approximately 25ºC.

Table I summarizes the results where the phase noise and power are comparable between the CHO and XO. The CHO exhibits lower jitter while also being implemented entirely in CMOS. Further, the start-up latency of the CHO is over 30 times lower than for the XO. Low start-up latency may enable system power management opportunities, particularly at deep submicron technology nodes.

Though the XO demonstrates lower total frequency error, the CHO demonstrates lower total dynamic frequency error once period jitter is considered because the period jitter of the XO is over twice that of the CHO. At 25MHz, 8ps period jitter corresponds to ±200ppm frequency error while 4ps period jitter corresponds to ±100ppm frequency error. Thus, considering the 1σ, or RMS, boundary in the period distribution, the XO will have an additional ±100ppm error as compared to the CHO. This concept is captured by quantifying the total timing error. The maximum fractional period error, $max(\delta T/T_o)$, for a given number of cycles can determined by considering the center frequency error, δf, and the period jitter as given by $max(\delta T/T_o) = |\delta f^{-1} + \alpha\sigma_j|/T_o$,where σ_j is the RMS period jitter, α is the scale factor corresponding to a given cycle count and T_o is the ideal period. For example, for 10^{12} cycles, it can be shown that α=14.1 [6]. At this boundary, the total timing error for the CHO is ±1562ppm, while it is ±2898ppm for the XO. As shown, $max(\delta T/T_o)$ is dominated by σ_j and not the center frequency error. This is particularly relevant for serial interfaces where the maximum period excursion over a packet will ultimately determine the bit error rate.

TABLE I SUMMARY OF MEASURED PERFORMANCE

Parameter	CHO	COTS XO
Frequency (MHz)	25.00	25.00
Power supply (V)	3.3	3.3
Bias current (mA)	18	14
Power dissipation (mW)	59.4	46.2
Total freq. error (ppm)	±152	±78
Period jitter (ps_{rms}/ps_{pp}@10^{12} cycles)	3.927/56.00	7.560/106.6
*Phase noise PSD @ 100kHz/1MHz (dBc/Hz)	-114/-143	-126/-139
Start-up latency (ms)	0.268	8.55
Total timing error (ppm@10^{12} cycles)	±1562	±2898

*Measurement is near noise floor of instrument.

V. CONCLUSIONS AND FUTURE WORK

This work demonstrates an implementation of an all-CMOS reference clock generator, with no external components, that achieves ±152ppm frequency error over all operating conditions and superior period jitter as compared to a COTS XO at the same frequency. The results presented here provide an existence proof that the demonstrated approach is feasible by design and achieves the performance requirements for a broad range of serial wire interfaces. Additionally, reported data further suggest ATE production techniques and define a design objective to ensure minimal frequency error due to the required analog trimming. The authors intend to extend this latest work with a focus toward efficient ATE algorithm development.

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