A 28-GHz CMOS Phased-Array Beamformer Utilizing Neutralized Bi-Directional Technique Supporting Dual-Polarized MIMO for 5G NR

Jian Pang, *Member, IEEE*, Zheng Li, *Student Member, IEEE*, Ryo Kubozoe, Xueting Luo, Rui Wu, *Member, IEEE*, Yun Wang, *Student Member, IEEE*, Dongwon You, *Student Member, IEEE*, Ashbir Aviat Fadila, Rattanan Saengchan, Takeshi Nakamura, Joshua Alvin, Daiki Matsumoto, Bangan Liu, *Student Member, IEEE*, Aravind Tharayil Narayanan, *Senior Member, IEEE*, Junjun Qiu, *Student Member, IEEE*, Hanli Liu, *Member, IEEE*, Zheng Sun, *Student Member, IEEE*, Hongye Huang, *Student Member, IEEE*, Korkut Kaan Tokgoz, *Member, IEEE*, Keiichi Motoi, *Member, IEEE*, Naoki Oshima, Shinichi Hori, *Member, IEEE*, Kazuaki Kunihiro, *Member, IEEE*, Tomoya Kaneko, *Member, IEEE*, Atsushi Shirane, *Member, IEEE*, and Kenichi Okada, *Senior Member, IEEE*

***Abstract*— This article presents a low-cost and area-efficient 28-GHz CMOS phased-array beamformer chip for 5G millimeter-wave dual-polarized multiple-in-multiple-out (MIMO) (DP-MIMO) systems. A neutralized bi-directional technique is introduced in this work to reduce the chip area significantly. With the proposed technique, completely the same circuit chain is shared between the transmitter and receiver. To further minimize the area, an active bi-directional vector-summing phase shifter is also introduced. Area-efficient and high-resolution active phase shifting could be realized in both TX and RX modes. In measurement, the achieved saturated output power for the TX-mode beamformer is 15.1 dBm. The RX-mode noise figure is 4.2 dB at 28 GHz. To evaluate the over-the-air performance, 16 H+16 V sub-array modules are implemented in this work. Each of the sub-array modules consists of four 4 H+4 V chips. Two sub-array modules in this work are capable of scanning the beam from −50° to +50°. A saturated EIRP of 45.6 dBm is realized by 32 TX-mode beamformers. Within 1-m distance, a maximum SC-mode data rate of 15 Gb/s and the 5G new radio downlink packets transmission in 256-QAM could be supported by the module. A 2 × 2 DP-MIMO communication is also demonstrated with two 5G new radio 64-QAM uplink streams. Thanks to the proposed area-efficient bi-directional technique, the required core area for a single element-beamformer is only 0.58 mm^2. Compact and low-cost 5G millimeter-wave MIMO systems could be realized.**

***Index Terms*— 28 GHz, 5G new radio, beamformer, bi-directional, CMOS, dual-polarized multiple-in-multiple-out (MIMO) (DP-MIMO), error vector magnitude (EVM), neutralization, phased-array.**

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Jian Pang, Zheng Li, Ryo Kubozoe, Xueting Luo, Rui Wu, Yun Wang, Dongwon You, Ashbir Aviat Fadila, Rattanan Saengchan, Takeshi Nakamura, Joshua Alvin, Daiki Matsumoto, Bangan Liu, Aravind Tharayil Narayanan, Junjun Qiu, Hanli Liu, Zheng Sun, Hongye Huang, Korkut Kaan Tokgoz, Atsushi Shirane, and Kenichi Okada are with the Tokyo Institute of Technology, Tokyo 152-8552, Japan (e-mail: pangjian@ssc.pe.titech.ac.jp).

Keiichi Motoi, Naoki Oshima, Shinichi Hori, Kazuaki Kunihiro, and Tomoya Kaneko are with NEC Corporation, Kawasaki 211-8666, Japan.

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I. Introduction

ULTRA-FAST wireless data access will be provided by the incoming 5G new radio (NR). Spectrum resource at millimeter-wave frequency band is ready to boost the available data rate significantly with the enlarged channel bandwidth. The dual-polarized multiple-in–multiple-out (MIMO) (DP-MIMO) technique will also be employed in 5G NR to improve the spectrum efficiency with spatial multiplexing [1], [2].

Recent research has been focused on high-performance 5G millimeter-wave phased-array transceivers [1]–[16]. However, to realize the 5G millimeter-wave DP-MIMO systems, which require numerous transceiver paths, the conventional phased-array solutions are still expensive regarding the total die area. [11] and [12] based on the LO phase shifting architecture realize gain-invariant and high-resolution phase shifting. However, additional power and area are consumed for the distributed LO. [1] and [2] are capable of steering the dual-polarized beams. However, the separated beamformer circuits for the TX and RX still occupy large die area. Due to the reduced array antenna pitch at millimeter-wave frequencies, the chip area reduction becomes essential not only for a minimized manufacturing cost but also for a low-loss distribution from the chip to the antenna.

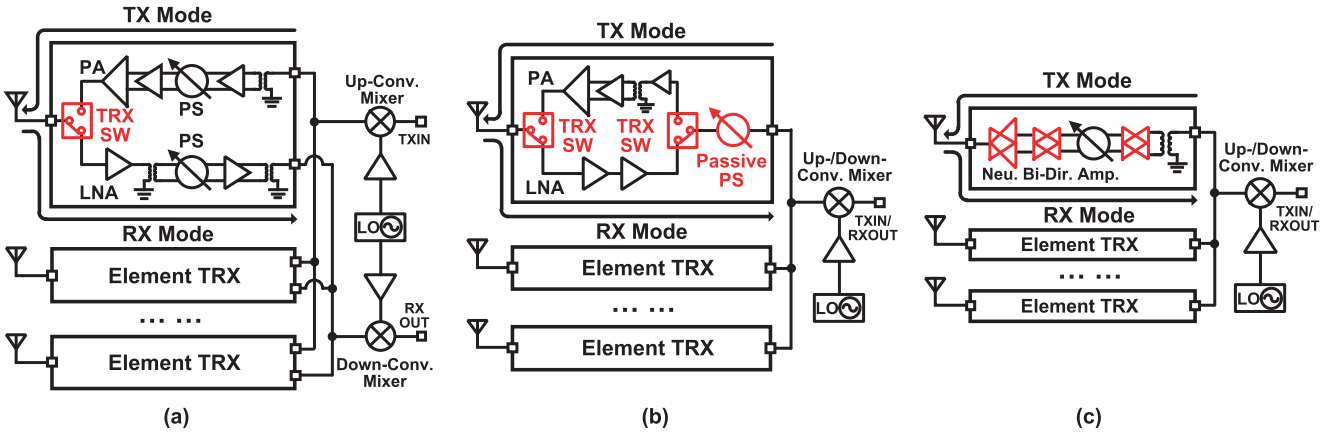


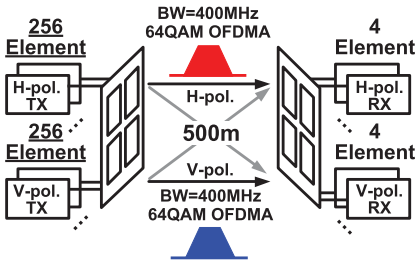
Fig. 1. Block diagrams of (a) conventional phased-array transceiver, (b) conventional bi-directional phased-array transceiver, and (c) proposed bi-directional phased-array transceiver.

This article introduces an eight-element 28-GHz phased-array beamformer chip for the 5G millimeter-wave DP-MIMO systems. To minimize the chip area and the manufacturing cost, a neutralized bi-directional technique is proposed in this article, which allows for the transmitter and receiver to share the same beamformer chain without any modifications. An active vector-summing phase shifter supporting bi-directional operation is also presented for an improved RF-path gain. From 26.5 to 29.5 GHz, the measured rms gain and phase errors during phase shifting are less than 0.5 dB and 2.1°, respectively. In measurement, the implemented 16H+16V sub-array module is capable of supporting a maximum single-carrier-mode (SC-mode) data rate of 15 Gb/s within 1-m distance. Standard-compliant 5G NR orthogonal-frequency-division-multiplexing-access-mode (OFDMA-mode) data streaming in 256-QAM is realized with a 400-MHz bandwidth. A 2×2 DP-MIMO communication in 64-QAM is also demonstrated in this work. Thanks to the proposed bi-directional technique, the element-beamformer in this work consumes only 0.58-mm^2 core area. High-performance and area-efficient chips are realized for low-cost and compact 5G millimeter-wave MIMO systems.

This article is an extension of [17] and is organized as follows. The transceiver architecture considerations for 5G DP-MIMO systems are introduced in Section II. Section III presents the detailed analysis for the proposed neutralized bi-directional circuits. The beamformer chip implementation and the corresponding measurement results are demonstrated in Section IV. Finally, Section V concludes this article.

II. Architecture Considerations

5G millimeter-wave MIMO systems are costly in various aspects. Simply by increasing the number of antenna paths, MIMO communication could be supported. However, the system physical size will be enlarged due to the additional antennas. Polarized MIMO utilizes cross-pol. isolation to transmit two independent data streams. Due to the shared aperture between different streams, the system size could be minimized with a decreased antenna number. Fig. 2(a) shows a single-user



(a)

Carrier Freq.	28GHz	Distance	500m
Channel BW.	400MHz	FSPL	115dB
kTB	-88dBm	Req. SNR	26dB (64-QAM)
TX		RX	
TX Array Size	256	RX Array Size	4
TX Array Gain $G_{TXArray}$	48dB	RX Array Gain $G_{RXArray}$	6dB
Antenna Gain-Imp. Loss G_{Ant}	4dB	Antenna Gain-Imp. Loss G_{Ant}	4dB
PA Pout P_{outPA}	5dBm	NF	8dB
TX EIRP	57dBm (P_{outPA}+$G_{TXArray}$+G_{Ant})	Pwr. After FSPL P_{Rev}	-58dBm (EIRP-FSPL)
Received TX-to-RX SNR	32dB (P_{Rev}+$G_{RXArray}$+G_{Ant}-NF-kTB)		

(b)

Fig. 2. (a) Usage scenario for dual-polarized MIMO and (b) link budget.

MIMO scenario with DP-MIMO configuration. Two data streams are transmitted through the horizontal-polarization (H-polarization) and vertical-polarization (V-polarization) of a dual-polarized antenna simultaneously. The communication distance is 500 m (line-of-sight). Fig. 2(b) shows the link budget example for such a data link. A four-element receiver array is adopted for the user equipment (UE), considering the system size and power dissipation. At the transmitter side, an output power of 5 dBm including the power backoff is usually available for supporting 64-QAM (OFDM-mode) communication in CMOS technology [3], [18], [19]. Thus, regarding a target 64-QAM SNR of 26 dB, a 256-element array will be required in the base station (BS) for maintaining a 32-dB TX-to-RX SNR over 500-m communication distance.

Even more element-transceivers will be demanded for supporting the DP-MIMO. Thus, area and cost reductions should also be considered for such millimeter-wave MIMO systems.

Fig. 1(a) shows the block diagram of conventional phased-array transceiver [10]. The antenna is shared by the TRX switch. However, the separated transmitter and receiver chains along with the up- and down-conversion circuits are not area-efficient. To realize a compact and low-cost phased-array system, the bi-directional architecture is employed in Fig. 1(b) [20], [21]. With another switch for the power amplifier (PA) and low noise amplifier (LNA), the signal flow direction of such a bi-directional amplifier could be reconfigured. Thus, the bi-directional operation could be supported. The area reduction is realized by sharing the passive phase shifters, the combiner/divider, the mixer, and the LO distribution between TX mode and RX mode. However, for a multistage amplifier operating in millimeter-wave frequencies, the occupied area is usually dominated by the interstage passive components. Thus, the system size reduction for a conventional bi-directional transceiver is still limited due to the unshared passives.

To further minimize the area consumption, Fig. 1(c) presents the proposed bi-directional transceiver. A differential neutralized bi-directional amplifier is introduced in this work. The inter-stage passives are completely shared between TX mode and RX mode. The required die area for each beamformer path is further minimized. Additionally, the proposed bi-directional amplifier maintains the cross-coupling-capacitor (CCC) neutralization in both TX and RX modes [22], [23]. Thanks to the gate–drain capacitance neutralization, the insertion loss caused by the matching sharing is compensated by an improved RF-path gain. A high-stability beamformer circuit with independent phase and gain tuning is realized by the enhanced reverse isolation.

III. Proposed Neutralized Bi-Directional Circuits

Neutralized bi-directional circuits are introduced in this work to minimize the cost of 5G millimeter-wave DP-MIMO systems. The remaining part of this section will introduce the circuit implementation of several key building blocks for the proposed bi-directional beamformer.

A. Neutralized Bi-Directional Amplifier

The operation of bi-directional transceiver relies on the bi-directional amplifier. As mentioned in Section II, the conventional bi-directional amplifier based on the TRX switches still occupies large ON-chip area due to the unshared interstage passives. As a result, this work introduces a neutralized bi-directional amplifier to support the bi-directional operation with a compact chip size.

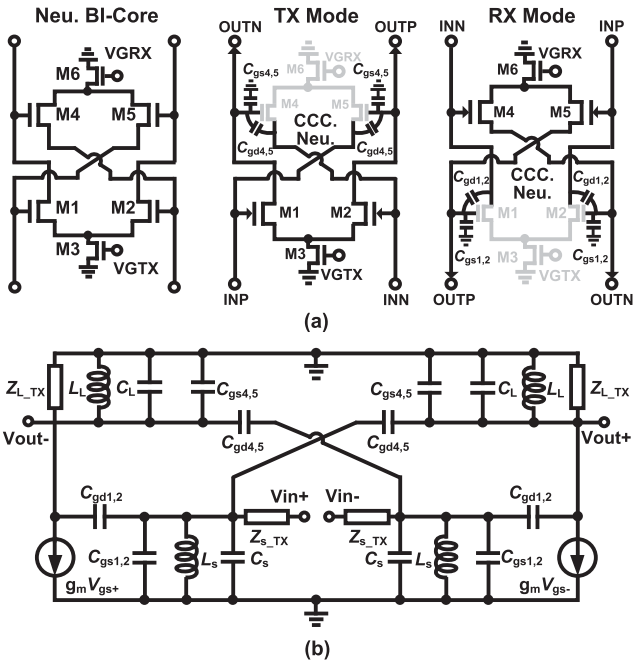


Fig. 3. (a) Circuit schematic of proposed bi-directional core and (b) TX-mode small-signal equivalent circuit.

Fig. 3(a) presents the circuit schematic of the neutralized bi-directional amplifier core. Two transistor pairs in cross-coupling connection are included. Transistors M1 and M2 are utilized for TX mode, while M4 and M5 are utilized for RX mode. The TRX mode selection is realized by switching the tail bias (M3 and M6). $C_{gs1,2}$, $C_{gd1,2}$ and $C_{gs4,5}$, $C_{gd4,5}$ in the figure denote the parasitic capacitances for M1, M2 and M4, M5, respectively. Fig. 3(b) demonstrates the small-signal equivalent circuit for the bi-directional amplifier in TX mode. C_s and L_s represent the passive components for input matching, while C_L and L_L represent the output matching. The voltage gain of the TX-mode amplifier could be derived with (1) (shown at the bottom of this page), where C_1 and C_2 in the equation are defined as follows:

$$C_1 = C_{gd1,2} + C_{gd4,5} + C_s + C_{gs1,2} \tag{2}$$

$$C_2 = C_{gd1,2} + C_{gd4,5} + C_L + C_{gs4,5}. \tag{3}$$

To neutralize the gate–drain capacitance $C_{gd1,2}$, the same transistor size should be applied between M1, M2 and M4, M5 [22], which leads to $C_{gd1,2} = C_{gd4,5}$. Therefore, (1) could be simplified with the following equation:

$$\frac{V_{out+}}{V_{in+}}(j\omega) = \frac{g_m Z_{L\_TX}}{\left(1 + \dfrac{Z_{L\_TX}}{j\omega L_L} + j\omega Z_{L\_TX} C_2\right)\left(1 + \dfrac{Z_{s\_TX}}{j\omega L_s} + j\omega Z_{s\_TX} C_1\right)}. \tag{4}$$

$$\frac{V_{out+}}{V_{in+}}(j\omega) = \frac{g_m Z_{L\_TX} + j\omega Z_{L\_TX}(C_{gd1,2} - C_{gd4,5})}{\left(1 + Z_{L\_TX}/j\omega L_L + j\omega Z_{L\_TX} C_2\right)\left(1 + Z_{s\_TX}/j\omega L_s + j\omega Z_{s\_TX} C_1\right) + g_m Z_{s\_TX} Z_{L\_TX} j\omega (C_{gd1,2} - C_{gd4,5})} \tag{1}$$

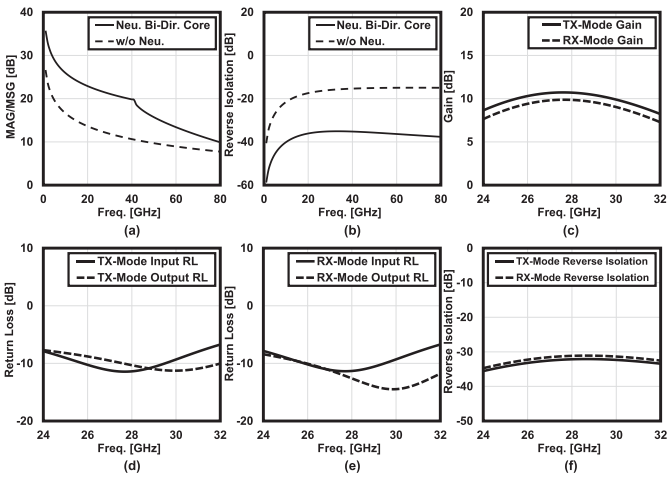


Fig. 4. Simulated performance for proposed bi-directional core: (a) MAG/MSG and (b) reverse isolation. Simulated performance for single-stage bi-directional amplifier: (c) TX-mode and RX-mode gain, (d) TX-mode return loss, (e) RX-mode return loss, and (f) TX-mode and RX-mode reverse isolation.

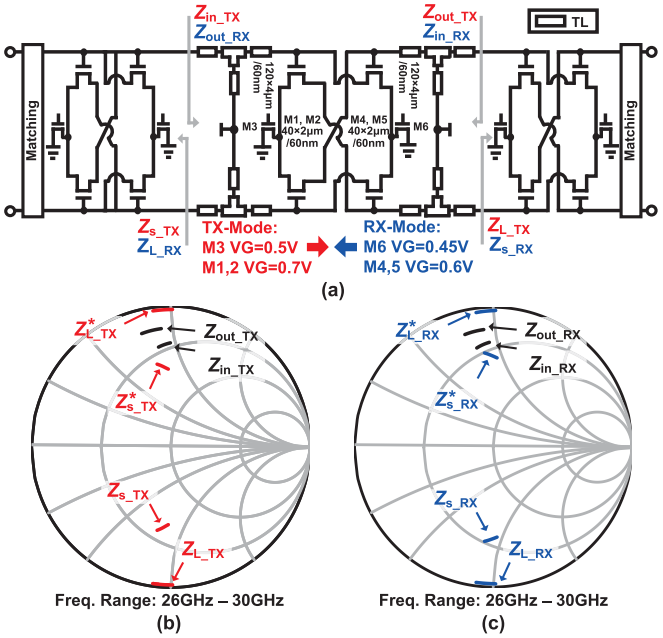


Fig. 5. (a) Circuit schematic of three-stage cascaded bi-directional amplifier and inter-stage matching conditions for (b) TX mode and (c) RX mode.

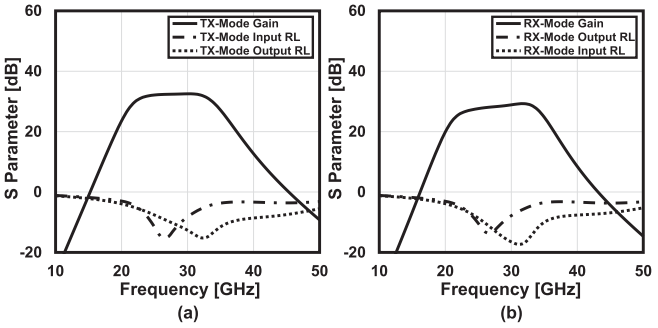


Fig. 6. Simulated performance of three-stage neutralized bi-directional amplifier in (a) TX mode and (b) RX mode.

Thanks to the gate–drain capacitance neutralization, the proposed neutralized bi-directional core achieves improved MAG/MSG and reverse isolation. Fig. 4(a) and (b) compares the proposed core with a differential pair without neutralization. The transistor size ($40 \times 2\ \mu$m/60 nm, defined with finger number $\times$ finger width/channel length), bias condition, and power dissipation are kept to be the same for comparison. After canceling the feedback path caused by the gate–drain capacitance of transistors, the MAG/MSG of the proposed neutralized core is improved from 12.2 to 21.4 dB at 28 GHz. The reverse isolation is also improved from -16.2 to -35.2 dB, which contributes to a higher stability. This improvement is also robust against the process variation because the neutralization is achieved by an additional transistor pair.

The realized gain also depends on the matching. The denominator in (4) demonstrates the input and output matching conditions for the TX-mode amplifier. The voltage gain of the RX-mode amplifier could also be derived with a similar analysis. If we define the source and load impedances for the RX-mode amplifier as Z_{s_RX} and Z_{L_RX}, respectively, the optimum gain is obtained in both TX- and RX-mode when Z_{s_TX} equals Z_{L_RX} and Z_{s_RX} equals Z_{L_TX}. This condition can be satisfied when the neutralized bi-directional amplifier is connected with non-switchable circuits. Appropriate values of C_s, L_s, C_L, and L_L could be selected considering the resonant frequency and the required bandwidth. Fig. 4(c)–(f) present the simulated performance of a single-stage bi-directional amplifier with 100-Ω source and load impedances. The RX-mode bias is slightly reduced for power saving. At 28 GHz, 10.7-dB gain is achieved in TX mode, while 9.9-dB gain is realized in RX mode. The return loss for all conditions is lower than -9 dB from 26.5 to 29.5 GHz. The reverse isolation is improved to lower than -30 dB.

When the proposed bi-directional amplifier is cascaded, $Z_{s\_TX} = Z_{L\_RX}$ and $Z_{s\_RX} = Z_{L\_TX}$ cannot be maintained any more due to the switchable circuits. Additional optimization is required for the inter-stage matching networks. Fig. 5(a) shows a three-stage cascaded bi-directional amplifier. The Z_{s_TX}, Z_{L_TX}, Z_{s_RX}, and Z_{L_RX} of the middle-stage amplifier are plotted in Fig. 5(b). Z_{L_TX} and Z_{L_RX} are almost along the edge of Smith chart due to the capacitive load impedance from the next-stage core. For inter-stage matching, the conjugate impedances $Z^*_{s\_TX}$ and $Z^*_{L\_RX}$, $Z^*_{L\_TX}$ and $Z^*_{s\_RX}$ are required to be maintained. At millimeter-wave frequencies, the differences between $Z^*_{s\_TX}$ and $Z^*_{L\_RX}$, $Z^*_{L\_TX}$ and $Z^*_{s\_RX}$ are not so large. Thus, passive components with fixed values could still be selected for minimizing the TX-mode and RX-mode insertion loss [Z_{in_TX}, Z_{out_TX}, Z_{in_RX}, and Z_{out_RX} in Fig. 5(b) and (c)]. The simulated performance of the three-stage neutralized bi-directional amplifier is demonstrated in Fig. 6. A TX-mode gain of 33 dB and an RX-mode gain of 28 dB are realized at 28 GHz. The return loss is always less than -10 dB within 26.5 GHz to 29.5 GHz. The TX-mode and RX-mode power consumptions are 46 and 27 mW, respectively, for the

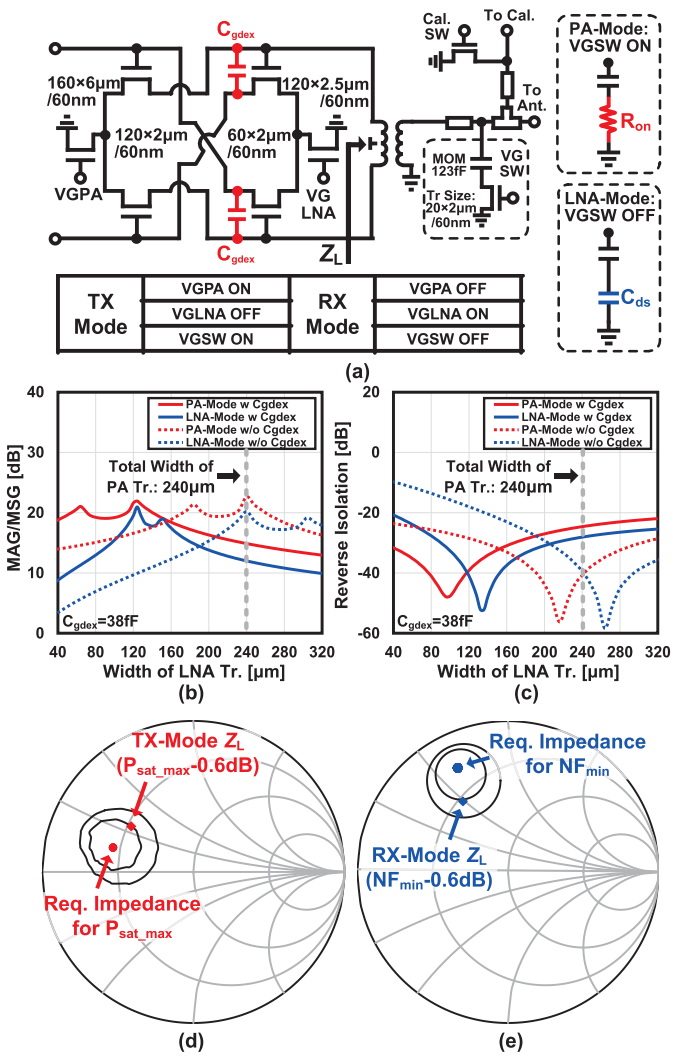


Fig. 7. (a) Circuit schematic of proposed PA-LNA based on unbalanced neutralized bi-directional technique. (b) MAG/MSG and (c) reverse isolation of PA-LNA core with and without proposed extra C_{gdex} compensation. (d) TX-mode Z_L and (e) RX-mode Z_L created by switchable matching.

three-stage amplifier. The matching networks are realized with the transmission lines in this work. The transmission lines are folded for a compact layout.

Transformers with large impedance transformation ratio are sometimes utilized for realizing optimum matching at lower frequencies. However, the input impedance of transistors at millimeter-wave frequencies is significantly smaller than that at low frequencies. As a result, reasonable matching performance can still be maintained by the proposed matching sharing.

B. PA-LNA

The bi-directional amplifier mentioned previously achieves the gate-drain capacitance neutralization with the same-sized transistor pairs. However, for PA and LNA, the requirements on transistor size are usually different. For improving power delivery, large-sized transistors are usually utilized in PA. While, small-sized transistors are employed in LNA for power saving. Therefore, an unbalanced neutralized bi-directional

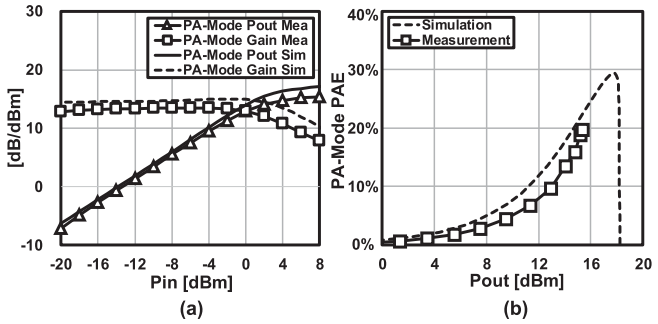


Fig. 8. Measured (a) PA-mode output power and (b) PA-mode PAE.

amplifier is further proposed for the PA and LNA in this work. Fig. 7(a) shows the circuit schematic. Two capacitors C_{gdex} are attached to the LNA transistors to compensate the additional gate-drain capacitance from the PA transistors. Thus, the neutralization condition can still be maintained in both operation modes. Fig. 7(b) plots the MAG/MSG and reverse isolation against the LNA transistor size. The size of PA transistors is fixed (60×2 μm/60 nm). As demonstrated in the figure, with C_{gdex}, a much smaller transistor size could be selected for the LNA. The power consumption could be saved along with an improved gain in RX mode.

Considering the TX-mode linearity and RX-mode noise figure (NF), the antenna-sharing network requires careful design considerations. In this work, an adaptive antenna-sharing network is utilized for minimizing the insertion loss and the ON-chip area. As shown in Fig. 7(a), the proposed adaptive network consists of a large-sized capacitor and a small-sized switching transistor. The required impedance for PA-mode optimum output power (P_{sat_max}) and the required impedance for LNA-mode minimum NF (NF_{min}) are simulated at the interface of Z_L and plotted in Fig. 7(d) and (e). By switching the transistor, the proposed adaptive antenna-sharing network is optimized to realize the required impedances for P_{sat_max} and NF_{min} in PA mode and LNA mode, respectively. Fig. 7(d) and (e) also demonstrate the realized Z_L in simulation. The induced loss during switching are both 0.6 dB in PA- and LNA-mode at 28 GHz. In measurement, a saturated output power of 15.4 dBm and an output $P_{1\,dB}$ of 13 dBm are achieved by the PA [Fig. 8(a)]. As demonstrated in Fig. 8(b), the measured maximum power-added-efficiency is 20% including the TRX switch. Fig. 9 shows the LNA-mode NF along frequency. An NF of 4.6 dB is achieved at 28 GHz.

C. Active Bi-Directional Phase Shifter

The bi-directional phase shifter architecture also requires design considerations. To support the bi-directional operation, passive phase shifters with reciprocal characteristics have been widely used [20], [21], [24]–[26]. However, to maintain enough phase-shifting coverage and resolution, an insertion loss of around -8 dB is usually induced at RF path by the passive phase-shifting circuitry [27]–[29]. RF buffers for gain compensation will be required, which occupies extra area. To address this issue, this work introduces a gain-improved

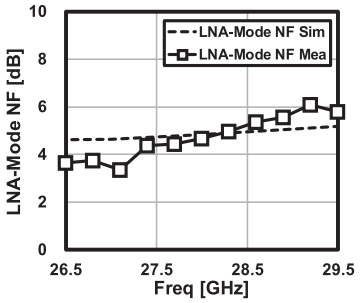
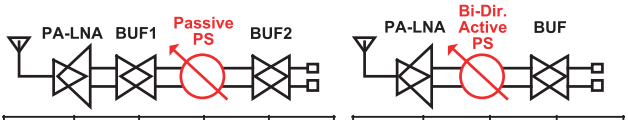


Fig. 9. Measured LNA-mode NF.



TX Mode	PA	BUF2	Passive PS	BUF1
Gain	15dB	10dB	-10dB	10dB
P_{DC}	120mW	20mW	0mW	20mW
Area	0.2mm²	0.2mm²	1.0mm²	0.2mm²
RX Mode	LNA	BUF2	Passive PS	BUF1
Gain	15dB	10dB	-10dB	10dB
NF	5dB	6dB	10dB	6dB
Cascaded NF	5.0dB	5.1dB	5.3dB	5.3dB
IIP3	-5dBm	0dBm	20dBm	0dBm
Cascaded IIP3	-5.0dBm	-15.4dBm	-15.8dBm	-18.4dBm

(a)

TX Mode	PA	Bi-Dir. Active PS	BUF1
Gain	15dB	0dB	10dB
P_{DC}	120mW	20mW	20mW
Area	0.2mm²	0.3mm²	0.2mm²
RX Mode	LNA	Bi-Dir. Active PS	BUF1
Gain	15dB	0dB	10dB
NF	5dB	10dB	6dB
Cascaded NF	5.0dB	5.4dB	5.5dB
IIP3	-5dBm	0dBm	0dBm
Cascaded IIP3	-5.0dBm	-15.4dBm	-18.2dBm

(b)

Fig. 10. Beamformers with (a) passive bi-directional phase shifter and (b) active bi-directional phase shifter.

bi-directional phase shifter based on the active vector-summing method. Fig. 10 shows a simplified system comparison. The characteristics for each building block here are example values. Fig. 10(a) summarizes the system gain, area, and power consumptions for a TX-mode conventional bi-directional beamformer with passive phase shifting. Additional buffers will be required at the RF path for compensating the induced loss. Fig. 10(b) shows the bi-directional beamfomer with active phase shifting. Further area reduction could be achieved by the proposed active bi-directional phase shifter. Regarding the RX-mode performance, comparisons on NF and IIP3 have also been included in Fig. 10. Although the passive phase shifter can realize a much better IIP3 than the active phase shifter, with the same RX-mode gain, the system performance will not be so different between using passive and active phase shifters.

Fig. 11(a) shows the circuit schematic of the active vector-summing bi-directional phase shifter. Two switchable poly-phase filters (PPFs) and two bi-directional variable gain amplifiers (VGAs) are included. The proposed switchable PPF can be configured into normal PPF mode or adder mode with additional control switches. During the operation, one of the switchable PPF is in PPF mode, while the other one is in adder mode. As a result, active vector-summing could be realized in both TX and RX modes. Fig. 11(b) demonstrates the circuit of bi-directional VGA. Two balanced neutralized bi-directional cores with flipped input connection are utilized for the VGA.

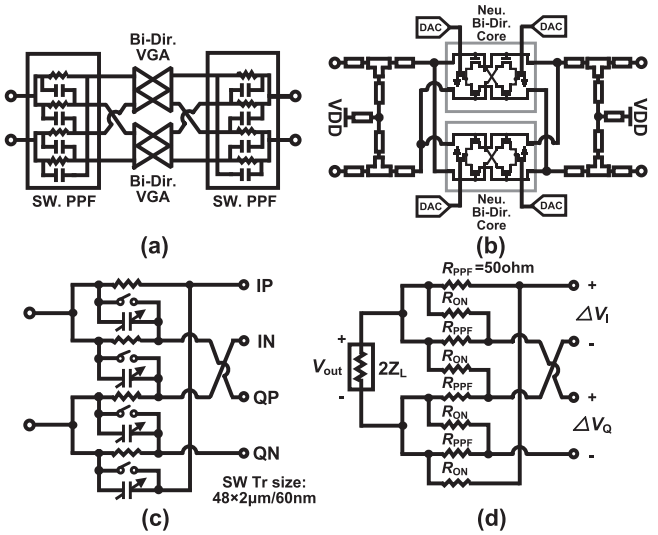


Fig. 11. (a) Block diagram of proposed bi-directional phase shifter, (b) circuit schematic of bi-directional VGA, (c) circuit schematic of switchable PPF, and (d) equivalent circuit of switchable PPF in adder mode.

The gain control is realized by tuning the tail bias with a 10-bit digital-to-analog converter (DAC). Because the gate-drain capacitance neutralization is realized by the proposed bi-directional core, the phase variation will be suppressed during gain tuning [30]. The proposed VGA achieves 23-dB gain control with less than 3.6° phase variation at 28 GHz.

Fig. 11(c) shows the circuit schematic of the switchable PPF. Totally four NMOS switches are implemented in shunt with the capacitors. In normal PPF mode, the switches will be turned off, and the parasitic capacitance will be part of the required capacitance for PPF. While, in adder mode, the switch will be turned on to short the capacitor path for summing up the I/Q signals. The ON-resistance R_{on} is required to be minimized in this design due to the imperfect I/Q summing. Fig. 11(d) shows the equivalent circuit of the adder-mode switchable PPF. The output voltage swing V_{out} could be derived regarding the input voltages ΔV_I and ΔV_Q

$$V_{out} = -\frac{Z_L(R_{PPF} - R_{ON})}{R_{PPF}R_{ON} + Z_L R_{PPF} + Z_L R_{ON}}\Delta V_I + \frac{Z_L(R_{PPF} + R_{ON})}{R_{PPF}R_{ON} + Z_L R_{PPF} + Z_L R_{ON}}\Delta V_Q \quad (5)$$

R_{PPF} in the equation represents the resistance of PPF, while R_{ON} is the ON-resistance of the NMOS switches. Ideally, R_{ON} equals zero and the proposed switchable PPF functions as an ideal adder. However, when R_{ON} equals a non-zero value, gain imbalance between the I and Q path will be induced. The I/Q gain imbalance due to the imperfect summing could be expressed with the following equation:

$$\text{Gain Imbalance} = 20\log\frac{R_{PPF} + R_{ON}}{R_{PPF} - R_{ON}}(\text{dB}). \quad (6)$$

Thus, a comparatively large transistor size is selected considering the I/Q gain imbalance in adder mode. The measured I/Q gain imbalance caused by the proposed adder-mode PPF is less

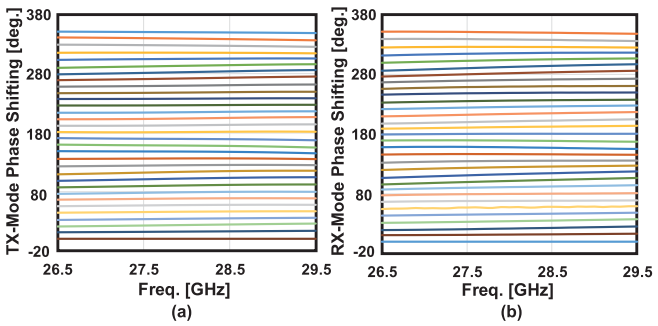


Fig. 12. Measured 5-bit (a) TX-mode phase shifting and (b) RX-mode phase shifting of proposed beamformer.

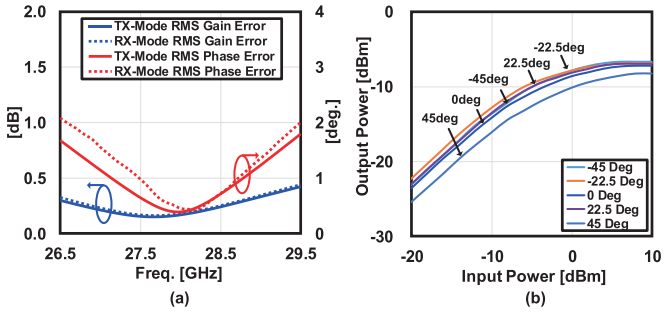


Fig. 13. Measured (a) rms gain and phase errors of proposed beamformer and (b) linearity of the phase shifter.

than 2 dB. During simulation and measurement, the adder gain imbalance is compensated by the DAC-controlled I/Q VGAs.

Fig. 12 shows the measured 5-bit TX-mode and RX-mode phase shifting for the beamformer. 360° could be covered by the proposed phase shifter. A −2.5-dB gain is achieved by the phase shifter at 28 GHz, which is much higher than the passive solutions. Fig. 13(a) demonstrates the measured rms gain and phase errors during phase shifting. The measured TX-mode and RX-mode gain errors are always less than 0.5 dB from 26.5 to 29.5 GHz. The rms phase errors are always less than 2.1°. Fig. 13(b) shows the measured linearity of the proposed phase shifter at 28 GHz within ±45°. The measured worst IP_{1dB} is −8 dBm. The proposed RX-mode beamformer is carefully designed and the IIP3 is not limited by the phase shifter. The RX-mode IIP3 can be improved by decreasing the gain along the RX path.

IV. Transceiver Implementation and Measurement

Fig. 14 shows the system block diagram of the proposed bi-directional beamformer chip. Totally eight element-beamformers are implemented into the same chip, and they are divided into two groups for the H- and V-polarizations, respectively. Thanks to the circuits introduced in Section III, the proposed phased-array beamformer is capable of operating in TX and RX modes with the same bi-directional circuit chain. Each of the element beamformers in this work consists of a two-stage PA-LNA, an RF buffer, a bi-directional phase shifter, and an isolation buffer. The gain control for each antenna path is realized by tuning the RF buffer. The RF buffer

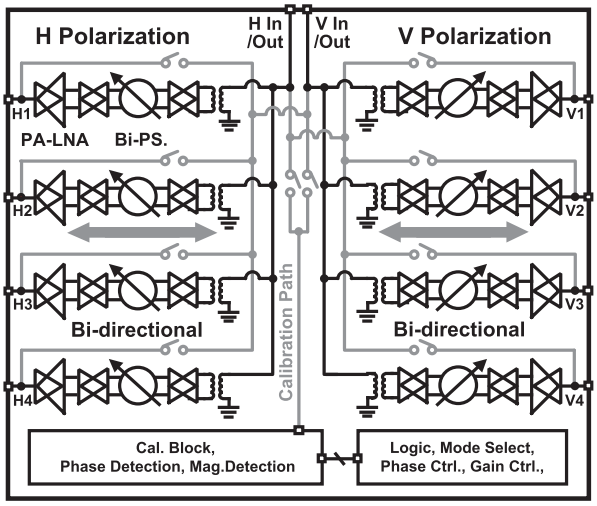


Fig. 14. Block diagram of proposed 4H+4V bi-directional beamformer.

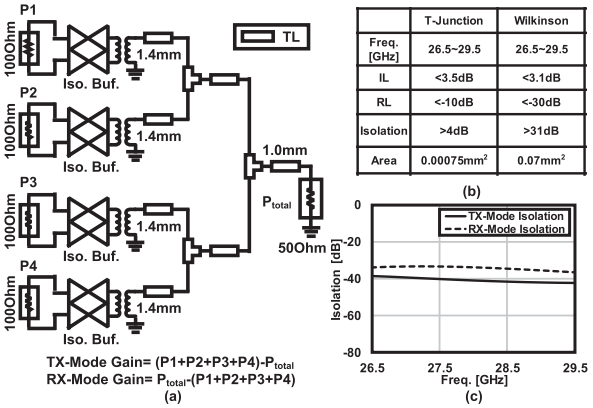


Fig. 15. (a) Block diagram of on-chip distribution and isolation buffers. (b) Comparison on T-junction divider and Wilkinson divider. (c) Simulated isolation between antenna paths for T-junction divider with isolation buffers.

in this work adopts a similar circuit topology with the VGA utilized in the phase shifter. Wide-range and phase-invariant gain tuning is maintained for each path.

The 28-GHz input–output signal is distributed in single-ended formation. The T-junction dividers/combiners are utilized for dividing/combining the RF signals. Fig. 15 shows the RF signal distribution. Compared with the Wilkinson dividers, the T-junction dividers realize acceptable insertion loss and return loss with compact chip area. However, the isolation between paths will be degraded in this case. To improve the isolation, isolation buffers are added in each element beamformers. The simulated isolation between element beamfomers are improved to over 34 dB in both TX- and RX-modes. Thus, only the failure in isolation buffers may influence the dividing network characteristics, but the following stages such as phase shifter, power amplifier can also be isolated from the dividing network. The loss caused by the distribution and balun is also compensated by the buffers. The simulated distribution gain is around 4 dB in TX mode and 5 dB in RX mode.

To calibrate the mismatches between different element beamformers, the magnitude and phase detection circuits similar to [11] are also included in this work. The signals for

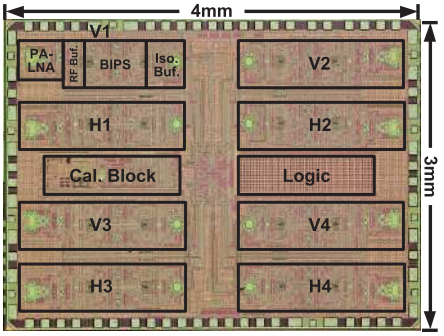


Fig. 16. Die micrograph of proposed phased-array beamformer chip.

TABLE I
CORE AREA OF BLOCKS

Blocks	Core Area $[\mathrm{mm}^2]$
PA-LNA	0.11
RF Buf.	0.07
Bi-Dir. Phase Shifter	0.29
Isolation Buf.	0.11
Logic	0.43

detection from each element beamformers are redirected to the calibration block by configuring the switches. After the magnitude and phase detections, the readout values are sent out from the chip through the SPI. The corrections for magnitude and phase errors are further done by tuning the VGA and phase shifter. For saving the area, the calibration paths are shared between the H and V beamformers. To improve the on-chip H–V isolation, shielded transmission lines are utilized for H- and V-pol. signal distributions [31]. Additionally, the switches for signal re-direction are properly sized considering the off-state isolation. As a result, over 39-dB ON-chip H-V isolation is achieved at 28 GHz.

The proposed beamformer is fabricated in a standard 65-nm CMOS process to further minimize the manufacturing cost. Fig. 16 shows the die micrograph of the chip. The chip size is 3 mm × 4 mm. Table I summarizes the core area breakdown of the chip. Thanks to the proposed neutralized bi-directional technique, the required core area for the element-beamformer is only 0.58 mm^2.

Fig. 17(a) demonstrates the measured on-wafer frequency response of the single-path TX-mode beamformer. The measured gain excluding the divider is around 20 dB at 28-GHz band. The gain variation over frequency is less than 2 dB. The measured TX-mode output power at 28 GHz for the element-transceiver is shown in Fig. 17(b). The achieved P_{sat} and P_{1dB} are 15.1 and 11.3 dBm, respectively. Fig. 17(c) shows the measured gain for the single-path RX-mode beamformer. The measured gain excluding the combiner is around 17 dB. The measured RX-mode NF is shown in Fig. 17(d). The NF is on-wafer measured with the Keysight PNA-X network analyzer N5247A. The achieved RX-mode NF is 4.2–5.0 dB from 26.5 to 29.5 GHz. Additionally, the output power, output noise floor, and IM_3 are measured at 28 GHz for the RX-mode

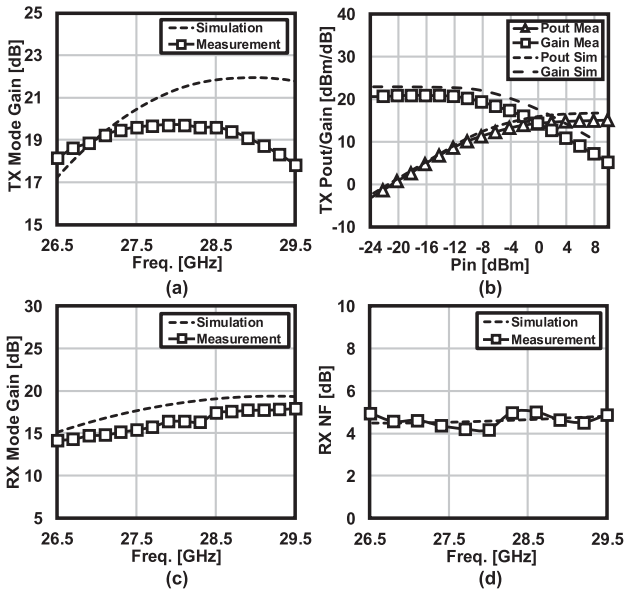


Fig. 17. Measured transceiver characteristics: (a) TX-mode gain, (b) TX-mode output power, (c) RX-mode gain, and (d) RX-mode NF.

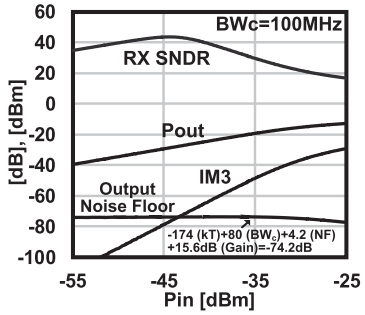


Fig. 18. Measured SNDR for RX-mode beamformer.

beamformer and presented in Fig. 18. With 100-MHz channel bandwidth, the calculated SNDR of the RX-mode beamformer is also shown in the same figure. A maximum SNDR of 43.6 dB is realized.

The single-path TX-mode beamformer is further evaluated with the SC-mode and OFDMA-mode modulated signals. Fig. 19(a) summarizes the measured EVMs in 64-QAM with 100- and 400-MHz signal bandwidths. The achieved peak EVMs are −41.4 and −37.5 dB for 100- and 400-MHz bandwidths, respectively. In both bandwidth conditions, over 10.6-dBm output power is available for an EVM of lower than −25.5 dB. Fig. 19(b) summarizes the measured EVMs in 256-QAM. Minimum EVMs of −40.7 and −36.7 dB are achieved with bandwidths of 100 and 400 MHz, respectively. An output power of 6.6 dBm is available for a lower than −32.5-dB EVM. The TX-mode beamformer is also evaluated with 5G NR OFDMA-mode downlink packets. In this measurement, the center frequency is 28 GHz, and the channel bandwidth is fixed to 400 MHz. Fig. 20(a) demonstrates the measured OFDMA-mode EVMs in QPSK, 16-QAM, 64-QAM, and 256-QAM. The modulation coding schemes (MCSs) in the figure are defined in 5G NR MCS index table 2 [32]. According to the 5G NR standard [33],

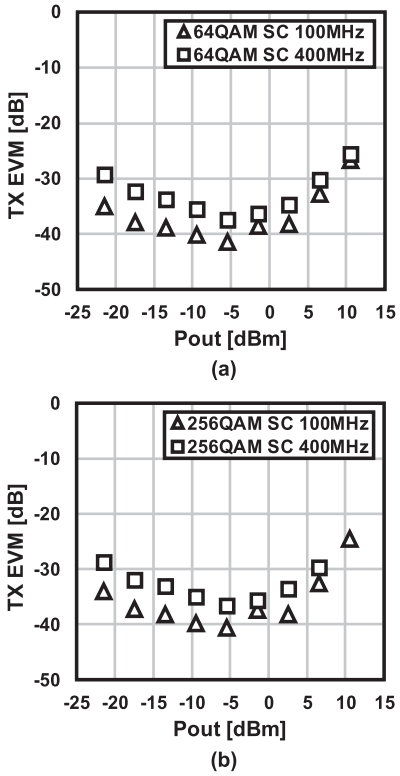


Fig. 19. Measured SC-mode EVMs in (a) 64-QAM and (b) 256-QAM for TX-mode beamformer.

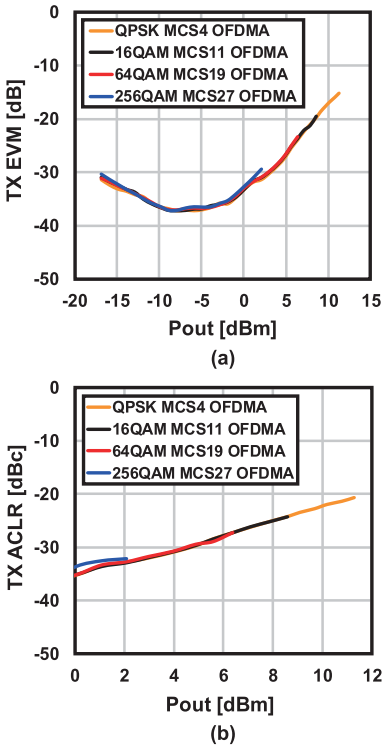


Fig. 20. Measured (a) OFDMA-mode EVMs and (b) ACLRs for TX-mode beamformer.

less than −15.1-dB (17.5%), −18.1-dB (12.5%), −21.9-dB (8.0%), and −29.1-dB (3.5%) EVMs are required for the BS downlink regarding modulation schemes of QPSK, 16-QAM, 64-QAM, and 256-QAM, respectively. Adjacent channel leakage ratios (ACLRs) of less than −28 and −17 dBc are also regulated in 5G NR standard for the BS and UE, respectively [33]. Fig. 20(b) shows the measured ACLRs for the TX-mode beamformer. This work realizes the maximum output power of 5.6 dBm in 64-QAM and 0.1 dBm in 256-QAM with EVMs of −25 and −32 dB, respectively. The measured ACLRs at the output power mentioned above are −28.4 dBc in 64-QAM and −33.1 dBc in 256-QAM. For modulation schemes of QPSK and 16-QAM, the maximum output power is limited to 5.6 dBm due to the ACLR limitation.

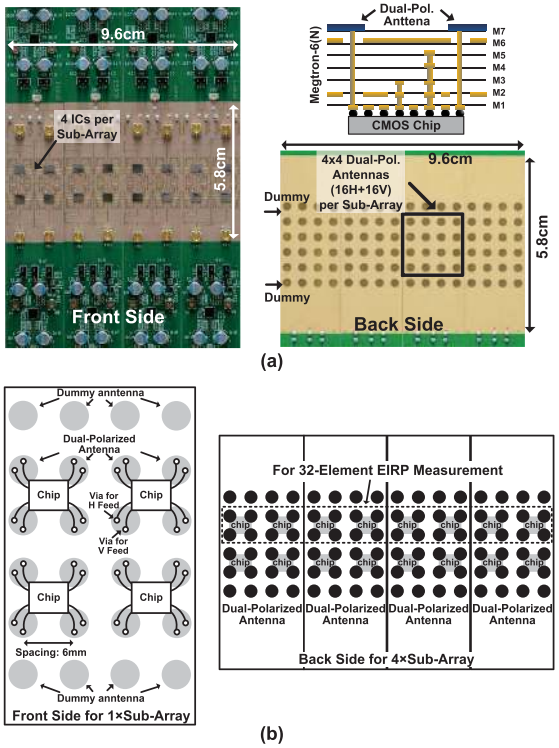


Fig. 21. (a) Photograph of transceiver module for OTA measurement and (b) connections between chips and dual-pol. antenna array.

To evaluate the over-the-air (OTA) performance of the proposed bi-directional beamformer, the fabricated chips are implemented into phased-array transceiver modules. Fig. 21(a) shows the module photograph and Fig. 21(b) further explains the connection between the chips and the dual-pol. antenna array. In this work, each sub-array module printed circuit board (PCB) shown in the figure has four chips on the front and a 4×4 dual-polarized array antenna on the back. Each antenna element has H and V ports for dual-polarized excitation. Each chip has eight RF-signal ports and is connected to the 2×2 array of the 4×4. The cross section view of the PCB is also shown in Fig. 21(a). Seven-layer metals are utilized for the module, and the RF ports are connected to the antennas through the vias. Multiple 4×4 sub-array module PCBs in this work can be combined side by side to make a larger array such as 8×4. The dual-pol. antenna and PCB are designed carefully considering the isolation between H- and V-polarization. The simulated antenna gain including the feed loss is 4 dB at 28 GHz. Fig. 22 shows the measured

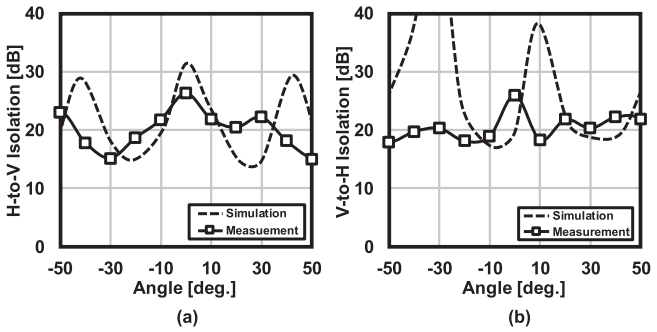


Fig. 22. Simulated and measured (a) H-to-V isolation and (b) V-to-H isolation for proposed dual-polarized antenna in azimuth plane.

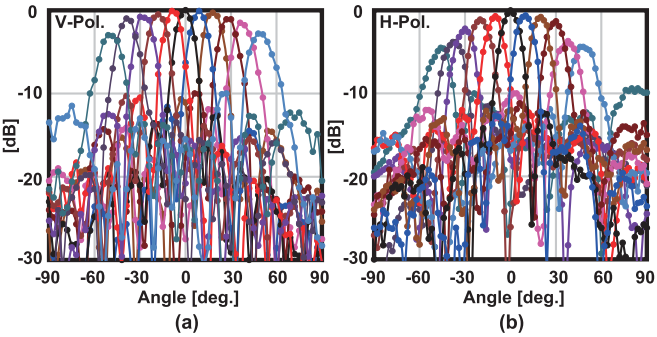


Fig. 23. Measured (a) V-polarization and (b) H-polarization beam patterns for two sub-array modules.

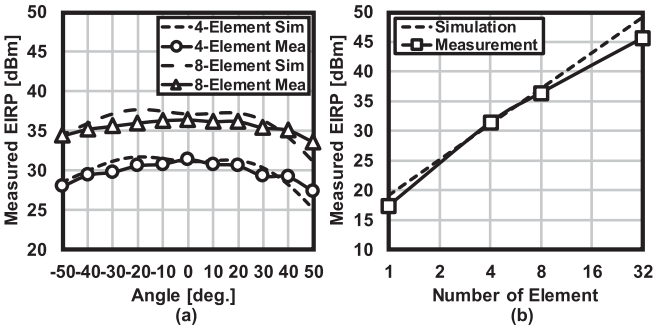


Fig. 24. (a) Measured saturated EIRP within scan angle from $-50°$ to $+50°$ and (b) measured saturated EIRP against element number at 0°.

cross-pol. isolations. Only one beamformer path is utilized for this measurement. Both H-to-V and V-to-H isolations are over 25 dB at 0°. Fig. 23 demonstrates the measured TX-mode beam patterns for two sub-array module PCBs in the azimuth plane. Fig. 23(a) shows the beam pattern for V-polarization and Fig. 23(b) shows the beam pattern for H-polarization. Beam scan range from $-50°$ to $+50°$ is covered by the proposed phased-array module. The measured sidelobe-levels are always lower than -11.4 dBc for V-polarization and -9.4 dBc for H-polarization. The measured saturated V-pol. EIRPs within the beam scan angle from $-50°$ to $+50°$ are summarized in Fig. 24(a) and the measured V-pol. EIRP against the element number is plotted in Fig. 24(b). External dividers are included in this measurement and an external amplifier is utilized for compensating the dividing loss. At 0°, the achieved EIRPs are 36.4 dBm for 2×4 elements and 31.4 dBm for 2×2

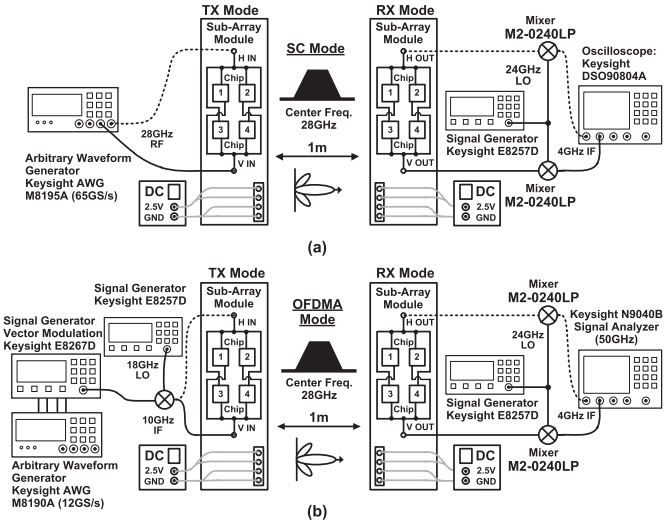


Fig. 25. Equipment setups for the 1-m OTA measurement: (a) SC mode and (b) 5G NR OFDMA mode.

TABLE II
POWER CONSUMPTION OF BLOCKS

	Sub Blocks	Power Consumption [mW]
TX-Mode	PA	149.0
	RF Buf.	42.5
	Bi-Dir. Phase Shifter	21.8
	Isolation Buf.	38.8
RX-Mode	LNA	31.3
	RF Buf.	30.0
	Bi-Dir. Phase Shifter	25.0
	Isolation Buf.	26.0

elements. A maximum saturated EIRP of 45.6 dBm is achieved by this work with 2×16 TX-mode element beamformers.

A 1-m OTA data transmission measurement is further carried on from TX to RX in this work. Fig. 25(a) demonstrates the equipment setup for SC-mode transmission. Two sub-array module PCBs are utilized in this measurement. One is operating in TX mode, while the other one is operating in RX mode. The modulated signals in QPSK, 16-QAM, 64-QAM, and 256-QAM with a center frequency of 28 GHz are directly generated by an arbitrary waveform generator (AWG). For TX-to-RX EVM measurement, the RX-mode sub-array module PCB is used. While, for TX EVM and constellation measurements, a 14-dBi horn antenna is utilized instead. After receiving, the combined signal is down-converted to low frequency by an external mixer. The EVMs and constellations are evaluated by the oscilloscope. The communication distance in this work is limited by the size of the chamber. The TX-to-RX EVMs are optimized considering the TX power backoff and RX SNDR. Fig. 26 summarizes the measured SC-mode performance with the setup mentioned above. At 0° scan, the measured maximum V-pol. data rates are 6 Gb/s in QPSK, 12 Gb/s in 16-QAM, 15 Gb/s in 64-QAM, and 6.4 Gb/s in 256-QAM. The achieved

TABLE III
PERFORMANCE COMPARISON OF 28-GHz PHASED-ARRAY TRANSCEIVERS

		This work		IBM [1]	Qualcomm [3]	UCSD [2]	UCSD [10]
Process		65nm CMOS		0.13μm SiGe	28nm CMOS	0.18μm SiGe	0.18μm SiGe
Polarization		Dual-pol.		Dual-pol.	Dual-pol.	Dual-pol.	Single-pol.
Carrier Freq.		28GHz (n257)		28GHz	28GHz (n257)	29GHz	28GHz
TX P1dB/path		11.3dBm		14.0dBm	12.0dBm	12.0dBm	10.5dBm
TX Psat/path		15.1dBm		16.4dBm	14.0dBm	N/A	12.5dBm
EIRP@Psat		45.6dBm 32 elements		54dBm 64 elements	35dBm 8 elements	26.5dBm@P_{1dB} 4 elements	45.0dBm 32 elements
RX NF		4.2∼5.0dB***		6.0dB	4.4∼4.7dB	4.8dB	4.6dB
Integration/chip		4×H-Beamformer, 4×V-Beamformer		16×H-TRX, 16×V-TRX, IF, LO (w/o PLL)	24×TRX, IF, LO	4×H-Beamformer, 4×V-Beamformer	4×Beamformer
PDC/path		TX: 252mW @11.3dBm/path RX:112mW		TX: 319mW @16.4dBm/path RX: 206mW	TX: 119mW @11.0dBm/path RX: 42mW	TX: 220mW RX: 150mW	TX: 200mW @10.5dBm/path RX: 130mW
Area/path		0.58mm^2 (4-stage PA, 4-stage LNA, PS		2.55mm^{2**} (4-stage PA, 3-stage LNA, PS)	0.68mm^{2**} (3-stage PA, 2-stage LNA, PS)	1.62mm^{2**} (3-stage PA, 3-stage LNA, PS)	1.79mm^{2**} (2-stage PA, 3-stage LNA, PS)
RMS Gain Error		0.2dB@28GHz		Gain var. < 1.5dB	N/A	0.6dB	< 0.8dB
RMS Phase Error		0.4°@28GHz		< 1°@28GHz	N/A	< 4°	< 6°
SC. Meas.	**Constellation**	64-QAM	256-QAM	N/A	N/A	64-QAM	16-QAM
	Data Rate	15Gb/s 2.5GBaud/s (SISO)	6.4Gb/s 0.8GBaud/s (SISO)	N/A	N/A	12Gb/s+12Gb/s 2G+2GBaud/s (DP-MIMO)	6Gb/s 1.5GBaud/s (SISO)
5G NR Meas.	**Modulation Supported**	QPSK, 16-QAM, 64-QAM, 256-QAM OFDMA		N/A	QPSK, 16-QAM, 64-QAM OFDMA	N/A	64-QAM OFDMA****
	2×2 DP-MIMO	64-QAM 2×400MHz Uplink EVM=4.9%*		N/A	N/A	N/A	N/A

* Referred to the RMS magnitude of the constellation. ** Estimated from paper. *** 26.5∼29.5 GHz **** Verizon pre-5G waveform is used.

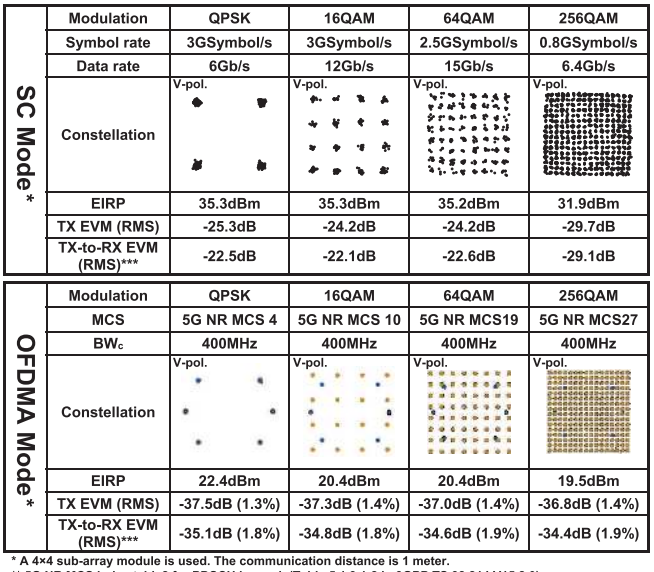
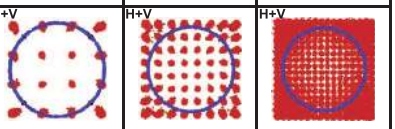


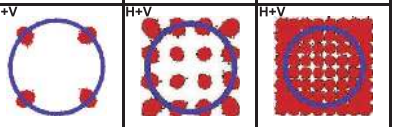
Fig. 26. Summarized SC-mode and OFDMA-mode constellations, TX EVMs, and TX-to-RX EVMs for sub-array transceiver module in 1-m OTA measurement.

corresponding TX EVMs and TX-to-RX EVMs are −25.3 dB and −22.5 dB for QPSK, −24.2 dB and −22.1 dB for 16-QAM, −24.2 dB and −22.6 dB for 64-QAM, −29.7 dB, and −29.1 dB for 256-QAM. For realizing a bit error rate of 10^{-3}, SC-mode TX-to-RX EVMs of −9.8 dB, −16.5 dB, −22.5 dB, and −28.4 dB are required for QPSK, 16-QAM, 64-QAM, and 256-QAM, respectively. Thus, all of the measured SC-mode EVMs meet the requirements for a bit error rate of less than 10^{-3}.

Fig. 25(b) shows the equipment setup for OFDMA-mode measurement. The input 5G NR downlink packets with 400-MHz channel bandwidth in QPSK, 16-QAM. 64-QAM and 256-QAM are generated with an AWG and a signal generator. While, at the RX side, a signal analyzer is used for evaluating the constellations and EVMs. The measured constellations, TX EVMs and TX-to-RX EVMs at 0° are also summarized in Fig. 26. Data transmissions of up to 256-QAM could be supported by this work. The measured TX EVMs are −37.5, −37.3, −37.0, and −36.8 dB for QPSK, 16-QAM, 64-QAM, and 256-QAM, respectively. The standard requirements for 5G OFDMA-mode TX EVM mentioned previously are satisfied in this measurement. The measured TX-to-RX EVMs are −35.1 dB for QPSK, −34.8 dB for 16-QAM, −34.6 dB for 64-QAM, and −34.4 dB for 256-QAM in this work.

The proposed sub-array module PCB is also evaluated in a 2×2 DP-MIMO configuration with 5G NR uplink signals in QPSK, 16-QAM, 64-QAM, and 256-QAM. Simultaneously, two-stream input signals with the same center frequency are generated from the Keysight AWG 8190A for the TX-mode module. While, the RX-mode module output signals are analyzed by the Keysight digitizer M9703B along with the Keysight 89600 VSA software (2018 U_1.0 BETA5). Fig. 27 summarizes the measured TX-to-RX constellations and EVMs. Due to the limitation of the measurement equipment, the

BW=100MHz*	Modulation	16QAM	64QAM	256QAM
	MCS	MCS 10	MCS 19	MCS 27
	TX-to-RX Constellation for DP-MIMO **			
	TX-to-RX EVM (RMS) for DP-MIMO	-31.4dB (2.7%)	-31.2dB (2.8%)	-31.1dB (2.8%)

BW=400MHz*	Modulation	QPSK	16QAM	64QAM
	MCS	MCS 4	MCS 10	MCS 19
	TX-to-RX Constellation for DP-MIMO **			
	TX-to-RX EVM (RMS) for DP-MIMO	-26.7dB (4.6%)	-26.2dB (4.9%)	-26.2dB (4.9%)

* A 4×4 sub-array module is used. Keysight digitizer M9703B & Keysight 89600 VSA software (2018_1.0 BETA5) are used for evaluation.
** H and V constellations are shown together.

Fig. 27. Summarized TX-to-RX EVMs and constellations for DP-MIMO operation.

constellations are shown together for H- and V-pol. streams. With 100-MHz channel bandwidth, TX-to-RX EVMs of −31.7, −31.2, and −31.1 dB are realized in 16-QAM, 64-QAM, and 256-QAM, respectively. With 400-MHz channel bandwidth, the measured TX-to-RX EVMs are −26.7 dB in QPSK, −26.2 dB in 16-QAM, and −26.2 dB in 256-QAM.

Table II shows the power consumption breakdown for the proposed phased-array beamformer. The measured power consumption in TX mode is 252 mW per path at an output power of 11.4 dBm. The measured RX-mode power consumption is 112 mW per path. Table III compares this work with state-of-the-art 28-GHz dual-pol. phased-array transceivers. This work based on the proposed neutralized bi-directional technique achieves 15.3-dBm TX-mode P_{sat} and 4.2-dB RX-mode NF with decent power consumption. The proposed sub-array module PCB is capable of scanning the beam from −50° to +50° for both H- and V-polarizations. The measured saturated EIRP for 32 TX-mode element-beamformers is 45.6 dBm. With 1-m distance, a maximum SC-mode data rate of 15 Gb/s in 64-QAM is achieved by the sub-array module PCB. 5G NR standard-compliant downlink packets of up to 256-QAM could be supported with 400-MHz channel bandwidth. The proposed 4H+4V beamformer chip reports a 2 × 2 DP-MIMO communication with 5G NR 64-QAM uplink signals. The data rate is improved for the future 5G NR with minimized system size and cost.

V. Conclusion

A 28-GHz CMOS 4H+4V phased-array beamformer chip supporting DP-MIMO for 5G NR is introduced in this article. Area-efficient neutralized bi-directional techniques are proposed for sharing the circuit chain between TX and RX modes. Two of the fabricated 16H+16V sub-array module PCBs are capable of scanning the beam from −50° to +50°. Within 1-m distance, a maximum SC-mode 64-QAM data rate of 15 Gb/s and the 256-QAM 5G NR OFDMA-mode downlink packets transmission are supported by the sub-array module PCB. This article also reports the first 2 × 2 DP-MIMO communication with standard-compliant 5G NR uplink signals. Remarkably improved data access speed is achieved for the next-generation mobile network with minimized system area, size, and cost.

References

[1] B. Sadhu *et al.*, "A 28-GHz 32-element TRX phased-array IC with concurrent dual-polarized operation and orthogonal phase and gain control for 5G communications," *IEEE J. Solid-State Circuits*, vol. 52, no. 12, pp. 3373–3391, Dec. 2017.

[2] K. Kibaroglu *et al.*, "A dual-polarized dual-beam 28 GHz beamformer chip demonstrating a 24 Gbps 64-QAM 2×2 MIMO link," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Jun. 2018, pp. 64–67.

[3] J. D. Dunworth *et al.*, "A 28GHz bulk-CMOS dual-polarization phased-array transceiver with 24 channels for 5G user and basestation equipment," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2018, pp. 70–72.

[4] S. Mondal *et al.*, "A 25–30 GHz fully-connected hybrid beamforming receiver for MIMO communication," *IEEE J. Solid-State Circuits*, vol. 53, no. 5, pp. 1275–1287, May 2018.

[5] S. Mondal, R. Singh, and J. Paramesh, "A reconfigurable bidirectional 28/37/39GHz front-end supporting MIMO-TDD, carrier aggregation TDD and FDD/full-duplex with self-interference cancellation in digital and fully connected hybrid beamformers," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2019, pp. 348–350.

[6] D. Dal Maistro *et al.*, "A 24.2-30.5GHz quad-channel RFIC for 5G communications including built-in test equipment," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Jun. 2019, pp. 283–286.

[7] Y. Yoon *et al.*, "A highly linear 28GHz 16-element phased-array receiver with wide gain control for 5G NR application," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Jun. 2019, pp. 287–290.

[8] M.-Y. Huang, T. Chi, F. Wang, T.-W. Li, and H. Wang, "A 23-to-30GHz hybrid beamforming MIMO receiver array with closed-loop multistage front-end beamformers for full-FoV dynamic and autonomous unknown signal tracking and blocker rejection," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2018, pp. 68–70.

[9] M. Y. Huang and H. Wang, "A 27-to-41GHz MIMO receiver with N-input-N-output using scalable cascadable autonomous array-based high-order spatial filters for instinctual full-FoV multi-blocker/signal management," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2019, pp. 346–348.

[10] K. Kibaroglu, M. Sayginer, and G. M. Rebeiz, "A low-cost scalable 32-element 28-GHz phased array transceiver for 5G communication links based on a 2×2 beamformer flip-chip unit cell," *IEEE J. Solid-State Circuits*, vol. 53, no. 5, pp. 1260–1274, May 2018.

[11] Y. Wang *et al.*, "A 39GHz 64-element phased-array CMOS transceiver with built-in calibration for large-array 5G NR," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Jun. 2019, pp. 279–282.

[12] J. Pang *et al.*, "A 28-GHz CMOS phased-array transceiver based on LO phase-shifting architecture with gain invariant phase tuning for 5G new radio," *IEEE J. Solid-State Circuits*, vol. 54, no. 5, pp. 1228–1242, May 2019.

[13] H.-T. Kim *et al.*, "A 28GHz CMOS direct conversion transceiver with packaged antenna arrays for 5G cellular system," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Jun. 2017, pp. 69–72.

[14] A. Nafe, M. Sayginer, K. Kibaroglu, and G. M. Rebeiz, "2×64 dual-polarized dual-beam single-aperture 28 GHz phased array with high cross-polarization rejection for 5G polarization MIMO," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2019, pp. 484–487.

[15] Y. Yin, S. Zihir, T. Kanar, and G. M. Rebeiz, "A 37-42 GHz 8×8 phased-array for 5G communication systems with 48-50 dBm EIRP," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2019, pp. 480–483.

[16] Y.-S. Yeh, E. Balboni, and B. Floyd, "A 28-GHz phased-array transceiver with series-fed dual-vector distributed beamforming," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Jun. 2017, pp. 65–68.

[17] J. Pang *et al.*, "A 28GHz CMOS phased-array beamformer utilizing neutralized bi-directional technique supporting dual-polarized MIMO for 5G NR," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2019, pp. 344–345.

[18] S. Shakib *et al.*, "A wideband 28GHz power amplifier supporting 8×100 MHz carrier aggregation for 5G in 40nm CMOS," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2017, pp. 44–45.

[19] Y. Zhang and P. Reynaert, "A high-efficiency linear power amplifier for 28GHz mobile communications in 40nm CMOS," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Jun. 2017, pp. 33–36.

[20] E. Cohen, M. Ruberto, M. Cohen, O. Degani, S. Ravid, and D. Ritter, "A CMOS bidirectional 32-element phased-array transceiver at 60 GHz with LTCC antenna," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 3, pp. 1359–1375, Mar. 2013.
[21] U. Kodak and G. M. Rebeiz, "Bi-directional flip-chip 28 GHz phased-array core-chip in 45nm CMOS SOI for high-efficiency high-linearity 5G systems," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Jun. 2017, pp. 61–64.
[22] W. Chan and J. R. Long, "A 58–65 GHz neutralized CMOS power amplifier with PAE above 10% at 1-V supply," *IEEE J. Solid-State Circuits*, vol. 45, no. 3, pp. 554–564, Mar. 2010.
[23] D. Zhao and P. Reynaert, "A 60-GHz dual-mode class AB power amplifier in 40-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 48, no. 10, pp. 2323–2337, Oct. 2013.
[24] E. Cohen, C. Jakobson, S. Ravid, and D. Ritter, "A bidirectional TX/RX four element phased-array at 60 GHz with RF-IF conversion block in 90nm CMOS process," in *Proc. IEEE Radio Freq. Integr. Circuits Symp.*, Jun. 2009, pp. 207–210.
[25] E. Cohen, C. G. Jakobson, S. Ravid, and D. Ritter, "A bidirectional TX/RX four-element phased array at 60 GHz with RF-IF conversion block in 90-nm CMOS process," *IEEE Trans. Microw. Theory Techn.*, vol. 58, no. 5, pp. 1438–1446, May 2010.
[26] M. Elkholy, S. Shakib, J. Dunworth, V. Aparin, and K. Entesari, "Low-loss highly linear integrated passive phase shifters for 5G front ends on bulk CMOS," *IEEE Trans. Microw. Theory Techn.*, vol. 66, no. 10, pp. 4563–4575, Oct. 2018.
[27] Y. Tousi and A. Valdes-Garcia, "A ka-band digitally-controlled phase shifter with sub-degree phase precision," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, May 2016, pp. 356–359.
[28] Q. Zheng *et al.*, "Design and performance of a wideband ka-band 5-b MMIC phase shifter," *IEEE Microw. Wireless Compon. Lett.*, vol. 27, no. 5, pp. 482–484, May 2017.
[29] P. Gu and D. Zhao, "Ka-band CMOS 360° reflective-type phase shifter with ±0.2 dB insertion loss variation using triple-resonating load and dual-voltage control techniques," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Jun. 2018, pp. 140–143.
[30] T. Wu *et al.*, "A 20~43 GHz VGA with 21.5 dB gain tuning range and low phase variation for 5G communications in 65-nm CMOS," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Jun. 2019, pp. 71–74.
[31] J. Pang *et al.*, "A 50.1-Gb/s 60-GHz CMOS transceiver for IEEE 802.11ay with calibration of LO feedthrough and I/Q imbalance," *IEEE J. Solid-State Circuits*, vol. 54, no. 5, pp. 1375–1390, May 2019.
[32] *Technical Specification 38.214 (V15.2.0) Physical Layer Procedures for Data*, document 38.214, 3GPP, Jun. 2018.
[33] *Technical Specification 38.104 (V15.2.0) Base Station (BS) Radio Transmission and Reception*, document 38.104, 3GPP, Jun. 2018.
[34] Y. Gong, M.-K. Cho, I. Song, and J. D. Cressler, "A 28-GHz switchless, SiGe bidirectional amplifier using neutralized common-emitter differential pair," *IEEE Microw. Wireless Compon. Lett.*, vol. 28, no. 8, pp. 717–719, Aug. 2018.
[35] J. Kaukovuori, K. Stadius, J. Ryynanen, and K. Halonen, "Analysis and design of passive polyphase filters," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 55, no. 10, pp. 3023–3037, Nov. 2008.
[36] S. Shakib, M. Elkholy, J. Dunworth, V. Aparin, and K. Entesari, "A wideband 28-GHz transmit–receive front-end for 5G handset phased arrays in 40-nm CMOS," *IEEE Trans. Microw. Theory Techn.*, vol. 67, no. 7, pp. 2946–2963, Jul. 2019.

Jian Pang (Member, IEEE) received the bachelor's and master's degrees from Southeast University, Nanjing, China, in 2012 and 2014, respectively, and the Ph.D. degree from the Department of Physical Electronics, Tokyo Institute of Technology, Tokyo, Japan, in 2019.

He is currently a Researcher with the Tokyo Institute of Technology, focusing on 5G millimeter-wave systems. His current research interests include high-data-rate low-cost millimeter-wave transceivers, power-efficient power amplifiers for 5G mobile system, MIMO, and mixed-signal calibration systems.

Dr. Pang was a recipient of the IEEE SSCS Student Travel Grant Award in 2016, the IEEE SSCS Predoctoral Achievement Award for 2018–2019, and the Seiichi Tejima Oversea Student Research Award in 2020. He serves as a reviewer for the IEEE JOURNAL OF SOLID-STATE CIRCUITS, the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES, the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I & II, and the IEEE MICROWAVE AND WIRELESS COMPONENTS LETTERS.

Zheng Li (Student Member, IEEE) received the B.E. and M.E. degrees in microelectronics and solid electronics from Xidian University, Xi'an, China, in 2014 and 2017, respectively. He is currently pursuing Ph.D. degree in electrical and electronic engineering with the Tokyo Institute of Technology, Tokyo, Japan, with a focus on 5G RF front-end and system design.

His current research interests include millimeter-wave CMOS wireless transceiver and 5G mobile system.

Ryo Kubozoe received the B.E. degree in electrical engineering from the Kochi University of Technology, Kochi, Japan, in 2017, and the M.E. degree in electrical and electronic engineering from the Tokyo Institute of Technology, Tokyo, Japan, in 2019.

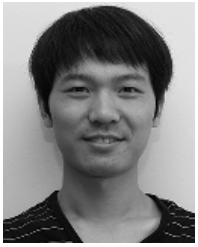
He is currently working for Panasonic Corporation, Osaka, Japan.

Xueting Luo received the B.E. and M.E. degrees in electrical engineering from the Tokyo Institute of Technology, Tokyo, Japan, in 2018 and 2020, respectively.

She is currently working for Sandisk Limited, Yokohama, Japan.

Rui Wu (Member, IEEE) received the B.S. and M.S. degrees from the University of Electronic Science and Technology of China, Chengdu, China, in 2006 and 2009, respectively, and the Ph.D. degree from the Tokyo Institute of Technology, Tokyo, Japan, in 2015.

From 2015 to 2018, he was a Post-Doctoral Researcher with the Tokyo Institute of Technology. Since 2018, he has been a full Professor with the National Key Lab of Microwave Imaging Technology, Institute of Electronics, Chinese Academy of Sciences, Beijing, China. His current research interests include RF/millimeter-wave transceivers for radar and high data-rate wireless communications.



Yun Wang (Student Member, IEEE) received the B.S. and M.S. degrees from the University of Electronic Science and Technology of China, Chengdu, China, in 2011 and 2014, respectively, and the Ph.D. degree in physical electronics from the Tokyo Institute of Technology, Tokyo, Japan, in 2019.

He was an Intern with the Pohang University of Science and Technology, Pohang, South Korea, in 2013, and Device Technology Laboratories, NTT Corporation, Atsugi, Japan, in 2016. He is currently a Post-Doctoral Researcher with the Tokyo Institute of Technology. His research interests include CMOS radio frequency (RF)/millimeter-wave wireless systems, 5G phased-array mobile system, and satellite communication.

Dr. Wang was a recipient of the China Government Scholarship (CSC) in 2014, and the winner of IEICE Best Paper Award in 2018 and the Best Student Paper Award (1st Place) at the 2019 IEEE Radio Frequency Integrated Circuits Symposium (RFIC). He serves as a reviewer for the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I, and the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES.

Dongwon You (Student Member, IEEE) received the B.S. degree in electrical and computer engineering from Ajou University, Suwon, South Korea, in 2017, and the M.S. degree in electrical and electronic engineering from the Tokyo Institute of Technology, Tokyo, Japan, in 2019. He is currently pursuing the Ph.D. degree in the electrical and electronic engineering with the Tokyo Institute of Technology, Tokyo, Japan.

His current research interests include CMOS Analog/RF/Millimeter-wave transceiver systems, MIMO, mixed-signal, wireless communication, device modeling.

Ashbir Aviat Fadila received the B.S. degree in electrical engineering from Institut Teknologi Bandung, Bandung, Indonesia, in 2015, and the M.S. degree in electrical and electronic engineering from the Tokyo Institute of Technology, Tokyo, Japan, in 2020, where he is currently pursuing the Ph.D. degree.

From 2015 to 2016, he was a Standard Cells Mask Layout Engineer with Marvell Technology Indonesia, Jakarta, Indonesia. From 2016 to 2017, he was a Research Assistant with Institut Teknologi Bandung, research SoC for IoT application. His current research interests include analog-mixed signal, data converter, and synthesizable analog circuit.

Rattanan Saengchan received the B.E. degree in electrical engineering from Chulalongkorn University, Bangkok, Thailand, in 2016, and the M.S. degree in electrical and electronic engineering from the Tokyo Institute of Technology, Tokyo, Japan, in 2020.

From 2016 to 2017, He was with Cypress Semiconductor, Bangkok, Thailand. He is currently with Renesas Electronics Corporation, Tokyo.

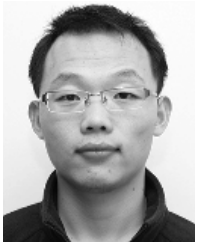
Takeshi Nakamura received the B.E. degree from the Department of Electrical and Electronic Engineering, Tokyo Institute of Technology, Tokyo, Japan, in 2018, where he is currently pursuing the M.E. degree.

In 2019, he was an Intern with imec, Leuven, Belgium.

Joshua Alvin received the B.E. degree in electrical and electronic engineering from the Tokyo Institute of Technology, Tokyo, Japan, in 2019, where he is currently pursuing the master's degree in electrical and electronic engineering.

Daiki Matsumoto received the B.E. degree in electrical engineering and the M.S. degree in electrical and electronic engineering from the Tokyo University of Science, Tokyo, Japan, in 2017, and 2019, respectively.

He is currently working for Renesas Electronics Corporation, Tokyo, Japan.

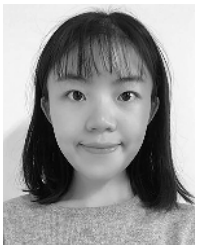


Bangan Liu (Student Member, IEEE) received the bachelor's degree from Northwestern Polytechnical University, Xian, China, in 2011, the master's degree from the University of Science and Technology of China, Hefei, China, in 2014, and the Ph.D. degree from the Tokyo Institute of Technology, Tokyo, Japan, in 2019, respectively.

His main research field includes digital phase-locked loops (PLL), fully synthesizable analog/RF circuits, and digital-intensive/digitally assisted mixed-signal systems.

Aravind Tharayil Narayanan (Senior Member, IEEE) received the B.Tech. degree in electronics and communication engineering from Calicut University, Kerala, India, in 2003, the M.S. degree in very large scale integration (VLSI)-CAD from Manipal University, Manipal, India, in 2009, and the Ph.D. degree from the Tokyo Institute of Technology, Tokyo, Japan, in 2016.

He is currently a Researcher with Ericsson AB, Lund, Sweden. His research interests include data converters, frequency generation and recovery, high-purity oscillator design, and mixed-signal design.



Junjun Qiu (Student Member, IEEE) received the B.Sc. degree in electrical and electronic engineering from the East China University of Science and Technology, Shanghai, China, in 2016, the M.E. degree in electrical and electronic engineering from Tokyo Institute of Technology, Tokyo, Japan, in 2018. She is currently pursuing the Ph.D. degree in electrical and electronic engineering with the Tokyo Institute of Technology, Tokyo, Japan.

She was focusing on fully synthesizable digital baseband circuit design for subgigahertz wireless transceiver system. Her current research interests include high performance phase locked loop design and mixed signal wireless communication system design for Bluetooth low energy.

Ms. Qiu was a recipient of the IEEE SSCS Student Travel Grant Award in 2020.

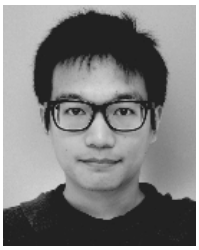
Hanli Liu (Member, IEEE) received the B.S. degree from the University of Electronic Science and Technology of China, Chengdu, China, in 2013, and the M.S. and Ph.D. degrees from the Tokyo Institute of Technology, Tokyo, Japan, in 2015 and 2018, respectively.

He was an Intern with Mixed-Signal IC Group, Toshiba Cooperate Research and Development Center, Kawasaki, Japan, from January to April 2017, working on digital PLL architectures. His research interests include ultra-low-power wireless transceivers for Bluetooth low energy, low-power low-jitter digital PLLs, and ultra-low-jitter PLLs for 5G cellular, high FOM oscillators.

Dr. Liu is a winner of the SSCS Predoctoral Achievement Award 2017–2018. He serves as a Reviewer for the IEEE JOURNAL OF SOLID-STATE CIRCUITS and the IEEE TRANSACTIONS ON VLSI SYSTEMS.

Zheng Sun (Student Member, IEEE) received the B.S. degree in information engineering from Southeast University, Nanjing, China, in 2014, and the M.S. degree in information, production and systems engineering from Waseda University, Tokyo, Japan, in 2015. He is currently pursuing the Ph.D. degree in electrical and electronic engineering from the Tokyo Institute of Technology, Tokyo.

He is/was involved in low-power RF, mixed-signal and digital PLL designs. His current interests include transceivers for Bluetooth Low Energy, *LC*-VCO for IoT applications, and harmonic suppression techniques for the power amplifier.



Hongye Huang (Student Member, IEEE) was born in Guilin, China, in 1994. He received the B.E. degree from the University of Electronic Science and Technology of China, Chengdu, China, in 2016, and the M.E. degree from the Tokyo Institute of Technology, Tokyo, Japan, in 2018, where he is currently pursuing the Ph.D. degree.

His current research interests include mixed-signal integrated circuits and frequency synthesizers.

Mr. Huang is a Scholarship Recipient of Watanuki International Scholarship Foundation in the fiscal year 2020.

Korkut Kaan Tokgoz (Member, IEEE) received the B.S. degree in microwave and antenna theory and telecommunications and the M.S. degree in electromagnetics from the Electrical and Electronics Engineering Department, Middle East Technical University, Ankara, Turkey, in 2009 and 2012, respectively, and the M.E. and Ph.D. degrees from the Department of Physical Electronics, Tokyo Institute of Technology, Tokyo, Japan, in 2014 and 2018, respectively.

From 2009 to 2012, he worked as a Teaching and Research Assistant with Middle East Technical University, where he was involved in RF MEMS, surface micromachined lumped components, and ultra-wideband RF phase shifters. From 2014 to 2018, he worked as a Research Assistant with the Tokyo Institute of Technology, focused on millimeter-wave and sub-terahertz circuits and systems. From 2018 to 2019, he worked as a Senior Researcher and an Assistant Manager with NEC Corporation, Kanagawa, Japan, where he was involved in 5G systems, high-power high-efficiency power amplifiers, and fixed point-to-point wireless links. He is currently working as an Assistant Professor with the Tokyo Institute of Technology. His current research interests include low power Edge-AI for monitoring systems, the IoT, sensors and systems, de-embedding, device characterization, analog/RF/millimeter-wave/sub-terahertz transceivers for wireless communications, and high-power, high-efficiency PAs for wireless systems.

Dr. Tokgoz was a recipient of several awards and scholarships, including the SSCS Predoctoral Achievement Award, in 2018, the IEEE MTT-S Graduate Student Fellowship, in 2017, the IEICE Student Encouragement Prize, in 2017, the Seiichi Tejima Overseas Student Research Award, and the IEEE/ACM ASP-DAC University LSI Design Contest 2017 Best Design Award.

Keiichi Motoi (Member, IEEE) received the B.S. and M.S. degrees in physics from Keio University, Yokohama, Japan, in 2008 and 2010, respectively.

In 2010, he joined NEC Corporation, where he has been engaged in the research and development of RF modules and RFIC circuits for wireless communication. His current interests include high-efficiency power amplifier architecture and IC/module implementation for mobile base stations and multi-mode/multi-band transceiver ICs for software-defined-radio systems.

Mr. Motoi is a member of the Institute of Electronics, Information, and Communication Engineers (IEICE), Japan.

Naoki Oshima received the B.E. and M.E. degrees in electrical engineering from Doshisha University, Kyoto, Japan, in 2006 and 2008, respectively.

In 2008, he joined NEC Corporation, Kawasaki, Japan, where he is currently with the System Platform Research Laboratories. His current research interests include RF circuit design for wireless communications, especially ultra-wideband and millimeter-wave applications.

Dr. Oshima is a member of the Institute of Electronics, Information and Communication Engineers, Japan.

Shinichi Hori (Member, IEEE) received the B.E. degree in mechanics and the M.E. degree in electronics from the University of Tokyo, Japan, in 1998 and 2000, respectively.

In 2000, he joined NEC Corporation, Kawasaki, Japan, where he has been engaged in the research and development of RF CMOS circuits for wireless communication. In 2008, he was a Visiting Scholar with Center for Integrated Systems, Stanford University, Stanford, CA, USA. His current interests include high- efficiency power amplifier architecture and IC/module implementation for mobile base stations, and multi-mode/multi-band transceiver ICs for software-defined-radio systems.

Mr. Hori is a member of Institute of Electronics, Information and Communication Engineers (IEICE), Japan.

Kazuaki Kunihiro (Member, IEEE) received the B.S. and M.S. degrees in applied physics from the Tokyo Institute of Technology, Tokyo, Japan, in 1988 and 1990, respectively, and the D.E. degree in quantum engineering from Nagoya University, Nagoya, Japan, in 2004.

In 1990, he joined the NEC Corporation, Kawasaki, Japan, where he has been engaged in device simulation, modeling, and circuit design of GaAs and GaN FETs for wireless communications. From 1995 to 1996, he was a Visiting Researcher with the Technical University of Berlin, Berlin, Germany, where he studied nonlinear modeling of III–V compound semiconductor devices. His current interests include the area of linear and energy-efficient transmitters and phased array antenna systems for 5G/B5G mobile infrastructures. He is currently a senior expert in Wireless Access Solutions Division in NEC Corporation.

Dr. Kunihiro is a member of the IEEE Microwave Theory and Techniques Society (IEEE MTT-S). He is also a member of the Institute of Electronics, Information and Communication Engineers (IEICE), Japan. From 2013 to 2015, he also served as a TPC Member of the IEEE Compound Semiconductor IC Symposium (CSICS). From 2006 to 2011, he was an Associate Editor of the *IEICE Journal*.

Tomoya Kaneko (Member, IEEE) received the B.S. degree in physics from the Tokyo University of Science, Tokyo, Japan, in 1984, and the M.S. degree in science from the University of Tsukuba, Tsukuba, Japan, in 1986, respectively.

He joined NEC Corporation, Kawasaki, Japan in 1986, where he has been engaged in design and development of MMICs, MCMs and sub-systems for radio communication systems. He is currently an Executive Specialist in Wireless Network Development Division of NEC Corporation. His current interests are millimeter-wave technologies and massive-MIMO considering their application to gNB.

Mr. Kaneko serves as a TPC Member and an Overseas Advisor for the IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS).

Atsushi Shirane (Member, IEEE) received the B.E. degree in electrical and electronic engineering and the M.E. and Ph.D. degrees in electronics and applied physics from the Tokyo Institute of Technology, Tokyo, Japan, in 2010, 2012, and 2015, respectively.

From 2015 to 2017, he was with Toshiba Corporation, Kawasaki, Japan, where he developed 802.11ax Wireless LAN RF transceiver. From 2017 to 2018, he was with Nidec Corporation, Kawasaki, where he researched intelligent motor with wireless communication. He is currently an Assistant Professor with the Department of Electrical and Electronic Engineering, Tokyo Institute of Technology. His current research interests include RF CMOS transceiver for IoT, 5G, and satellite communication.

Dr. Shirane is a member of the IEEE Solid-State Circuits Society, and the Institute of Electronics, Information and Communication Engineers (IEICE).

Kenichi Okada (Senior Member, IEEE) received the B.E., M.E., and Ph.D. degrees in communications and computer engineering from Kyoto University, Kyoto, Japan, in 1998, 2000, and 2003, respectively.

From 2000 to 2003, he was a Research Fellow of the Japan Society for the Promotion of Science with Kyoto University. In 2003, he joined the Tokyo Institute of Technology, Tokyo, Japan, as an Assistant Professor, where he is currently a Professor of electrical and electronic engineering. He has authored or coauthored more than 400 journal and conference articles. His current research interests include millimeter-wave CMOS wireless transceivers for 20/28/39/60/77/79/100/300GHz for 5G, WiGig, satellite and future wireless system, digital PLL, synthesizable PLL, atomic clock, and ultra-low-power wireless transceivers for Bluetooth low-energy, and subgigahertz applications.

Dr. Okada is a member of the Institute of Electrical and Electronics Engineers (IEEE), the Institute of Electronics, Information and Communication Engineers (IEICE), the Information Processing Society of Japan (IPSJ), and the Japan Society of Applied Physics (JSAP). He is/was a member of the technical program committees of IEEE International Solid-State Circuits Conference (ISSCC), VLSI Circuits Symposium, and European Solid-State Circuits Conference (ESSCIRC), Radio Frequency Integrated Circuits Symposium (RFIC). He was a recipient or co-recipient of the Ericsson Young Scientist Award in 2004, the A-SSCC Outstanding Design Award in 2006 and 2011, the ASP-DAC Special Feature Award in 2011 and Best Design Award in 2014 and 2015, the MEXT Young Scientists' Prize in 2011, the JSPS Prize in 2014, the Suematsu Yasuharu Award in 2015, the MEXT Prizes for Science and Technology in 2017, the RFIT Best Paper Award in 2017, the IEICE Best Paper Award in 2018, the RFIC Symposium Best Student Paper Award in 2019, the IEICE Achievement Award in 2019, the DOCOMO Mobile Science Award in 2019, and more than 40 other international and domestic awards. He is/was Guest Editors and an Associate Editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS (JSSC), an Associate Editor of the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES (T-MTT), a Distinguished Lecturer of the IEEE Solid-State Circuits Society (SSCS).