A 3.1–10.6 GHz Ultra-Wideband CMOS Low Noise Amplifier With Current-Reused Technique

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***Abstract*—A 3.1–10.6 GHz ultra-wideband (UWB) low noise amplifier (LNA) utilizing a current-reused technique and a simple high-pass input matching network is proposed. The implemented LNA presents a maximum power gain of 16 dB, and a good input matching of 50 Ω in the required band. An excellent noise figure (NF) of 3.1–6 dB was obtained in the frequency range of 3.1–10.6 GHz with a power dissipation of 11.9 mW under a 1.8-V power supply. The proposed UWB LNA demonstrates the highest power gain and lowest NF among the published works in 0.18-μm CMOS technology.**

***Index Terms*—Low noise amplifier (LNA), noise figure (NF), ultra-wideband (UWB).**

I. Introduction

SINCE the Federal Communications Commission (FCC) has allocated 7500-MHz bandwidth for ultra-wideband (UWB) applications in the 3.1–10.6 GHz frequency range [1], the related technologies have attracted much attention from both industry and academia. This new standard provides low cost, low complexity, low power consumption, high security, and high data-rate wireless communication capabilities, which can be used in wireless personal area network (WPAN), medical-image systems, and vehicular communications. The design of the front-end low noise amplifier (LNA) is one of the challenges in radio frequency (RF) receivers, which needs to provide a good input impedance match, a flat power gain, and a low noise figure (NF) within the required band. Recent advances in CMOS-based UWB LNA have shown good bandwidth and gain performance [2]–[4]. However, the observed lowest NF is ∼4 dB in 0.18-μm CMOS technology, which still needs to be improved.

In this study, a different wideband technique with a simple high-pass filter as the input matching network is adopted, and the current-reused structure proposed in narrow-band LNA design [5] has been successfully extended to UWB applications. In addition, the grounded-coplanar-waveguide (GCPW) structures are employed in the layout to further reduce the signal loss and undesired noise coupling. With these techniques, an UWB LNA implemented by standard 0.18-μm CMOS technology demonstrates an excellent NF as low as 3.1 dB with a large power gain of 16 dB while consuming only 11.9 mW.

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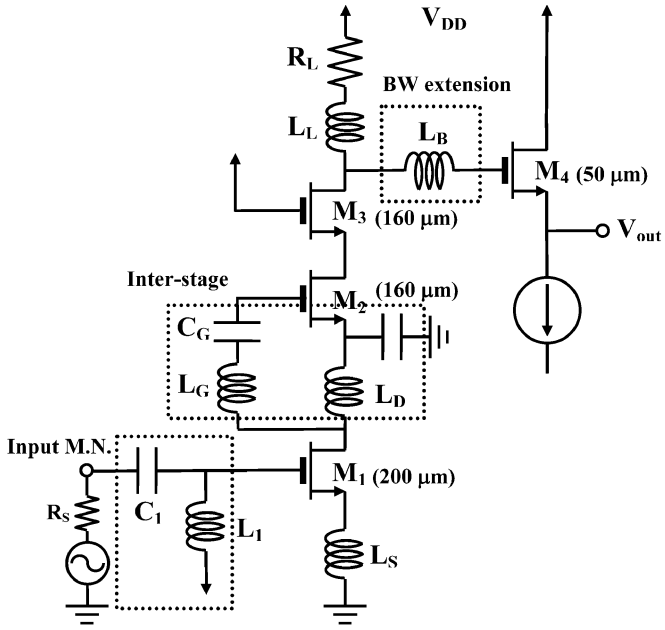

Fig. 1. Schematic of the proposed current-reused LNA.

II. Circuit Topology and Analysis

Fig. 1 shows the proposed CMOS UWB LNA utilizing the current-reused technique. As can be seen, the LC high-pass filter of C_1 (0.9 pF) and L_1 (1.8 nH) is employed as the input matching network, and the inter-stage network composed of the inductors L_G (0.5 nH), L_D (3.3 nH) and capacitor C_G (0.9 pF) performs a current-reused function to achieve high power gain. In addition, an inductor L_B (3.6 nH) is connected between the main circuit and the output buffer for further bandwidth extension due to a series LC resonance with the gate capacitance of M_4.

A. Current-Reused Technique

The current-reused configuration can be considered as a two-stage cascade amplifier, where the first stage is the CS amplifier (M_1), and the second stage is the cascode amplifier (M_2 and M_3) with an additional buffer stage (M_4) at the output. Note that M_3 is the common-gate stage of the cascode configuration, which eliminates Miller effect and provides a better isolation from the output return signal. The purpose of using L_G and C_G is to perform a series-resonant with $C_{\rm gs}$ of M_2 for a

low impedance path, while the impedance of L_D is adequately large in the desired bandwidth to provide a high impedance path to block the signal. The simulation results indicate that the current-reused function can work properly as L_D exceeds a certain value, and is not affected by the selection of C_G and L_G. As a consequence, the input signal can be amplified twice under this con-current structure.

Note that the resonate circuit composed of L_G and C_G presents a narrow-band characteristic. Therefore, the current-reused function is maximized at around the resonant frequency, which is designed to enhance the gain at the upper end of the desired band. In addition, R_L (50 Ω) and L_L (1.8 nH) are designed to have a peaking characteristic to compensate the high frequency gain roll-off of the devices. At the lower end of the desired band, as deviated from the resonant frequency, the effective current-reused amplification is degraded due to the increased impedance of the L_G-C_G path. However, combining with the higher intrinsic gain of the devices at lower frequencies (for example, a device with $W = 200$ μm has a S_{21} of 14.4 dB at 3 GHz, while that of 8.3 dB at 10 GHz from the foundry provided RF model), an overall wideband flat-gain response can be achieved.

B. Wideband Matching Design

As shown in Fig. 1, the LC high-pass filter is designed as the input matching stage for a wideband characteristic. The function of the LC network is twofold, one is to perform the filtering function to have the desired lower-end cutoff characteristic; the other is to satisfy the overall low input reflection coefficient within the bandwidth. The corner frequency of the LC filter is designed close to the lower cutoff frequency for the signal suppressing outside the UWB standard. On the other hand, the LC network combined with the source degenerated inductor L_S (0.5 nH) and the intrinsic capacitances of M_1 to form a multi-section LC ladder network for achieving a wideband matching characteristic to 50 Ω. Note that the impact of the interstage components on the input matching is not significant, since the inter-stage is isolated to the input characteristics through M_1 in the interested frequency range.

C. Design for Low NF

In the proposed LNA topology, both the simplified high-pass input matching network and the current-reused configuration are beneficial to the low noise design. Compared with [2], which adopted a band-pass LC filter for input match, the proposed high-pass filter with only one spiral inductor simplifies the circuit complexity and reduces the thermal noise generated from the parasitic resistance of additional inductors. As a result, an improved noise performance can be expected.

In addition, as mentioned, the current-reused amplifier functions as a two-stage cascade amplifier. The NF of the second stage contributed from both the MOSFETs (M_2 and M_3) and the inductors (L_G and L_D) can be reduced by the gain of the first stage. In addition, the NF originated from R_L, L_L, L_B, and M_4 is reduced twice by the gains of the first and second stages. With this design technique, not only can a high gain be obtained, but a low NF can also be achieved simultaneously.

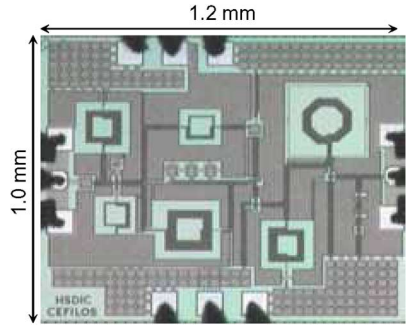

Fig. 2. Microphotograph of the proposed LNA.

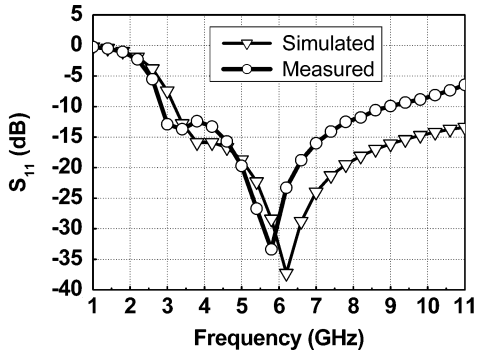

Fig. 3. Measured and simulated input reflection coefficients.

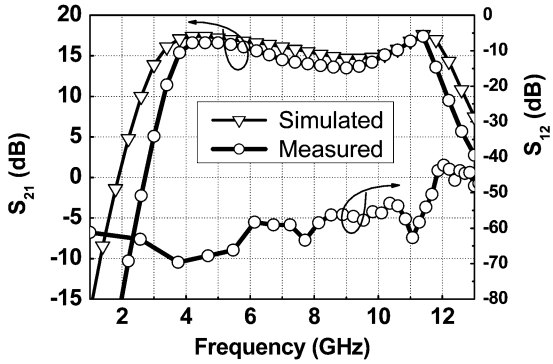

Fig. 4. Power gain and reverse isolation.

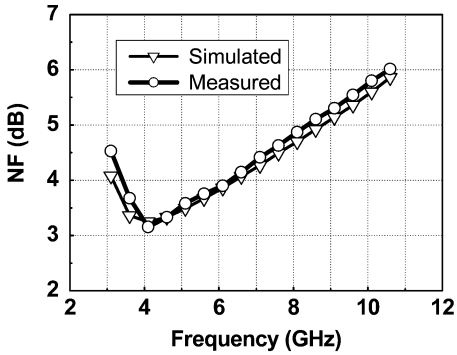

Fig. 5. Measured and simulated NFs.

D. Layout Consideration

The layout plays an important role in the overall circuit performance. Operating in such a high-frequency range, the signal can suffer from the lossy silicon substrate and the crosstalk from

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH PUBLISHED WORKS

Specification	*This work*	[2]	[3]	[4]	[8]	[9]
Technology	0.18-μm CMOS	0.18-μm CMOS	0.18-μm CMOS	0.18-μm CMOS	0.13-μm CMOS	0.18-μm SiGe HBT
Frequency (GHz)	3.1 — 10.6	3.1 — 10.6	3.1 — 10.6	3.1 — 10.6	3.1 — 10.6	3.1 — 10.6
Input return loss S_{11} (dB)	< −8	< −9	< −10	< −11	< −10	< −14
Supply voltage (V)	1.8	1.8	1.8	1.5	1.2	2.5
Power gain (dB)	13.5−16	9.2	8.5	10.8−12	13.7−16.5	16.4−18
Reverse isolation S_{12} (dB)	< −40	< −35			< −30	
Noise Figure (dB)	3.1−6	4−9	4.3−5.3	4.7−5.6	2.1−2.8	3.4−4.7
Bandwidth (GHz)	3.4−11.4	2.3−9.2	1.3−10.7	1−11.6	3.1−10.6	3−10
IIP3 @ 6GHz (dBm)	−7	−6.7	8	−11	−7	−11.7
P_{diss} (mW)	11.9	9.2	4.5	10.6	9	42.5
Chip Area	1.2 mm^2	1.1 mm^2	1.0 mm^2	0.66 mm^2	0.87 mm^2	0.53 mm^2

adjacent interconnects. In this design, the GCPW configuration of the transmission lines is employed, which has been demonstrated for microwave circuit applications in CMOS technology [6]. By completely isolating the lossy Si substrate with the metal one layer as the bottom ground plane, the via metals as the sidewall, and the metal six layer as the top ground plane, a reduced loss and crosstalk can be expected. Note that 50-Ω GCPW lines were designed and optimized by an EM simulation tool and used in the proposed LNA. The measured good noise performance suggests that the GCPW interconnect is suitable for low-noise applications.

III. MEASURED RESULTS

Fig. 2 shows the microphotograph of the fabricated LNA, and the chip area is 1.2 mm^2 (1 mm × 1.2 mm) including the probing pads (core area: 0.7 mm^2). The GCPW layout can be identified as a large ground metal plane on the top of the chip. Fig. 3 presents the measured and simulated input reflection coefficients. As can be seen, the well-matched S_{11} demonstrates a successful design of the simple LC high-pass filter as the input matching network. Fig. 4 shows the power gain and the reverse isolation. The power gain ranges from 13.5 to 16 dB, and the 3-dB bandwidth covers from 3.4 to 11 GHz and S_{12} is below −40 dB within the required bandwidth. Fig. 5 compares both the measured and simulated NFs. The result shows an excellent noise performance of 3.1–6 dB in a frequency range of 3.1 to 10.6 GHz. Note that an additional noise source of the induced gate-noise is employed for a more complete noise model [7]. Table I summarizes the performance of recently published UWB LNAs by standard 0.18-μm CMOS, 0.13-μm CMOS, and 0.18-μm SiGe HBT technologies [8], [9]. As can be seen, similar power gain was obtained by this work compared with those from more advanced technologies. Although the NF is not the lowest, the result obtained is still the best among the published LNAs in 0.18-μm CMOS technology.

IV. CONCLUSION

The feasibility of a newly proposed wideband matching topology and current-reused technique for improving noise performance, achieving good input matching and high power gain has been demonstrated in this letter. The proposed LNA provided a peak power gain of 16 dB within the 3-dB bandwidth of about 8 GHz and a good input matching under a power dissipation of 11.9 mW. NF ranged from 3.1 to 6 dB within the bandwidth, which is the best result reported among the published UWB LNAs in 0.18-μm CMOS technology.

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