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A 3.1-GHz Class-F Power Amplifier With 82% Power-Added-Efficiency

Kenle Chen
Birck Nanotechnology Center, Purdue University, chen314@purdue.edu

Dimitrios Peroulis
Birck Nanotechnology Center, Purdue University, dperouli@purdue.edu

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A 3.1-GHz Class-F Power Amplifier With 82% Power-Added-Efficiency

Kenle Chen, *Student Member, IEEE*, and Dimitrios Peroulis, *Member, IEEE*

***Abstract*—This letter presents the first high-frequency, multi-harmonic-controlled (> 3), Class-F power amplifier (PA) implemented with a packaged GaN transistor. For PA design at high frequencies, parasitics of a packaged transistor significantly increase the difficulty of harmonic manipulation, compared to low-frequency cases. To overcome this issue, we propose a novel design methodology based on a three-stage, low-pass, output matching network, which is realized with transmission lines. This network provides optimal fundamental impedance and allows harmonic control up to the fourth order to enable an efficient Class-F behavior. The implemented PA exhibits a state-of-the-art performance at 3.1 GHz with a 82% PAE, 15 dB gain, and 10 W output power, indicating a clear advantage of this method over the conventional ones with extra parasitic compensators.**

***Index Terms*—Class-F, efficiency, GaN, high frequency, lowpass matching network, parasitics.**

I. Introduction

POWER amplifiers are required to operate efficiently at higher frequencies as wireless communication standards keep evolving [1]. High-efficiency PAs are normally realized by decreasing the overlap between transient current and voltage at the drain node. They can be categorized into two basic families based on whether they are designed in time or frequency domains: a) switch mode and b) harmonic-tuned mode. For a high operation frequency, typically >2 GHz, harmonic-tuned PAs, e.g., Class-F and inverse Class-F, have been the leading candidates, due to their higher gain/power, better linearizability, and no inherent frequency limitations typically found in their switch-mode counterparts.

To maximize the efficiency using a harmonic-tuned topology, it requires precise manipulation of harmonic terminations beyond the third order [1]. Also, transistor parasitics need to be carefully considered, whose impact on PA design grows with frequency and power. In a typical Class-F/F^{-1} PA design [1]–[4], parasitic compensation unit and harmonic control circuit (HCC) are utilized, which are complicated and not straightforward. In particular, this may lead to inaccuracies in high-frequency designs using packaged devices and with harmonic control above the third harmonic [1].

In this research, a novel systematical method for designing multi-harmonic-tuned Class-F PA is developed. The output circuit is based on a high-order ($n = 6$), transmission-line-implemented, low-pass filter, thus requiring no specific parasitic compensator and HCC. By well synthesizing this filter-matching network, it is capable of loading the packaged GaN transistor with optimal fundamental impedance, as well as harmonic impedances up to the fourth order. Following the proposed methodology, a highly efficient Class-F PA is realized with measured performance of 82% PAE and 10 W power at 3.1 GHz. To the authors' best knowledge, the achieved PAE is the highest reported at this frequency and for this power level with a Class-F/F^{-1} operation.

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The authors are with the School of Electrical and Computer Engineering and Birck Nano Technology Center, Purdue University, West Lafayette, IN 47906 USA (e-mail: chen314@purdue.edu; dperouli@purdue.edu).

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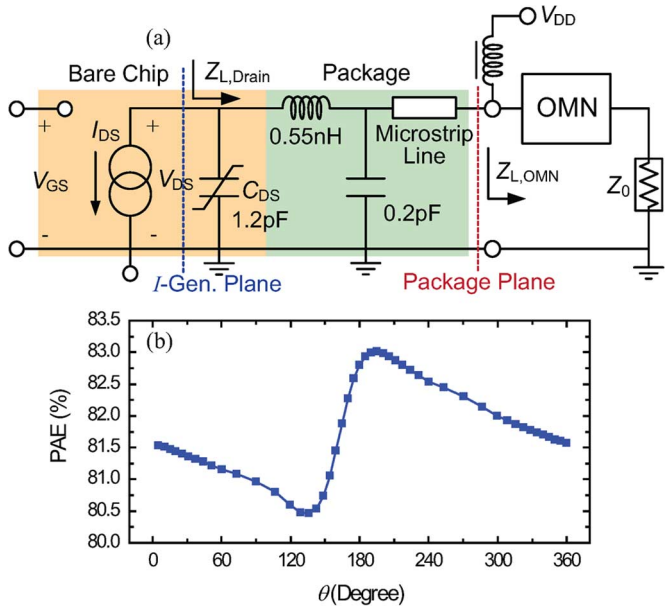

Fig. 1. (a) Illustrative PA schematic with the equivalent-circuit model of CGH40010F. (b) Simulated PAE versus phase of the unity-magnitude fourth-harmonic reflection coefficient.

II. Design Methodology

A. Transistor Modeling

A 10 W GaN HEMT device, Cree CGH40010F, is used in this PA design. It consists a bare GaN chip of CGH60015DE and the respective package. The equivalent circuit model of this packaged transistor is plotted in Fig. 1(a), showing the parasitic components and their values. The modeling is conducted using a combination of the bare-chip model and the package model, which are both supplied by the manufacturer. In an actual PA design, the parasitic network needs to be carefully treated because the output matching network is directly connected to the package, as shown in Fig. 1(a).

In this PA design, the harmonic manipulation is performed up to the fourth order. The effect of the fourth harmonic impedance on PA efficiency is extracted from load-pull simulation, in which optimized Class-F terminations have already been set at $f_0, 2f_0,$

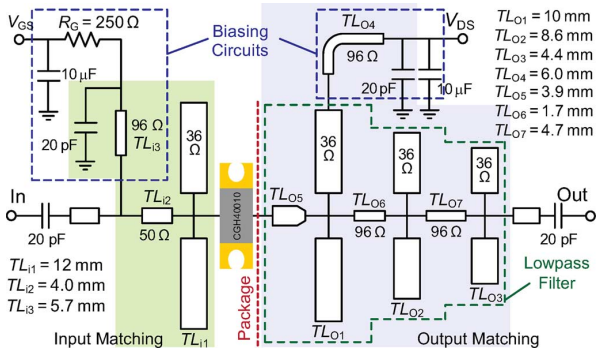

Fig. 2. Circuit schematic of the Class-F PA with relevant dimensions (implementation on Rogers Duroid 5880).

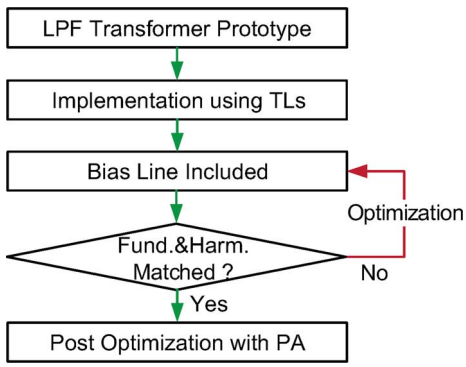

Fig. 3. Procedure for designing the output matching network.

and $3f_0$. Fig. 1(b) shows the PAE versus the phase variation of the fourth harmonic reflection coefficient, indicating a $\approx 3\%$ of PAE difference when it passes through the short-circuit point. It underlines that a proper loading of the fourth harmonic is necessary.

B. Class-F PA Design

Recently, multi-stage low-pass filter-matching-networks have been extensively utilized for realizing broadband high-efficiency PAs [5], [6]. In such designs, the fundamental and harmonic matchings are performed with the filter's pass-band and stop-band, respectively. If applying this lowpass network to a narrowband design, there can be sufficient degrees of freedom for conducting accurate multi-harmonic control in order to result in a high-efficiency operation around a single frequency. In this design, the output matching of the Class-F PA is performed using a three-stage lowpass topology, because it yields a good trade-off between design freedom, stop-band attenuation, and insertion loss [5]. Fig. 2 shows the entire circuit schematic of the PA, including input and output matching circuits.

The flow chart of designing and realizing the output matching network is illustrated in Fig. 3. It mainly takes four stages. First, a three-stage lowpass-filter (LPF) transformer prototype is extracted, modified (from real-to-real to real-to-complex), and scaled using the approach presented in [5]. Second, this determined prototype is implemented using respective transmission lines (TLs). Specifically, the capacitors are replaced by low-impedance open-circuit stubs, and inductors by high-impedance short TLs, as shown in Fig. 2. The load impedance at the I-generation plane $(Z_{\mathrm{L,Drain}})$ is obtained by connecting the parasitic network to the OMN, as shown

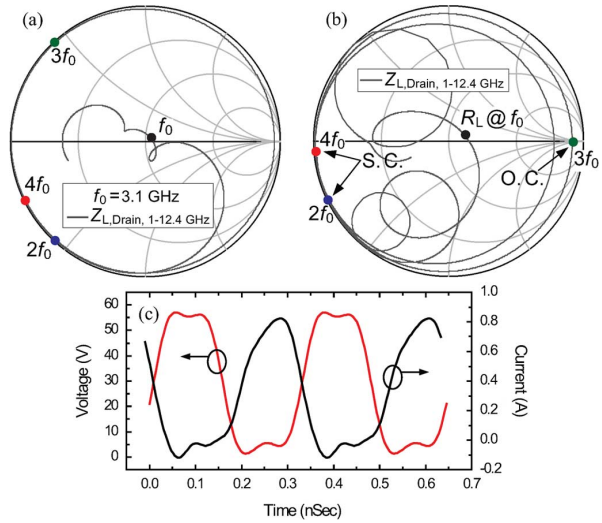

Fig. 4. Impedance of the entire output circuit $(\mathrm{parasitics} + \mathrm{OMN})$, representing $Z_{\mathrm{L,Drain}}$: (a) initial 3-stage lowpass network, (b) bias line included. (c) Simulated waveforms of voltage and current at the intrinsic-drain plane.

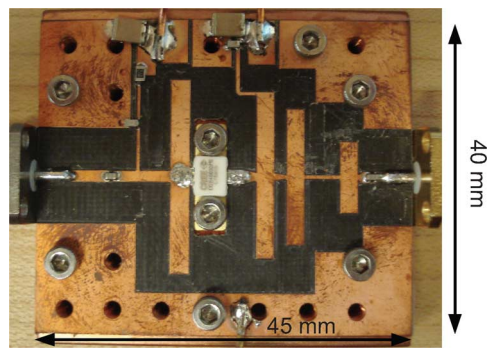

Fig. 5. Fabricated PA circuit.

in Fig. 4(a). Third, a high-impedance, short-ended bias-line with properly selected length is connected to the implemented lowpass MN, which assists to perfect the fundamental and harmonic impedances. At this stage, an iterative CAD-based optimization can be conducted by finely adjusting the physical length of each of the TLs until the exact matching condition is met. Finally, a post-optimization is performed together with the transistor in order to achieve the highest PA performance. The final design parameters of the output matching network are listed in Fig. 2, while its impedance trajectory is shown in Fig. 4(b). The desired Class-F load condition is obtained as indicated by the intrinsic-drain impedance $(Z_{\mathrm{L,Drain}})$ in Fig. 4(b). The second harmonic impedance is set to slightly capacitive for achieving the highest PAE, mainly due to the non-linear behavior of the output capacitor C_{DS} [7]. The insertion loss of the entire OMN is around 0.1 dB obtained from full Wave simulation.

In terms of the input matching, an optimal source impedance of $6.8 - j10$ at f_0 is provided by the input network shown in Fig. 2(a). The harmonics are all shorted mainly due to the large gate-source capacitance of the transistor ($C_{\mathrm{GS}} \approx 5$ pF). A 250 Ω resistor is connected to the bias line as a stabilizer. The entire circuit schematic is simulated using ADS Harmonic-Balance simulator. The de-embedded current and voltage waveforms at the intrinsic-drain plane are shown in Fig. 4(c), indicating an explicit Class-F behavior of the designed PA.

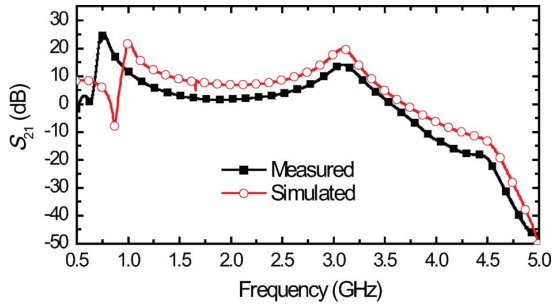

Fig. 6. Measured and simulated small-signal gain of the implemented PA.

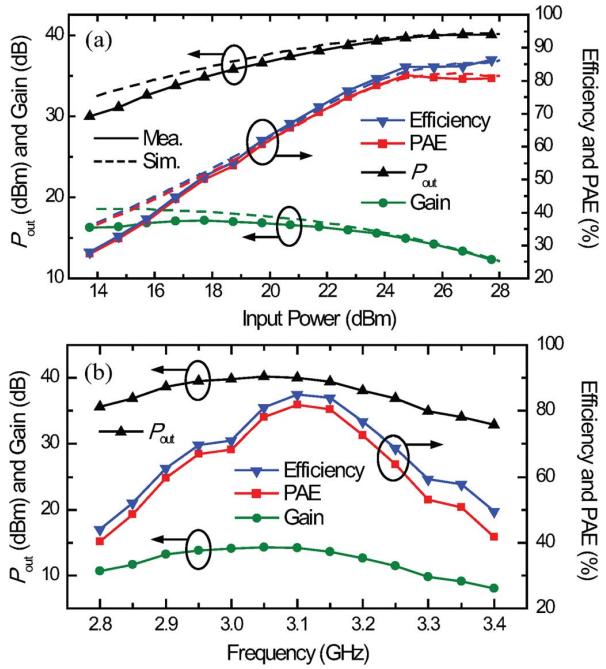

Fig. 7. (a) Measured and simulated PA performance versus input power at 3.1 GHz. (b) Measured PA performance at various frequencies.

TABLE I
PERFORMANCE COMPARISON OF REPORTED STATE-OF-THE-ART POWER AMPLIFIERS USING A GAN DEVICE

Refs.	Class	f(GHz)	G(dB)	P(W)	PAE(%)	$\eta^{*}_{Freq.}$
2007 [2]†	F	2.0	13	17	85	101.1
2008 [4]	F	2.14	15	10	70.9	85.9
2009 [8]†	F^{-1}	3.5	12	11	78	106.7
2010 [9]†	F^{-1}	2.15	18	8.2	84	101.6
2012 [7]	Saturated	3.5	17	6.9	80.1	109.1
This work	F	3.1	15	10	82	108.8

$*$ $\eta_{Freq.}$ denotes the frequency-weighted efficiency, PAE $\times$ (GHz)$^{0.25}$, in MTT-5 student PA design competition.
† The design is based on an unpackaged transistor chip.

III. PA IMPLEMENTATION AND EXPERIMENTAL RESULTS

The designed PA is fabricated on a Rogers 5880 PCB board, and it is mounted on a copper fixture using screws. Fig. 5 shows the fabricated PA circuit and board dimensions. Fig. 6 shows the small-signal frequency response of the PA with a drain voltage of 28 V and quiescent current of 50 mA. In the large-signal measurement, the gate is biased at a voltage of -3.6 V slightly below the pinch-off point (-3.3 V) for a maximized PAE. The PA is first tested with a power-swept continuous Wave (CW) input signal at 3.1 GHz. Fig. 7(a) shows the measured PA performance with respect to input power, including efficiency, PAE, gain, and output power. It can be seen that the gain starts to compress at $P_{\rm in} \approx 23$ dBm. The highest PAE of approximately 82% occurs at a $P_{\rm in}$ of around 25 dBm, with a corresponding $P_{\rm out}$ of 40 dBm, gain of 15 dB, and drain efficiency of 85%. The simulated results are also plotted in Fig. 7(a) for comparison, exhibiting a very good agreement with measurements. Subsequently, the frequency of the input signal is shifted around 3.1 GHz with a span of 0.6 GHz. The measured PA performance is shown in Fig. 7(b), indicating that a $>70\%$ PAE can be maintained from 3–3.2 GHz. The 3 dB bandwidth is around 350 MHz.

The measured results compare favorably to the state-of-the-art Class-F/F^{-1} PAs with the highest frequency Weighted efficiency $(\eta_{Freq.})$, as summarized in Table I [8], [9]. A recently-reported saturated PA presents a slightly higher $\eta_{Freq.}$, but it is based on a GaN device with lower power of 6 W. It is important to highlight that this design methodology does not rely on the bare-chip transistor with minimized parasitics, underlining its effectiveness of parasitic compensation for a high-frequency Class-F PA design.

IV. CONCLUSION

This letter presents a systematical approach for realizing high-frequency high-efficiency Class-F PAs using packaged GaN transistors. To effectively deal with the parasitics of the packaged device and perform harmonic control up to the fourth-order, a multi-stage, transmission-line, low-pass network is designed and implemented as the output circuit of the PA. With this matching network, the GaN transistor is optimally loaded at both fundamental frequency and harmonic frequencies. Simulation and experimental results show that an highly efficient Class-F PA mode is achieved at 3.1 GHz with a state-of-the-art PAE of 82%, 15 dB gain, and 10 W output power.

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