A 3.3V 625 kHz switched-current multiplier

A 3.3 V 625 kHz Switched-Current Multiplier

D. M. W. Leenaerts, G. H. M. Joordens, and J. A. Hegt

Abstract—**This paper presents a switched-current multiplier, designed for 3.3 V supply voltage, performing 0.625 M multiplications per second with a maximum nonlinearity of 0.94%. The die area is 100 × 75 μm^2 in a 2.4 μm n-well CMOS process.**

I. Introduction

CURRENT domain techniques and especially switched-current (SI) circuits are receiving more and more attention. Compared with switched-capacitor sampled-data circuits, SI circuits have a number of important advantages: they are exclusively composed of MOS transistors, switches and current sources instead of operational amplifiers, and precise linear floating capacitors, making them suitable for implementation in standard CMOS processes. As capacitors in SI technique are only used for holding voltages, SI circuits have no problems with capacitor mismatch. Furthermore, SI circuits are well suited for low-voltage applications.

A central element in SI circuits is the memory cell [1], [2] allowing for short-term storage of currents. The SI technique is often applied in filters, but its application area is rapidly growing [3] and comprises oscillators, digital-to-analog converters (DAC's), algorithmic analog-to-digital converters (ADC's), Sigma-Delta converters, cellular neural networks, etc. To the best knowledge of the authors, this paper is the first proposal for an SI multiplier.

Section II deals with the basic concept of (switched) current multipliers. In Section III the actual implementation of the multiplier using the quarter-square principle is described. Experimental results are provided in Section IV, while some concluding remarks are given in Section V.

II. Switched-Current Multiplier

There is a variety of existing current domain multiplier principles, such as the translinear multiplier [4], current domain multiplier based on a Gilbert cell [5], pulse modulation multiplier [6], multiplication based on ADC/DAC conversion [7], and quarter square multiplier [8], [9]. The key to the latter principle is in the following equation:

$$(x+y)^2-(x-y)^2=4xy. \tag{1}$$

When both x and y represent currents, two current squarers could be used. To cancel the quadratic terms completely however, the squarers should be perfectly matched. With the application of an SI memory cell, only one current squarer is required, as depicted in Fig. 1, circumventing the problem of matching. In this approach, first I_x and I_y are summed in the input circuit. The result is squared in the current squarer and temporarily stored in the memory circuit. Next I_x and I_y are subtracted. The result is squared and subtracted from the current that was stored in the memory circuit, resulting in an output current I_{out}, proportional to the product of I_x and I_y. This principle was used as a starting-point for the proposed SI multiplier. The SI multiplier of Fig. 1 is composed of three sub-circuits:

- an input circuit;
- a current squarer;
- an SI memory cell.

These three sub-circuits will be described below.

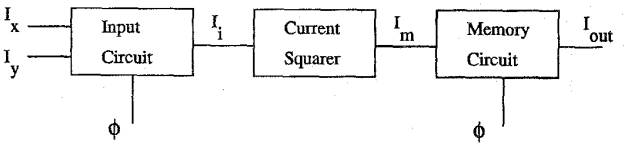

Fig. 1. Block diagram SI multiplier.

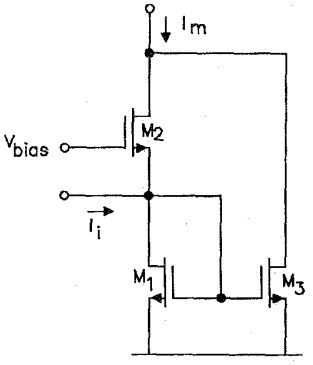

Fig. 2. Current squarer.

A. Current Squarer

For the current squarer in Fig. 1 several circuits exist, such as presented in [8]–[10]. The circuit in [10] was chosen for its simplicity and is given in Fig. 2. It has an (idealized) transfer of $I_m = I_o + I_i^2/4I_o$ in which I_o is a constant current, which depends on V_{bias}. The transfer function of the nonidealized current squarer of Fig. 2 can in first order be approximated as

$$I_m = I_o + e_1 + \frac{(I_i+e_2)^2}{4I_o} \tag{2}$$

Manuscript received November 6, 1995; revised April 2, 1996.

The authors are with the Department of Electrical Engineering, Eindhoven University of Technology, NL 5600 MB Eindhoven, The Netherlands.

Publisher Item Identifier S 0018-9200(96)06467-0.

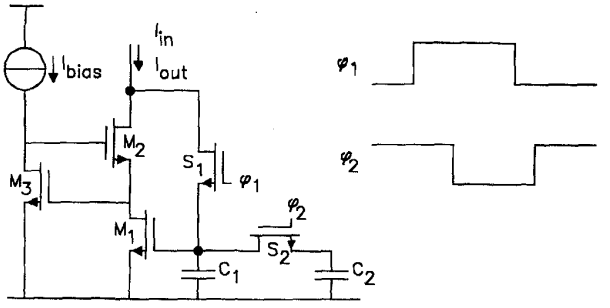

Fig. 3. Accurate SI memory cell.

where e_1 represents the output offset error and error e_2 the offset error at the input compared to the idealized transfer curve. Both errors are almost constant. A thorough analysis of this circuit reveals that the body effect of M_2 and channel length modulation may deteriorate its performance. For that reason this circuit was slightly adapted in the actual implementation, as will be described in Section III.

B. Input Circuit

With the quadratic transfer characteristic given by (2), simple analysis shows that the error in the output of (1) is $4ye_2/4I_o$. To eliminate this error, a slightly adapted version of this principle was used, based on

$$(x+y)^2 - x^2 - y^2 = 2xy. \tag{3}$$

This principle has two important advantages. First, the input currents of the current squarer are $I_x + I_y$, I_x, and I_y. As no subtraction of input currents is needed anymore, these currents can easily be realized using only a few switches, without the need for a current inverter with its related error. Second, the constant errors e_1 and e_2 of the current squarer can now completely be canceled. To realize this, four clock phases are required in which the currents $I_x + I_y$, I_x, 0 (i.e., no current), and I_y are provided in turn. Applying (3) then yields

$$\begin{aligned} I_{out} &= \left\{ I_0 + e_1 + \frac{(I_x + I_y + e_2)^2}{4I_o} \right\} \\ &\quad - \left\{ I_0 + e_1 + \frac{(I_x + e_2)^2}{4I_o} \right\} \\ &\quad + \left\{ I_0 + e_1 + \frac{(e_2)^2}{4I_o} \right\} \\ &\quad - \left\{ I_0 + e_1 + \frac{(I_y + e_2)^2}{4I_o} \right\} \\ &= \frac{I_x I_y}{2I_o} \end{aligned} \tag{4}$$

where the bracketed quantities correspond to the operations done on each of the four clock phases. Note the clock phase in which no current is provided to the current squarer is necessary to eliminate all errors. Due to the four clock phases, this multiplier is called a four-phase quarter-square SI multiplier.

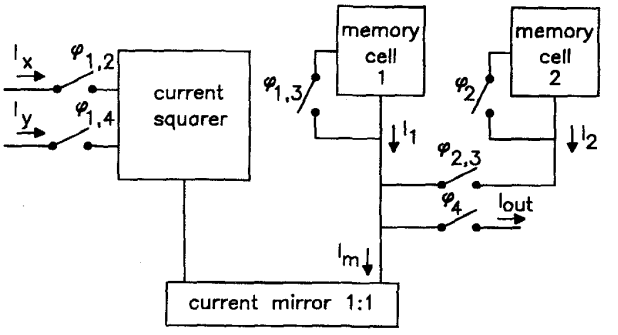

Fig. 4. Block diagram four-phase quarter-square SI multiplier.

The input circuit can now be composed of only two transistors, one connected to I_x and the other to I_y.

C. Memory Circuit

The third sub-circuit in Fig. 1 is an SI memory cell, for which several solutions exist [1]–[3]. The SI memory cell of Fig. 3 is used here [11]. Switching transistor S_2, which has the same size as S_1, and capacitor C_2 were added to reduce the clock feedthrough effects, caused by S_1. Cascode stage M_2, M_3 was added to reduce the effects due to the channel length modulation of M_1. The error at the output of the multiplier caused by this memory cell can be neglected in practice, compared to the errors caused by the nonidealities of the input circuit and the current squarer.

III. Actual Implementation

The block diagram of the final multiplier is given in Fig. 4. In the first phase, the current $I_x + I_y$ is squared and stored in memory cell 1. In the second clock phase, I_x is squared and stored in memory cell 2. Then in the third phase, no signal is applied to the squarer, but the contents of memory cell 2 are subtracted from that of cell 1. The output of the squarer is added to this intermediate result and the result is stored in cell 1. If in some applications a small output error is allowed, this clock phase may be skipped. In the final phase, I_y is squared and subtracted from the contents of cell 1. This result is immediately available at the output node. The described sequence is equal to the sequence as defined in (3) and (4).

The total four-phase quarter-square SI multiplier circuit is depicted in Fig. 5. A PMOS version (M_1–M_3) of the current squarer of Fig. 2 is used. In an n-well CMOS process the connection of the source of M_2 to the n-well eliminates the body effect problem. The output of the current squarer is fed to a regulated cascoded current mirror (M_4–M_7). In this way, problems caused by the finite output resistance of the current squarer due to channel length modulation were overcome. Two PMOS implementations (M_8–M_{11}, S_5, S_6, C_1, C_2) and (M_{12}–M_{14}, S_7, S_8, C_3, C_4) of the accurate SI memory cell of Fig. 3 were used. The cascoded current source (M_{15}–M_{17}) was added to ensure a positive current through the second memory cell. Capacitors C_1 and C_3 are 0.1 pF, the other capacitors are 0.5 pF. All capacitors are implemented in double poly.

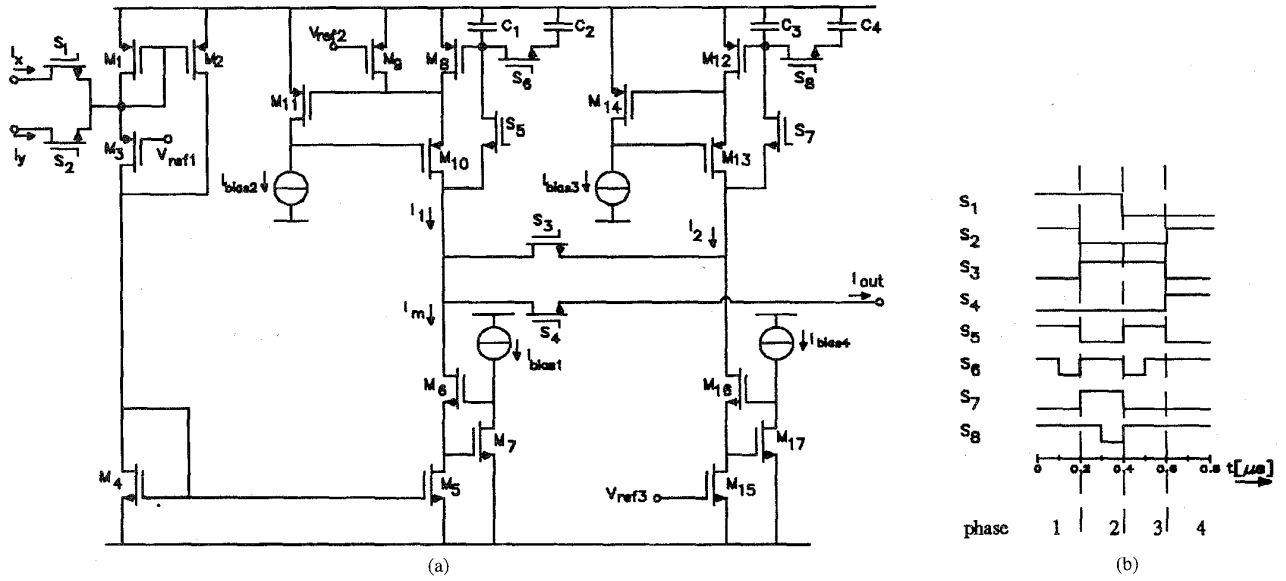

Fig. 5. Four-phase quarter-square SI multiplier circuit.

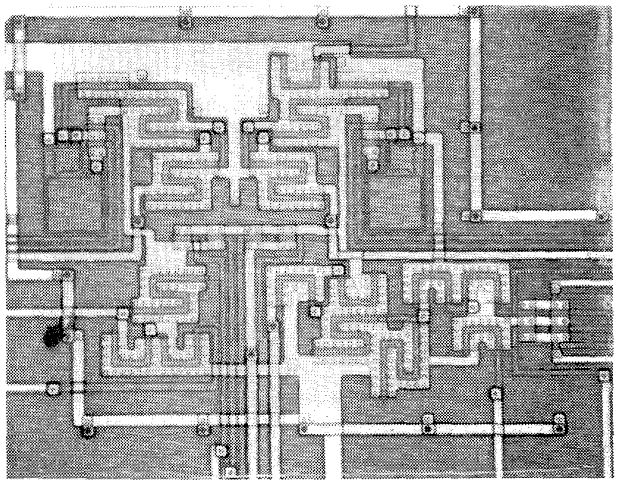

Fig. 6. Die photograph of the multiplier.

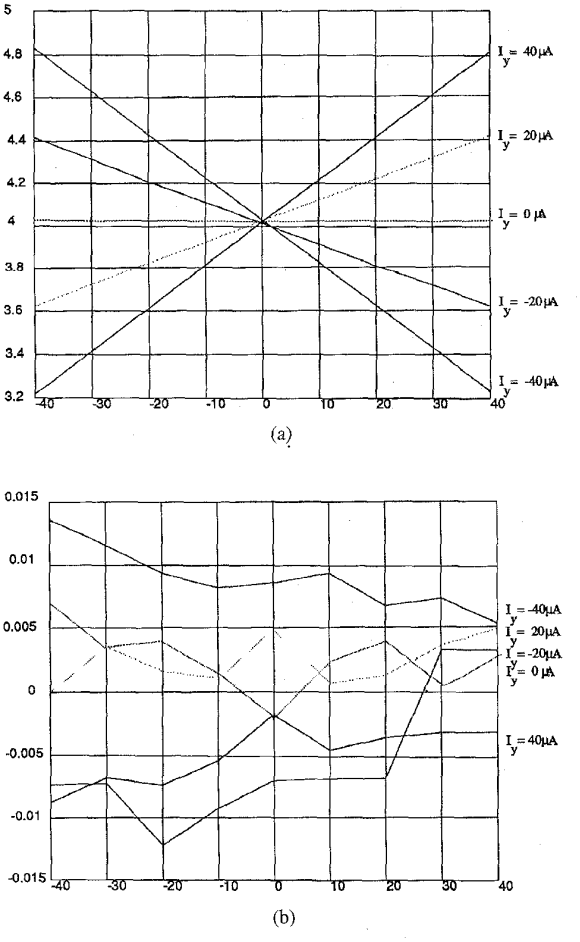

Fig. 7. Measured performances (a) output current (μA) versus input current I_x (μA) and (b) absolute error (μA) versus input current for different currents I_y.

IV. Experimental Results

Fig. 6 shows the die photograph of the multiplier. It occupies a 100 × 75 μm^2 chip area in a 2.4-μm CMOS process. The input currents as well as the output currents were measured by means of a 16-b ADC. The output node was held at 1.6 V during measurements using an operational amplifier. The measurements were performed with a clock frequency of 2.5 MHz, corresponding to 0.625 million multiplications per second. Fig. 7(a) shows the transfer curve and Fig. 7(b) shows the absolute error, compared to the expected transfer characteristic $I_{\text{out}} = aI_xI_y + b$ with $a = 4980\ \text{A}^{-1}$ and $b = 4.022\,\mu$A. The input current range is from -40 to 40 μA, the maximum output current is 4.8 μA. The total nonlinearity, defined as the absolute error divided by the maximum output swing, is 0.94%. This value is similar to

the simulated performance in [8] and measured performance of [9] but obtained at a 3.3 V power supply voltage instead of 5 V. The power dissipation for maximum input currents is 0.3 mW.

Continuous-time multipliers use several squares and their accuracy depends on the matching of these squarers. Here this matching problem is avoided by using memory cells to store intermediate results. Because this is the first attempt at designing a multiplier in SI technique, we cannot compare this design to similar ones. Its −3-dB bandwidth is much lower than continuous-time multipliers and is approximately 100 kHz. Besides the low nonlinearity, also the compactness of the circuit can be advantageous in applications. Experiments show that increasing the conversion time by a factor ten, the nonlinearity reduces to 0.2% which is of potential interest in applications where speed is not the main design issue.

V. Conclusion

In this paper, an SI multiplier is described. It consists of only one current squarer and two accurate SI memory cells. It is based on a slightly altered version of the "quarter square" principle. In this way, the problem of matching of two current squarers is circumvented, and furthermore, a number of nonidealities of the building blocks are canceled, resulting in an accurate multiplier in the current domain. Experimental results have been given to demonstrate the feasibility of the multiplier in SI design techniques. Advantages include a 3.3 V power supply voltage and a die area of $100 \times 75\ \mu m^2$.

Acknowledgment

The authors wish to thank the reviewers for helpful comments. Further, they wish to thank P. Klessens for generating the layout and O. Stoelinga for setting up the measure equipment.

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