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A 3.5 mW 5 μsec settling time dual-band fractional-N PLL synthesizer

Jun Gyu Lee[a)] **and Shoichi Masui**[b)]

Research Institute of Electrical Communication, Tohoku University

2–1–1 Katahira, Aobaku, Sendai, Miyagi 980–8577, Japan

a) *yijungyu@riec.tohoku.ac.jp*

b) *shomasui@riec.tohoku.ac.jp*

Abstract: We explore a dual-band fractional-N PLL synthesizer with 3.5 mW, 5 μsec settling time and 15 μsec start-up time in 0.18 μm CMOS technology. The power consumption is minimized through the design efforts in LC-VCO design to maximize the quality factor of an integrated inductor up to 6.1 at 866 MHz and minimize the VCO gain by a capacitor tuning technique with an on-chip nonvolatile memory and the proper choice of varactor. Measured results of a prototype fractional-N PLL satisfy the required settling and start-up times, and indicate that the phase noises at 10 kHz and 100 KHz offset are −108.7 dBc/Hz and −98.3 dBc/Hz, respectively, and the reference spurious level is −81.6 dBc.

Keywords: phase locked loop, low power design, voltage controlled oscillator

Classification: Integrated circuits

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1 Introduction

We propose a dual-band fractional-N PLL (phase locked loop) synthesizer featuring 3.5 mW, 5 μsec settling-time, and 15 μsec start-up time in a 0.18 μm CMOS for short-range communication transceivers applicable to smart-key systems. The specification and block diagram of the proposed 4th-order fractional-N PLL are shown in Fig. 1 (a), and Fig. 1 (b), respectively. The operation bands are 312.1–315.5 MHz (315 MHz band) used in Japan/U.S. and 433.6–434.4 MHz (433 MHz band) used in Europe. The power consumption of 3.5 mW is achieved by elaborations of VCO (voltage controlled oscillator) design as is described in the next section. In Fig. 1 (b), PFD, CP, DAC, DDSM, and NV-M represent phase frequency detector, charge pump, digital-to-analog converter, digital delta sigma modulator, and nonvolatile memory, respectively.

To maximize the data rate in FSK modulation, settling time of the proposed PLL is designed as 5 μsec. The parameters that dominate the settling time are programmable divider ratio N, charge pump current I_{CP}, VCO gain K_{VCO}, and loop filter passive components, C_p, R_s, C_s, R_r, and C_r. These parameter values are optimized from the constraints of settling time, phase noise and area by taking into account of process, voltage and temperature variations in the passive components, and obtained values are summarized in Fig. 1 (b) [1]. To accommodate to the dual-band operation and maintain the identical PLL crossover frequency for each operation band, only I_{CP} is scaled according to the change of N. Such design can remove influences by the change of passive components. The start-up time of 15 μsec is achieved with an open-loop calibration method featuring VCO capacitor coarse setting, and V_{CTRL} setting with the NV-M in order to eliminate the frequency detection and VCO coarse tuning sequences used in conventional start-up acceleration techniques. In the VCO capacitor coarse setting, the predetermined setting code, D_{FXC}, is provided from the NV-M to the VCO capacitors, and in the subsequent V_{CTRL} setting, an optimized V_{CTRL} is supplied from the DAC and associated varactor setting code, D_{DAC}, stored in the NV-M. The PLL loop control circuit generates a non-overlapping clock $\phi 1$, representing open-loop status, to provide calibration codes to the capacitors and varactors in LC-VCO, and $\phi 2$, representing closed-loop status, to synthesize the PLL output. A 3rd-order self-dithered DDSM is employed to reduce the fractional spurious below -80 dBc [2]. This DDSM demands 3rd-order loop filter, as shown in Fig. 1 (b), to filter out the shaped quantization noise.

In the following sections, the low-power design of the fractional-N PLL and its experimental results are presented.

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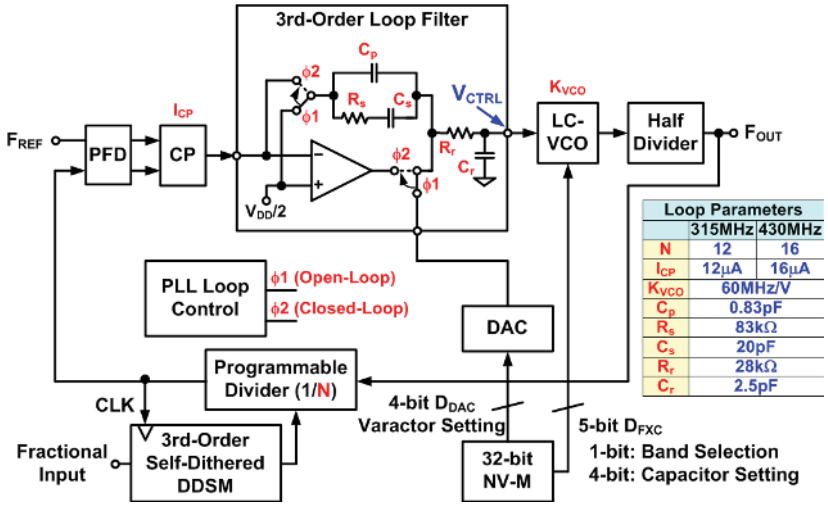
Specification Item	Value
Technology	0.18μm 1.8V
Reference Clock Frequency: F_{REF}	26 (MHz)
PLL Output Frequency: F_{OUT} (Dual-Band)	312.1 - 315.2 (MHz) [Japan/U.S.]
	433.6 - 434.4 (MHz) [Europe]
Modulation	FSK
Frequency Ressolution	1 (kHz)
Frequency Step in Modulation	30 (kHz)
Settling Time in Modulation	5.0 (μsec)
Start-Up Time	15.0 (μsec)
Phase Noise	-70 (dBc/Hz) @10kHz Offset
	-90 (dBc/Hz) @100kHz Offset
Reference/Fractional Spurious	-80 (dBc)
Power Consumption	3.5 (mW)

(a)



(b)

Fig. 1. Specification and architecture of the proposed fractional-N PLL synthesizer (a) Specification for short-range communication transceiver, (b) Architecture and circuit parameters of the proposed fractional-N PLL.

2 Low-power fractional-N PLL design

The power consumption in each block of the proposed fractional-N PLL designed in a 0.18 μm CMOS is summarized in Fig. 2 (a). Since over 52% of total power is consumed in the LC-VCO, the low-power VCO design by taking account of its phase noise becomes critical. The schematic diagram of the employed LC-VCO is shown in Fig. 2 (b). To minimize the phase noise for a given bias current I_{BIAS} of 0.95 mA, quality factor Q of the inductor L should be maximized [3] and K_{VCO} should be minimized through the optimization of capacitors and varactors.

The layout of the employed inductor with a patterned ground shield as well as its characteristics compared with those of other inductors designed for the VCO output frequency around 1 GHz are shown in Fig. 2 (c). It should be noted that the PLL output frequency is designed as a half of the VCO output frequency to reduce the phase noise. Q values of the designed inductor are higher than other results due to the increased size (410 μm $\times$ 410 μm)

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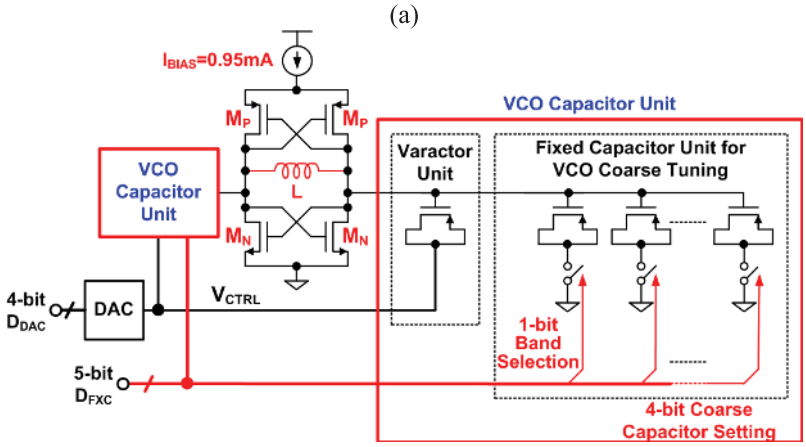
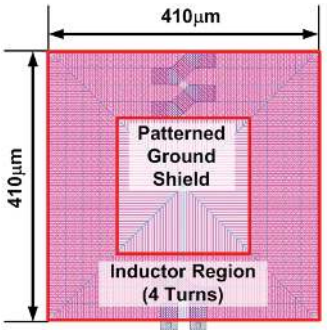
Circuit Block	Power Consumption [mW]	Ratio [%]
PFD and CP	0.28	8.2
Loop Filter	0.42	12.2
LC-VCO	1.80	52.1
Half Divider and Programmable Divider	0.37	10.8
DDSM and PLL Loop Control	0.43	12.3
Nonvolatile Memory and DAC	0.15	4.5
Total	3.46	100.0

(a)

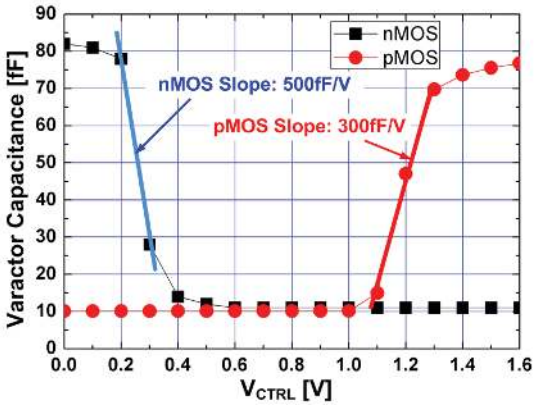


(b)



	[4]	[5]	This Work
Technology [μm]	-	0.18	0.18
Inductance [nH]	7.0	4.5	7.1
Output Frequency [MHz]	1000	800	630, 866
Q	5.0	4.0	4.9 (630MHz) 6.1 (866MHz)
Area [mm^2]	0.09	0.04	0.17

(c)



(d)

Fig. 2. Low-power fractional-N PLL design (a) Power consumption in each block of the proposed PLL, (b) Schematic diagram of the proposed LC-VCO, (c) Layout of on-chip inductor and comparison of inductor characteristics, (d) C-V characteristics of nMOS and pMOS transistors for varactor application.

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and line width (25 μm) for a given 5th Al-metal layer. To minimize the VCO gain, the fixed-capacitor unit, whose value is controlled by D_{FXC} with 1-bit band selection code and 4-bit capacitor coarse setting code, is added to the varactors as shown in Fig. 2 (b). Furthermore, pMOS capacitors and varactors are employed in the LC-VCO. Fig. 2 (d) presents simulated C-V characteristics for nMOS and pMOS transistors available to varactors in a given technology. Since the slope of the C-V characteristic is smaller in pMOS, its relative change of VCO output frequency over V_{CTRL}, equivalent to K_{VCO}, becomes smaller than that of nMOS.

As shown in Fig. 2 (b), CMOS topology is used for the LC-VCO to increase the oscillation amplitude in the current-limited operation mode provided from I_{BIAS} of 0.95 mA [3]. Total transconductance G_M necessary for the oscillation of 630 MHz is calculated as 21 mS, and 60% of G_M is supplied from nMOS transistors, M_N, and the rest of G_M is from pMOS transistors, M_P, to reduce the parasitic drain-to-bulk capacitance. Since the required G_M for 866 MHz is 17 mS, the identical LC-VCO structure can reduce the phase noise for 433 HHz band. The simulated phase noises of the designed LC-VCO are -90.7 dBc/Hz at 10 kHz offset, and -117.6 dBc/Hz at 100 kHz offset for 630 MHz, and -92.1 dBc/Hz at 10 kHz offset, and -118.9 dBc/Hz at 100 kHz offset for 866 MHz. The phase noise of the PLL can be attenuated to the insignificant level by the loop filter [1]. The worst-case figures of merit of the designed LC-VCO have reasonable values of 184.1 and 188.3 for 630 MHz and 866 MHz, respectively [3].

As is described in this section, the low-power design of the proposed PLL is achieved by the elaboration of LC-VCO design in terms of the inductor Q enhancement and K_{VCO} minimization techniques with capacitor tuning with a NV-M and a proper choice of varactor.

3 Experimental results

The proposed fractional-N PLL is fabricated in a 0.18 μm 1.8 V standard CMOS technology. The die micrograph is presented in Fig. 3 (a), where the die size is 950 μm $\times$ 515 μm, and a 32-bit 16-program-cycle NV-M with a 2-transistor memory cell utilizing a hot-electron trapping at the sidewall of memory transistor stores D_{FXC} and D_{DAC} [6]. Fig. 3 (b) indicates the measured transient waveforms of FSK modulation, and obtained settling times are 4.42 μsec and 4.13 μsec for 315 MHz and 433 MHz band, respectively. The measured V_{CTRL} waveform in the PLL start-up sequence for 315 MHz band is presented in Fig. 3 (c), and the start-up time is derived as 14.6 μsec by observing the PLL output frequency rather than this V_{CTRL}. The start-up time for 433 MHz is typically higher than that of 315 MHz due to the fast settling as shown in Fig. 3 (b).

The measured results of the phase noise and reference spurious level for 315 MHz band are shown in Fig. 3 (d) and Fig. 3 (e), respectively. The phase noise for 315 MHz band is worse than that for 433 MHz band due to the smaller Q in LC-VCO and smaller I_{CP} [1]. The phase noises at 10 kHz and

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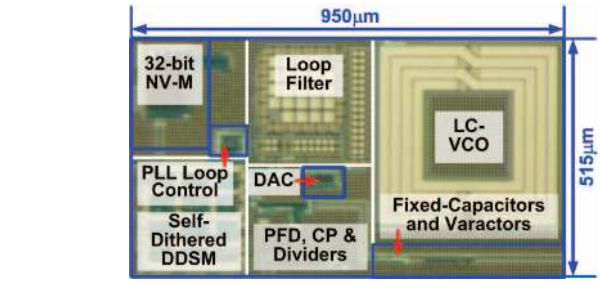
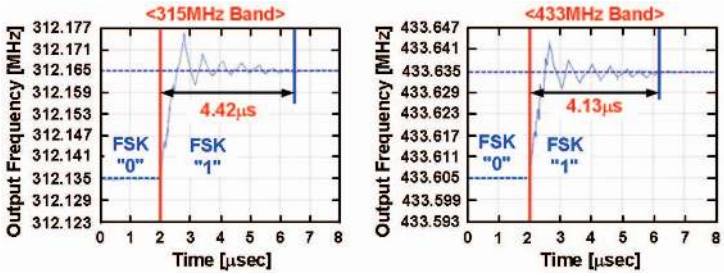


(a)



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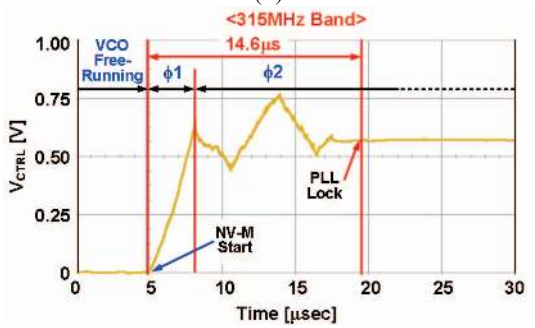
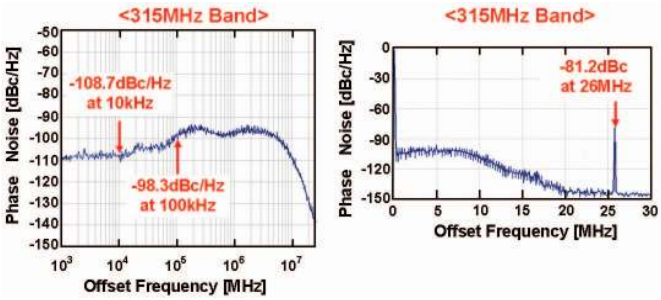


(c)



(d) (e)

PLL Characteristics	[7]	[8]	This Work
Technology [μm]	0.35μm	0.18μm	0.18μm
Output Frequency [MHz]	618~648	2431	312.1 - 315.2, 433.6 – 434.4
Phase Noise [dBc/Hz]	-85.0 @ 10kHz	-113.0 @ 1MHz	-108.7 @ 10kHz, -98.3 @ 100kHz
Settling Time [μsec]	10	10	4.4
Start-up Time [μsec]	250	20	14.6
Power [mW]	16	29.6	3.5
Size [mm^2]	0.4	2.1	0.48

(f)

Fig. 3. Experimental results (a) Die micrograph of the proposed PLL, (b) Setting time measurement results for 315 MHz and 433 MHz band, (c) Start-up time measurement for 315 MHz band, (d) Phase noise measurement for 315 MHz band, (e) Reference spurious level measurement for 315 MHz band, (f) Comparison of PLL characteristics.

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100 KHz offset for 315 MHz band are −108.7 dBc/Hz and −98.3 dBc/Hz, respectively, and the obtained spectrum well corresponds to the calculated result [1]. From the analysis it is clarified that for the offset frequencies below 10 kHz the contribution from CP is dominant to the entire phase noise, and over 1 MHz that from DDSM becomes most significant, while between these frequencies, the contribution from the OTA in the loop filter dominates. The reference spurious level observed at 26 MHz offset is −81.6 dBc, and remarkable fractional spurious tones are not observed.

Fig. 3 (f) compares characteristics of the proposed and published PLLs for low-power and fast settling/start-up applications. The proposed fractional-N PLL overwhelms other PLLs in terms of the settling time, start-up time and power consumption with comparable phase noise results.

4 Conclusion

A 3.5 mW fractional-N PLL synthesizer with 5 μsec settling time and 15 μsec start-up time is successfully developed by the elaboration of LC-VCO, optimized loop design methodology and the open-loop calibration method featuring the VCO capacitor coarse setting and subsequent V_{CTRL} setting enabled by an on-chip nonvolatile memory. A prototype fractional-N PLL fabricated in a standard 0.18 μm CMOS technology satisfies the required phase noise and reference spurious level.

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