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A 3.6μs Latency Asynchronous Frame-Free Event-Driven Dynamic-Vision-Sensor

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***Abstract*—This paper presents a 128x128 dynamic vision sensor. Each pixel detects temporal changes in the local illumination. A minimum illumination temporal contrast of 10% can be detected. A compact preamplification stage has been introduced that allows to improve the minimum detectable contrast over previous designs, while at the same time reducing the pixel area by 1/3. The pixel responds to illumination changes in less than 3.6μs. The ability of the sensor to capture very fast moving objects, rotating at 10K revolutions per second, has been verified experimentally. A frame-based sensor capable to achieve this, would require at least 100K frames per second.**

I. INTRODUCTION

Conventional image sensors are frame-based. In frame-based imagers the detected photocurrent is integrated in a capacitor during a fixed time period (the frame time). The reached voltage level of each pixel is communicated in a sequential way out of the chip. Frame-based imagers have some advantages such as very compact pixels, high fill factor, low fixed pattern noise (FPN), among others. However, they have serious drawbacks such as waste of bandwidth, because all the pixels send out their information regardless of wether they have new information to transmit or not. Also, because photocurrent is integrated over a fixed time period (generally in the order of 20-30ms), information about higher speed moving objects is lost. When a fast moving scene has to be sensed one solution is to reduce the frame period but this generates an overwhelming amount of data to be transmitted and processed. Mechanisms for detection of regions of interest can be applied but this has also high computational costs and delays [1]-[3].

Biological vision sensors operate in a quite different way. When the activity level of a retina pixel reaches some threshold, the pixel sends a spike to its connected neurons. That way, information is sent out and processed continuously in time (in a frame-less way) and communication bandwidth is used only by active pixels. Highly active pixels send spikes faster and more frequently than less active ones. Event driven or Address-Event-Representation (AER) [4]-[6] bioinspired vision sensors have become very attractive in recent years because of their fast sensing capability, reduced information throughput and efficient in-sensor processing. A large variety of AER vision sensors have recently appeared in the literature, such as simple luminance to frequency transformation sensors [7], time-to-first spike coding sensors [8]-[11], foveated sensors [12]-[13], temporal contrast vision sensors [14]-[19], motion sensing and computation systems [20]-[22], and spatial contrast sensors [17]-[18], [23]-[25], just to mention a few.

In this paper we present a very low latency AER-based temporal contrast vision sensor. The detection of temporal contrast at the focal-plane level can be very useful to sense and process high-speed moving objects while reducing redundancy and thus maintaining a low level of data to be processed. Several prior frame-based temporal difference detector imagers have been published [26]-[30], however they suffer from limited speed response because they operate based on photocurrent integration during consecutive frames and computing the difference between them. Several event-based (frame-free) temporal contrast vision sensors have been reported in recent years [14]-[19]. They are also referred to as Dynamic Vision Sensors (DVS). The sensor published by Kramer [16] had low contrast sensitivity, while the one by Zaghloul [17]-[18] suffered from poor FPN (fixed pattern

noise). Lichtsteiner et al. [14]-[15] presented the first practical DVS by introducing a self-clocked switched capacitor differencing and amplification stage resulting in low FPN (2.5%), practical contrast sensitivity (15%), reasonable pixel array size (128x128), very good latency (15μs), excellent intrascene dynamic range (120dB), and sufficient maximum event rate throughput (1Meps). The sensor was appropriate for high speed vision, since it could follow rotating objects up to a speed of 200 rps. Recently, a single pixel for a DVS sensor that achieves a 0.3% contrast sensitivity has been published [31]. The higher contrast sensitivity is achieved by a two-stage differencing amplifier [32], thus increasing the pixel gain a factor 50. However, this new design has very reduced pixel bandwidth.

This paper presents a new AER transient vision sensor (DVS) which is based on the one reported by Lichtsteiner and Delbrück [14]-[15]. By introducing a small area non-switched preampliflying stage we obtain a slightly better contrast sensitivity (10%) while reducing the pixel area by a 1/3 factor. By using an alternative photo sensing stage, latency can be reduced down to 3.6μs. As a result, the sensor is capable of detecting rotating objects up to a speed of 10000 rps. The price paid is an increase in the current consumption due to the preamplification stage and a smaller intrascene dynamic range. FPN also increases slightly but it remains significantly lower than the achieved contrast sensitivity. A mechanism has been designed to dynamically adapt the DC levels of the pixel preamplifying stage according to ambient illumination. Thanks to this adaptation mechanism the retina achieves a dynamic range higher than 100dB. However, intrascene dynamic range is reduced to 54dB.

II. PIXEL DESIGN

The pixel presented in this paper is based on a previously reported design [14]-[15]. However, in the present design a preamplification stage has been introduced that allows to achieve a slightly improved pixel sensitivity while reducing pixel area.

Fig. 1(a) shows a conceptual block diagram of the pixel. The first stage, the photoreceptor stage, which is based on a gate-biased source-driven stage [34], converts photocurrent I_{ph} to voltage V_{ph}

$$V_{ph} = V_G + nU_T \ln \frac{I_{ph}}{I_{sp}} \quad , \tag{1}$$

where n and I_{sp} are the substhreshold slope factor and the substhreshold current factor of transistor M_p [33]. In this type of source-driven stages, gate voltage V_G sets the DC level of the source voltage V_{ph} of transistor M_p for a given photocurrent I_{ph}.

The second stage, which is the new preamplification stage, is a voltage gain stage producing an output voltage

$$V_{pa} = V_{off} + GnU_T \ln \frac{I_{ph}}{I_{sp}} \tag{2}$$

being G the voltage gain of this preamplification stage and V_{off} a DC voltage. Voltage V_{pa} feeds a capacitive differentiator stage (as proposed in [14]) such that

$$dV_{diff} = -\frac{C_1}{C_2} dV_{pa} = -G\frac{C_1}{C_2} nU_T d\ln \frac{I_{ph}}{I_{sp}} = -G\frac{C_1}{C_2} nU_T \frac{dI_{ph}}{I_{ph}} \quad . \tag{3}$$

The capacitive ratio C_1/C_2 is designed to produce additional voltage amplification. Thus, total voltage amplification from V_{ph} to V_{diff} is $A = GC_1/C_2$. Voltage V_{diff} is compared to thresholds V_θ^+ and V_θ^-. When voltage V_{diff} exceeds the upper threshold V_θ^-, a negative event is generated through channel OFF and node V_{diff} is reset to an intermediate reference voltage V_{REF}. When voltage V_{diff} decreases below the lower threshold V_θ^+, a positive event is generated through channel ON and node V_{diff} is reset to reference voltage V_{REF}.

Let us call $V_{diffON} = (V_\theta^+ - V_{REF}) + (V_{os} + V_{osn})$ the voltage excursion at node V_{diff} that generates a single positive event through the ON channel, where V_{osn} is the DC offset voltage of comparator A_{on} in Fig. 1(a), and V_{os} represents the DC offset voltage of amplifier A_d plus the systematic offset voltage introduced at its input node by switching. Similarly, $V_{diffOFF} = (V_\theta^- - V_{REF}) + (V_{osf} - V_{os})$ is the voltage excursion at node V_{diff} that generates a single negative event through the OFF channel, with V_{osf} being the DC offset voltage of comparator A_{off}. Referring to the input, let us call "ON contrast threshold" (or "ON contrast sensitivity") θ_{ev}^+ the minimum contrast stimulus that generates a single positive event through output channel ON, and "OFF contrast threshold" (or "OFF contrast sensitivity") θ_{ev}^- the minimum contrast stimulus that generates a single negative event through output channel OFF. By integrating equation (3),

$$\begin{aligned} \theta_{ev}^+ &= \ln\frac{I_{bright}}{I_{dark}} = \frac{V_{diffON}}{nU_TA} = \frac{(V_\theta^+ - V_{REF}) + (V_{os} + V_{osn})}{nU_TA} \\ \theta_{ev}^- &= -\ln\frac{I_{dark}}{I_{brigth}} = \frac{V_{diffOFF}}{nU_TA} = \frac{(V_\theta^- - V_{REF}) + (V_{os} - V_{osf})}{nU_TA} \end{aligned} \tag{4}$$

That way, the minimum contrast stimulus to be detected can be adjusted through pixel threshold voltages V_θ^+ and V_θ^-. For amplifiers A_d, A_{on}, and A_{off} we used simple 7-transistor differential input structures, as opposed to the very simple structures used by Lichtsteiner [14]. The reason was to be able to freely adjust voltage V_{REF}, and also to allow testing of large differences between V_{REF} and $V_\theta^{+/-}$. In Section IV.A., we will illustrate how these thresholds must be set to optimize the pixel contrast sensitivity. Next, we describe in more detail the photoreceptor and preamplification stages.

A. Photoreceptor

The schematic of the photoreceptor block is depicted in Fig. 1(b). An n-well/p-substrate photodiode generates a photocurrent I_{ph} which is converted into voltage V_{ph} by transistor M_p. The photodiode node is clamped to virtual ground, thus increasing the photoreceptor bandwidth and compensating the effect of the large photodiode parasitic capacitance C_d. This input clamping stage [34] avoids any Miller coupling capacitance between the input and output nodes of the voltage amplifier, thus achieving very high bandwidth. Another interesting feature of this source-driven active feedback stage, as analyzed carefully elsewhere [34], is that it becomes stable for operating currents I_{ph} below a top value. The "inverting voltage amplifier" in Fig. 1(b) is always biased with a sufficiently high current I_b (in the order of nano amperes) to not limit the delay of the photo diode branch. Thanks to the avoidance of any Miller capacitance between the amplifier input and output nodes, the sensor's latency could be improved by a factor of 5 with respect to its prior design [14]-[15].

For low values of the photocurrent I_{ph}, the photoreceptor has a first order dynamics with a dominant pole due to the photodiode node with an associated time constant [34]

$$\tau_d = \frac{g_{dsb} + g_{dsc}}{g_{mn}}\frac{nU_TC_d}{I_{ph}}, \tag{5}$$

where g_{mn} is the transconductance of the voltage amplifier transistor M_n, and g_{dsb} and g_{dsc} are the output conductances of transistors M_c and M_b respectively (see Fig. 1b).

For larger values of the photocurrent I_{ph}, two complex conjugate poles may appear, dominated by the output node dynamics, with an associated time constant and Q

$$\tau_o = 2\frac{C_o}{g_{dsb} + g_{dsc} + \frac{I_{ph}}{nU_T}}, \quad Q = \sqrt{\frac{g_{mp} g_{mn} C_o}{C_d (g_{mp} + g_o)}} \tag{6}$$

where C_o is the equivalent capacitance at output node V_{ph} and $g_o = g_{dsb} + g_{dsc}$.Transconductance g_{mp} is the only light dependent parameter changing Q. The worst case Q (maximum) is achieved for $g_{mp} = g_o$, resulting in $Q = \sqrt{g_{mn} C_o / 4 g_o C_d}$. Transconductance g_{mn} can be one or two orders of magnitude larger than g_o, but C_d is easily at least two orders of magnitude larger than C_o. Therefore, maximum Q would at the most approach unity. Consequently, in this circuit, even if complex poles appear because of large photo currents, these poles will induce negligible ringing.

In Section IV we show that for illumination values up to 30klux, the photoreceptor is the stage that limits the pixel´s bandwidth and the dominant pole is approximately linear with the photoreceptor current as predicted by eq (5).

B. Small-Area Preamplifying Stage

The schematic of the small-area preamplifier stage is shown in Fig. 1(c). It is composed of two inverting gain stages formed by transistors M_{n_1}, M_{p_1} and M_{n_2}, M_{p_2}, respectively. Each gain stage is preceded by a buffering stage which helps to adapt the DC voltage level at the input of the amplifier. The inverting gain stages are designed to operate in the strong inversion regime, providing a total gain

$$G = \sqrt{\frac{\beta_n \left(\frac{W}{L}\right)_{n_1}}{\beta_p \left(\frac{W}{L}\right)_{p_1}}} \sqrt{\frac{\beta_n \left(\frac{W}{L}\right)_{n_2}}{\beta_p \left(\frac{W}{L}\right)_{p_2}}} \tag{7}$$

The preamplifying stage was designed to provide a total voltage gain approximately equal to 25.

The transistors aspect ratios $\left(\frac{W}{L}\right)_{n_1} = \frac{2{,}4\mu m}{2{,}4\mu m}$, $\left(\frac{W}{L}\right)_{p_1} = \frac{1{,}2\mu m}{16\mu m}$, $\left(\frac{W}{L}\right)_{n_2} = \frac{1{,}2\mu m}{1{,}2\mu m}$, $\left(\frac{W}{L}\right)_{p_2} = \frac{0{,}6\mu m}{8\mu m}$ were designed to operate in strong inversion while at same time having a moderate current biasing in the order of 1μA per pixel. The first stage is designed with larger transistors as its mismatch is amplified by the voltage gain of the second stage.

In weak inversion the gain of the preamplifying stage becomes

$$G = \left(\frac{n_p}{n_n}\right)^2, \tag{8}$$

where n_p and n_n are the subthreshold slope factors [33] of the PMOS and NMOS transistors respectively. So the gain of the preamplifying stage would be reduced approximately to 1, if biased in weak inversion.

As we will see in the next Section, voltages V_{adc_1} and V_{adc_2} adapt dynamically to global illumination changes, so that global illumination can change over several decades while the preamplifier stages remain properly biased.

ndwidth and the dominant pole is approximately linear with the photoreceptor current as predicted by eq (5).

C. Differentiator and Comparator Stages

The next stage is a self-clocked switched capacitor differencing and amplification stage as used by Lichtsteiner et al. [14]. Lichtsteiner used a gain of 20 for this stage, which required a C_1/C_2 capacitor ratio of 20, resulting in a high capacitor area consumption. Actually, most of the pixel area (almost 50%) was consumed by these two capacitors. In our case, since we introduce extra gain through the preamplifiers, we only implemented a gain of 5 for the switched capacitor differential stage, thus helping to reduce the overall pixel area. If the CMOS process offers the possibility of using MiM capacitors, Lichsteiner's design

would be much more area efficient. However, even in this case, introducing these small area pre-amplifiers improves the gain (and therefore the contrast sensitivity) by an extra multiplicative factor.

For the voltage comparators and the in-pixel AER communication circuits, we used the same circuit already reported by Serrano et al. [35].

III. SYSTEM DESIGN

The complete system architecture block diagram is shown in Fig. 2(a). The system is composed of a 128x128 pixel array, a row of 128 preamplifier biasing cells that detect the average illumination along that row which adapts the DC levels of the preamplifiers voltage biases V_{adc_1} and V_{adc_2}, a set of programmable current sources that allow to fine tune all the current biases needed by the pixel by accessing to a very reduced set of pins [36], and finally the row and column address event communication circuitry that generates the output addresses. The AER read-out scheme implemented in this design is Boahen's row parallel technique which latches all the events generated simultaneously in a row and reads them out sequentially speeding up significantly the read out process when high event rates have to be managed [37].

The schematic of a preamplifier biasing cell is detailed in Fig. 2(b). Each cell contains a replica of the pixel photoreceptor circuit that senses the local illumination I_{ph}. The sensed current is replicated by the current mirror formed by the two identical transistors M_p and M_{p_r} and summed and low pass filtered in a common node V_C, where a large distributed capacitor C_C eliminates the high frequency components of the sensed current. The result is a spatio-temporal average of the sensed illumination along the row $\overline{I_{ph}}$ which is locally replicated through a subpico ampere current mirror [38]-[39]. The replicated $\overline{I_{ph}}$ feeds a modified replica of the pixel photoreceptor circuit where the photodiode has been substituted by the subpicoampere current mirror output. The output voltage of this stage $\overline{V_{ph}}$ is the input to a replica of the preamplifying stage, where two feedback amplifiers A_{f1} and A_{f2} have been added to keep the DC levels of the preamplifiers outputs tied to the external voltage references V_{o1} and V_{o2}. These reference voltages are adjusted to optimize gain and power consumption of the preamplifier stage. Feedback amplifiers A_{fi} (i = 1,2) are detailed in Fig. 2(c). The output transistors M_{pxi} and M_{nxi} are replicated once per pixel array cell (row) plus once per biasing cell (column). This way, the DC current provided to nodes V_{adci} scales directly with pixel array size. The capacitive load at node V_{xi} scales with the number of rows in the array, so that bias current I_{bf} and the compensation capacitor C_x would require further readjustments when adding rows. The biasing cells are replicated once per pixel array column to ensure scalability with the number of columns. Nodes V_{x1}, V_{x2}, V_{adc_1} and V_{adc_2} are shared by the whole array as well as by the row of 128 biasing cells. Their DC levels are adapted with illumination changes so that the average output voltages of the preamplifiers are always correctly biased in the strong inversion saturation regime. Whenever there is a sudden change of global illumination, this type of retinas produce a sudden storm of output events (also if there is no adaptation mechanism [14]). The time constant of the adaptation mechanism depends on the average photocurrent. We designed it to be in the order of hundreds of milliseconds for illumination levels of about 1klux.

IV. EXPERIMENTAL RESULTS

A prototype has been fabricated in a double-poly 4-metal 0.35μm CMOS technology. The fabricated retina has a resolution of 128x128 pixels and occupies a total area of 5.5x5.7mm^2 including the pads. Fig. 3(a) shows a microphotograph of the fabricated prototype and Fig. 3(b) a plot of the layout of an arrangement of 4 pixels. Pixels are arranged in a symmetrical way sharing analog and digital routing channels. Thus, noise coupling between analog and digital parts is minimized. Digital lines are routed horizontally over digital parts using metal 2, while sensitive analog lines are routed horizontally over analog parts. Metal 4 is

reserved to cover the full array except for the photodiode. Table 1 summarizes the main design specifications [40] and compares them with previously reported designs. The retina was tested with a 16mm F/1.4 C-mount lens. Comparing with the design reported by Lichtsteiner et al. [14], this prototype achieves a lower contrast threshold with a 1/3 area reduction. The latency time has also been reduced from 15μs down to 3.6μs. The current consumption increases due to the preamplification stages. FPN also increases slightly but it remains significantly lower than the achieved contrast sensitivity. The retina achieves a dynamic range higher than 100dB. However, intrascene dynamic range is reduced to a factor of 54dB. Sample images are shown in Fig. 4.

A. Uniformity of Response, Minimum detectable contrast, and Pixel Gain Characterization.

To characterize the uniformity of the response to a given contrast, a similar procedure to the one developed by Lichtsteiner and Delbrück [14] was followed. In order to stimulate all pixels uniformly, a moving gradient bar (shown in Fig. 5(c)) was presented to the retina and the number of positive and negative events generated by each pixel was recorded. The bar crossed the screen in about 4s. For this we used a TFT monitor providing a scene illumination of about 250 lux. The contrast of the stimulus was measured to be $\theta = \ln\frac{I_{bright}}{I_{dark}} = 1{,}39$ (which corresponds to a 1:4 contrast, or 400%). The experiment was repeated for different settings of the pixel thresholds. The bar was swept 30 times for each setting. This way, for each pixel (x, y) we obtain its corresponding number of positive $N^{+}(x, y)$ and negative $N^{-}(x, y)$ events fired per edge presentation for the different settings of threshold voltages ($\left|V_{REF} - V_{\theta}^{+/-}\right|$). Fig. 5(a) shows the histograms for $N^{+/-}(x, y)$, for both positive (crosses) and negative (dots) events. Histograming the number of events (as done in [14]) does not clearly show the contrast sensitivity of the sensor as a function of threshold voltage settings ($\left|V_{REF} - V_{\theta}^{+/-}\right|$). However, the same data can be used to histogram $\theta_{ev}^{+/-}$, by noting the following. The number of events generated by a pixel for a given stimulus contrast θ and threshold voltage setting is given by

$$N^{+/-} = \frac{\theta}{\theta_{ev}^{+/-}} \tag{9}$$

	This work	Lichtsteiner et al.	Gottardi et al.	Chi et al.	Zaghloul et al.	Gruev et al.	Posch et al. [19]
Resolution	128x128	128x128	128x64	90x90	96x60	189x182	304x240
Fill factor	8.7%	8.1%	20%	17%	14%	30%	10%-20%
Latency	3.6μs	15μs	250μs	<5ms	-	20ms	3μs
Consumption	132-231mW	24mW	100μW	4.3mW	63mW	30mW@5V	50mW-175mW
Technology	0.35μm 4M 2P	0.35μm 4M 2P	0.35μm	0.5μm 3M 2P	0.35μm 4M 2P	0.5μm	0.18μm 4M 2P MIM
Pixel area	35x35μm^2	40x40μm^2	26x26μm^2	25x25μm^2	34x40μm^2	25x25μm^2	20x20μm^2
Chip area	5.5x5.6mm^2	6x6.3mm^2	4.5x2.5mm^2	3x3mm^2	3.5x3.3mm^2	-	9.9x8.2mm^2
Contrast Sensitivity	10%	15%	10%	2.2%	-	-	13% (single pixel)
FPN	4.0% contrast	2.1% contrast	-	0.5% of scale	1-2 decades	0.6% of scale	-
DR	>100dB	120dB	100dB	51dB	50dB	-	125dB
Intrascene DR	56dB	120dB	100dB	51dB		-	125dB

Table 1. Main design specifications and comparison with previous designs

Consequently, for each pixel we can compute its contrast sensitivity $\theta_{ev}^{+/-}(x,y) = \theta / N^{+/-}(x,y)$, and generate the corresponding histogram for $\theta_{ev}^{+/-}$ as shown in Fig. 5(b). As can be observed, it was possible to set an average contrast threshold as low as $\theta_{ev} = 10{,}45\%$ with a FPN of $\sigma(\theta_{ev}) = 4.0\%$. It was possible to adjust a lower threshold value, but then the output was dominated by noise events. This minimum detectable contrast has been improved with respect to the 15% minimum contrast threshold reported in [14] thanks to the increase in pixel gain. It is limited by noise, but also by the mismatch of the comparators (A_{off} and A_{on} in Fig. 1). Tuning $V_{\theta}^{+/-}$ too close to the reset voltage of node V_{diff} in Fig. 1, results in some pixels having some of the comparators always ON, and thus self-oscillating. Increasing gain $\bar{A}$ helps in attenuating the effect of this comparator offset mismatch (see eq. (4)). Improving minimum detectable contrast has been precisely the motivation of the present design, increasing the pixel gain to increase the pixel sensitivity, and doing it with a compact circuitry that allows to simultaneously reduce pixel area. Although this preamplifying circuitry introduces some amount of gain mismatch, the 4% FPN remains lower than the 10% overall contrast sensitivity limit.

Using eq. (4) and the measured mean values of the contrast thresholds $\overline{\theta_{ev}^{+}}$ and $\overline{\theta_{ev}^{-}}$ we can estimate the achieved value of the average pixel gain $\bar{A}$. By representing the average contrast threshold ($\overline{\theta_{ev}^{+}}$ and $\overline{\theta_{ev}^{-}}$) as a function of the voltage threshold $\left|V_{REF} - V_{\theta}^{+/-}\right|$, and fitting these graphs to straight lines, we can obtain the average gain $\bar{A}$ from the slopes, as well as the average offset voltages for $V_{os} + V_{osn}$ and $V_{os} - V_{osf}$. The resulting average gain is $\bar{A} = 60.8$, while the offsets are $\overline{V_{os} + V_{osn}} = 103mV$ and $\overline{V_{os} - V_{osf}} = 89mV$. Assuming $\overline{V_{osn}} = \overline{V_{osf}}$ results in $\overline{V_{osn}} = \overline{V_{osf}} = 7mV$ and $\overline{V_{os}} = 96mV$. This latter offset is dominated by reset switching induced offset.

B. Dynamic Range

The operation of the retina has been verified for over 100dBs of illumination change. The retina has been tested for bright illumination (higher than 50Klux) down to illuminations below 1lux. Maximum ambient illumination was set by using two 20W compact fluorescent light (CFL) bulbs each providing about 30Klux when placed 40cm apart from the retina (scene illumination was measured with an RS 180-7133 digital lightmeter located at the retina position). Then neutral density filters were used to progressively darken the field of view of the retina. The density filters were Newport FS-ND broadband ones that guarantee flat transmission from ultraviolet to near infrared.

The lower illumination limit of the retina is limited by the dark current of the photodiodes which is lower than 12fA. We were not able to measure the photodiode dark current with very high precision in our chip, but could establish that it was lower than $12fA$. This was done by collecting the total current flowing through node V_{gnd01a} in Fig. 2(b) while keeping the retina in darkness. The current measured through that node in these conditions is $128 \times I_{dark}$ plus the leakage current due to the pads and wiring. The total current measured in the darkness through node V_{gnd01a} was $2.33pA$. We measured a leakage current for the pads and wiring of $0.76pA$, what gives an estimation of the dark current I_{dark} of $12fA$.

Intra-scene illumination range of the retina is limited, since the preamplifying stage self-adapts to one single global illumination level. Nevertheless, an intra-scene illumination dynamic range of up to 54dB has been verified. Fig. 6 shows the response of the retina with half of the visual field at 1lux while the other half is illuminated at 500lux, by inserting a neutral density filter diagonally over the field of view while placing the setup in a dark chamber to avoid reflections.

C. Pixel Bandwidth

To measure the pixel bandwidth a group of pixels located in the center of the array were stimulated with a flashing Kingbright super bright red LED L-793SRC-B (1400mcd@20mA) following a similar procedure as the one developed by Lichtsteiner and Delbruck [14]. We created a scene illumination by placing two CFL bulbs near the retina but not directly focused on it. A scene

illumination of 30klux was measured by placing the light meter RS-180-7133 in the retina position. The LED was placed in front of the retina. The LED diode was modulated with a sinusoidal signal

$$V(t) = V_{off} + A\sin 2\pi ft \tag{10}$$

We varied the frequency of the sinusoid and counted the number of positive and negative events generated by each stimulated pixel per period of the sinewave. The measurements were averaged over a 20 seconds time period. If the magnitude of the stimulus contrast and the voltage thresholds are kept constant, the pixel gain is directly related to the number of generated events (see eqs. (4) and (9)). The measurements were repeated for different values of the illumination by inserting neutral density filters of different attenuation values. These neutral density filters were placed just in front of the retina, thus attenuating simultaneously the scene and the LED illuminations.

Fig. 7(a) plots the measured values of the events per cycle as a function of the frequency of the sinusoidal signal for different illumination values. Each of these curves was fitted to a first order transfer function. Fig. 7(a) also shows the fitted first order function corresponding to the lowest illumination of 1.5lux. The optimally extracted poles are plotted in Fig. 7(b) as a function of the illumination. Also, superimposed as a solid trace, the optimal linear fitting of the poles position versus the illumination is shown. As can be observed, in all the measured illumination range the bandwidth is approximately linear with the photocurrent as predicted by eq.(5).

D. Latency

Latency is the delay it takes from the occurrence of an illumination change at the photodiode until the corresponding output event is transmitted off-chip. To measure the latency, we used the super bright LED stimulated with a step signal [14]. We measured the latency as the delay between the step in the LED signal and the first output request corresponding to an event with the address of the stimulated pixel. In the same way as we did in the previous experiment, we created an intense scene illumination by placing two CFL bulbs near the retina but not directly focused on it. A scene illumination of 30klux was measured by placing the light meter RS-180-7133 in the retina position. The LED was placed in front of the retina. Neutral density filters were placed just in front of the retina, thus attenuating simultaneously the scene and the LED illuminations. We performed the measurements for different values of the illumination. Each measurement was repeated a total of 30 times. The results of these measurements are shown in Fig. 7(c) which plots the measured latency as a function of the illumination. The latency deviation measured among the 30 trials is also marked with error bars. As can be observed, the latency is inversely proportional to the illumination. For very low illumination (in the order of 1 lux) the measured latency is $10ms$, while for high level of illumination (10 Klux) the measured latency was 3.6μs. The only part of the pixel whose latency depends on illumination is the photoreceptor stage in Fig. 1(a). The rest of circuitry introduces a light independent delay, but depending on biasing.

E. Noise Characterizations

To characterize noise, we collected noise events (without stimulus) for different settings of illumination and threshold $\left|V_{REF} - V_{\theta}^{+/-}\right|$ settings. Events are separated according to their sign. Fig. 8(a) represents as a function of $\left|V_{REF} - V_{\theta}^{+/-}\right|$ the number of noise events per pixel per second collected for each sign, under an ambient illumination of 3 lux. Fig. 8(b) represents the noise events as a function of illumination for $\left|V_{REF} - V_{\theta}^{+/-}\right| = 175mV$, which is approximately the bias we used to determine the minimum contrast threshold $\theta_{ev}^{+/-}$ in Fig. 5. Noise events are generated at a constant average rate, for a given light and threshold setting. If a stimulus is moving fast, then the ratio of signal to noise events will be high. However, as stimuli move slower, the noise events start to become relevant and the overall signal to noise ratio decreases.

F. Power Consumption

Chip power consumption has been characterized. The measurements are shown in Fig. 9, where the total chip current consumption is plotted versus the output event rate. The total current consumption includes the current consumed by the programmable current biasing block, the pixel analog and digital parts, and the peripheral AER communication circuitry. At low output event rates the current consumption is dominated by the analog parts, which depends on the chip biasing, while at high event rates the current is consumed mainly by the digital event generation parts. The current consumption at moderate output event rates (below 1*Meps*) measured in Fig. 9 is approximately 44mA from a 3.3V power supply, that is a consumption of 145mW. Most of this current consumption comes from the strong inversion biased preamplifier stages. For very high event rates (above 1*Meps*) there is a sudden increase in power consumption because now the contribution of the digital output pads (and all the AER communication circuitry) becomes larger than that of the preamplifier stages.

G. Stimulus Rotation Limit

This sensor is specially appropriate for very fast moving objects. According to our measurements the sensor can detect moving objects at frequencies higher than 10KHz. We have set up several experiments to generate very high speed moving stimuli.

We painted a white dot on the rotating black blade of an electrical fan. The maximum rotating speed of the fan was 400Hz (24Krpm). The retina could easily detect it. Fig. 10 shows a spatio-temporal representation of the positive and negative events captured during a time of 7ms. The gray dots correspond to the positive events and the black dots correspond to the negative signed ones.

In order to generate faster and controlled stimuli we used a Tektronix 2467-B analog oscilloscope working in XY mode. We applied as X and Y inputs two signals with a controlled frequency generating a spiral-like trace on the oscilloscope display. However, there was a persistency of the ON state of the oscilloscope phosphor display that made not possible to check the negative transitions at frequencies higher than 1KHz. We could check that positive edges are correctly detected up to frequencies slightly higher than 10KHz. Fig. 11(a) plots the input stimuli waveforms applied to the X and Y inputs of the oscilloscope and Fig. 11(b) shows the image observed in the oscilloscope display for a 500Hz frequency of the input signals captured by a commercial photograph camera. Fig. 11(c)-(d) plot the spatio-temporal representation of the positive and negative events generated by the retina when it is stimulated by the oscilloscope display for different frequencies of the applied signals. Positive events are represented as gray dots while negative events are plotted as black dots. At a stimulus frequency of 500Hz both positive and negative events are clearly distinguished for the spiral moving generated dot. However, for frequencies in the order of 1KHz the negative events begin to become sparse. The problem was related with the stimulus, as we observed that the oscilloscope phosphor display had a persistency time of the ON state that prevented to observe a quick ON-OFF transition. On the contrary, the fast OFF-ON transition of the oscilloscope display allowed us to observe the ON events of the fast moving dot up to a frequency of 10KHz. The chip illuminance for this experiment was 250lux which is the light provided by the oscilloscope (when setting trace intensity to maximum), measured with our light meter. As shown in Fig. 11(b), the spiral has 5 cycles. Consequently, at 10*KHz* spiral rotation, a pixel detects a change after 5 cycles, requiring a bandwidth of about 2*KHz*. According to Fig. 7(a), at this illumination level, a pixel can still provide output for 2*KHz*.

V. CONCLUSIONS

A 128x128 temporal contrast retina has been implemented. The new design including a low area preamplifying stage allows to improve contrast sensitivity over previous designs while reducing the pixel area by a 1/3 factor. A global adaptation mechanism

is included that dynamically adapts the bias levels of the preamplification stages to ambient illumination, thus achieving a dynamic range higher than 100dBs. The global adaptation mechanism uses light sensed on a peripheral row. In future prototypes the objective is to obtain the average directly from the pixel array. Designing preamplifying stages operating at low currents to reduce static power consumption is also an objective of future work.

VI. ACKNOWLEDGEMENTS

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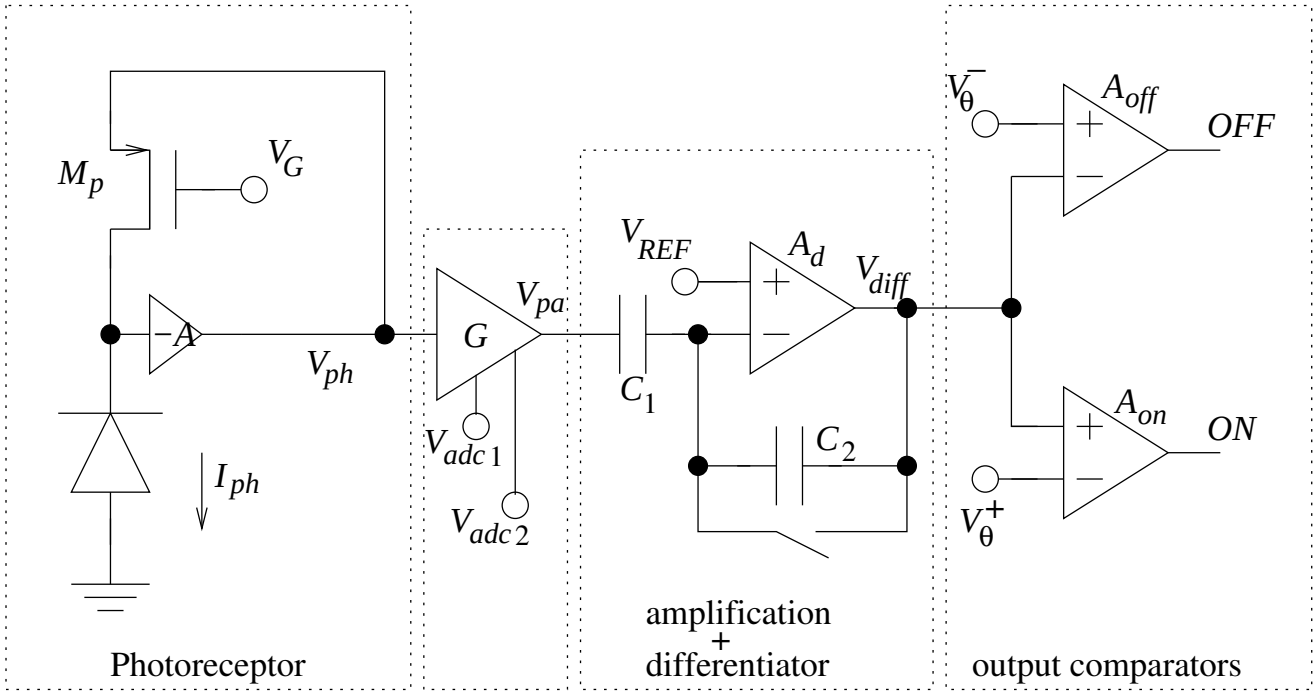

M_p
V_G
$-A$
V_{ph}
I_{ph}
G
V_{pa}
V_{adc1}
V_{adc2}
V_{REF}
A_d
V_{diff}
C_1
C_2
V_θ^-
A_{off}
OFF
A_{on}
ON
V_θ^+
Photoreceptor
amplification + differentiator
output comparators

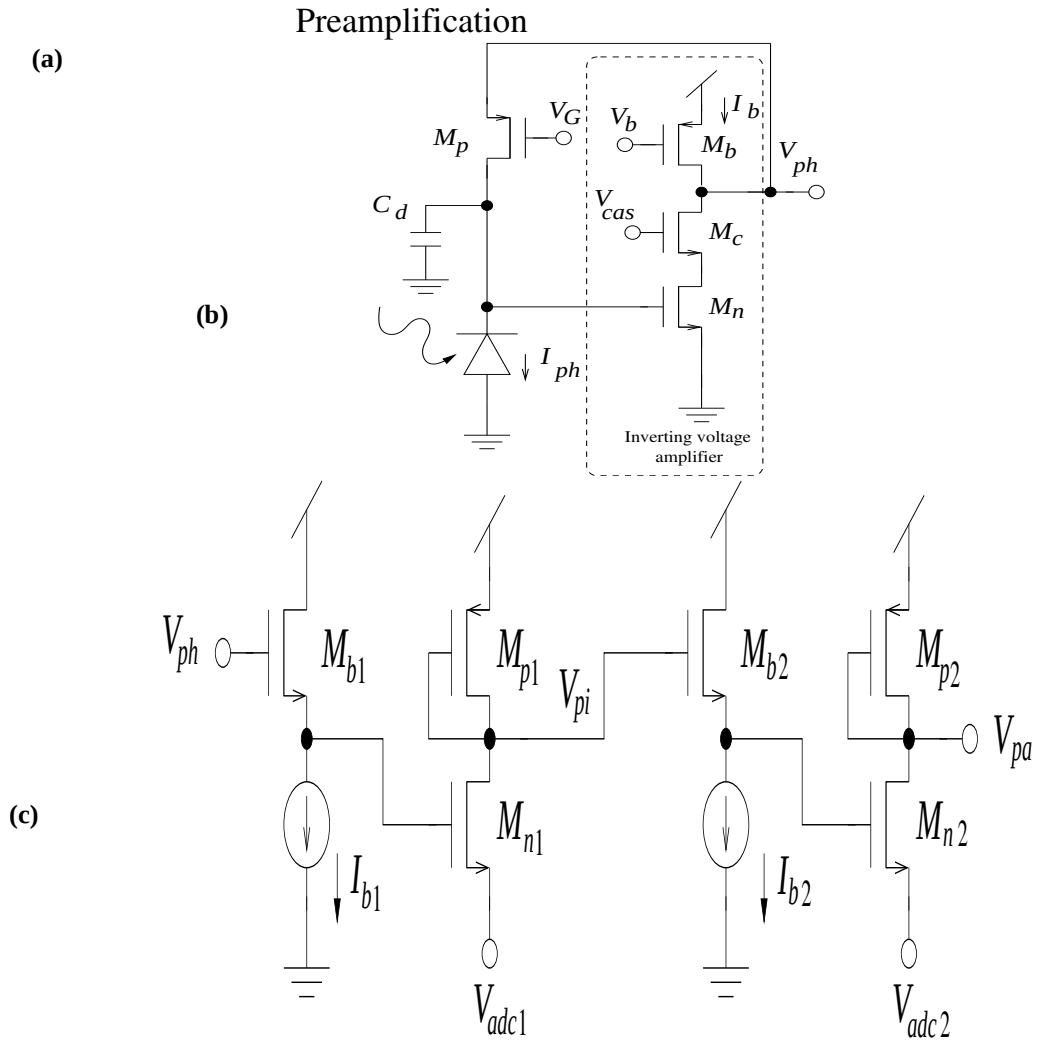
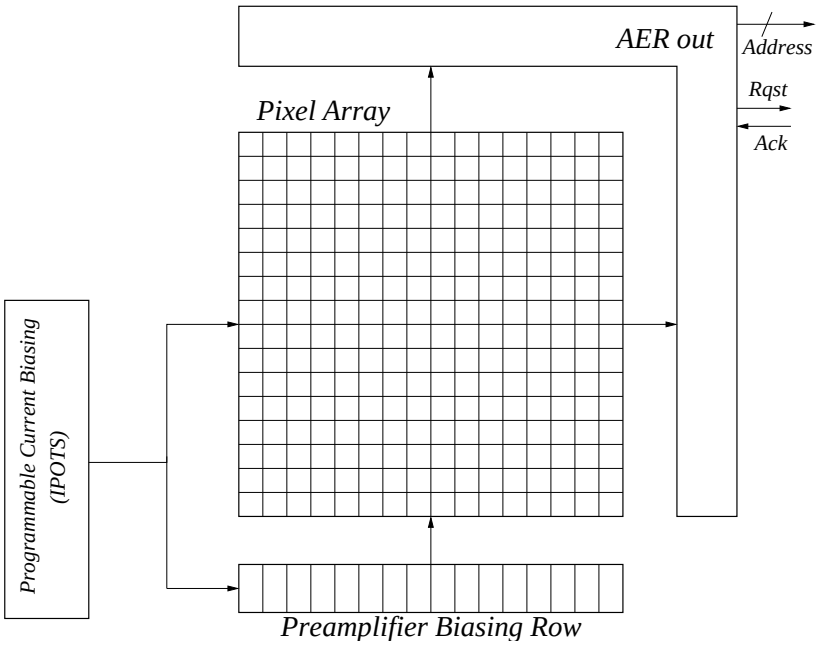
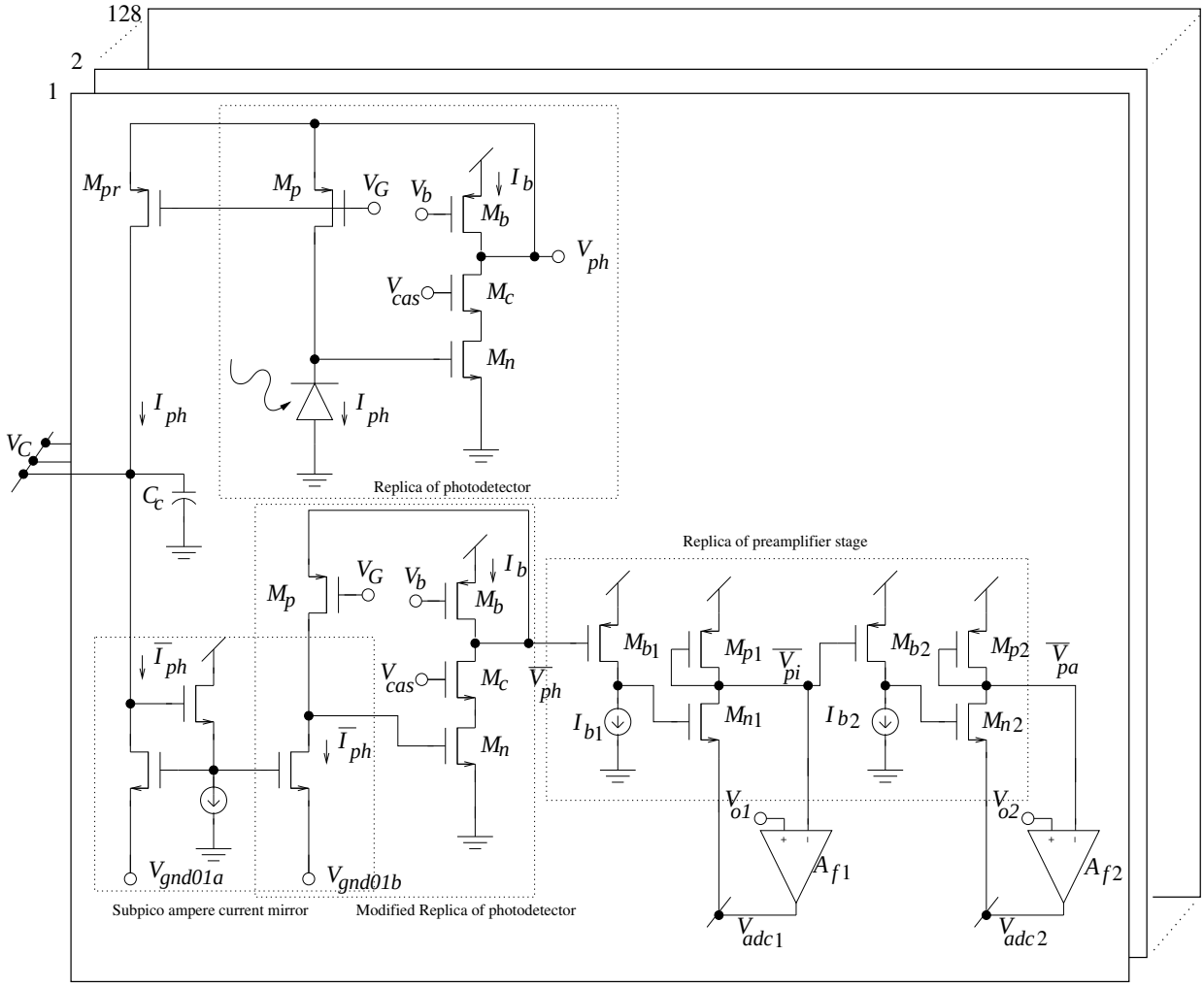

Preamplification
(a)
(b)
(c)
V_G
V_b
I_b
M_p
M_b
V_{ph}
C_d
V_{cas}
M_c
M_n
I_{ph}
Inverting voltage amplifier
V_{ph}
M_{b1}
M_{p1}
V_{pi}
M_{b2}
M_{p2}
V_{pa}
M_{n1}
M_{n2}
I_{b1}
I_{b2}
V_{adc1}
V_{adc2}

Figure 1

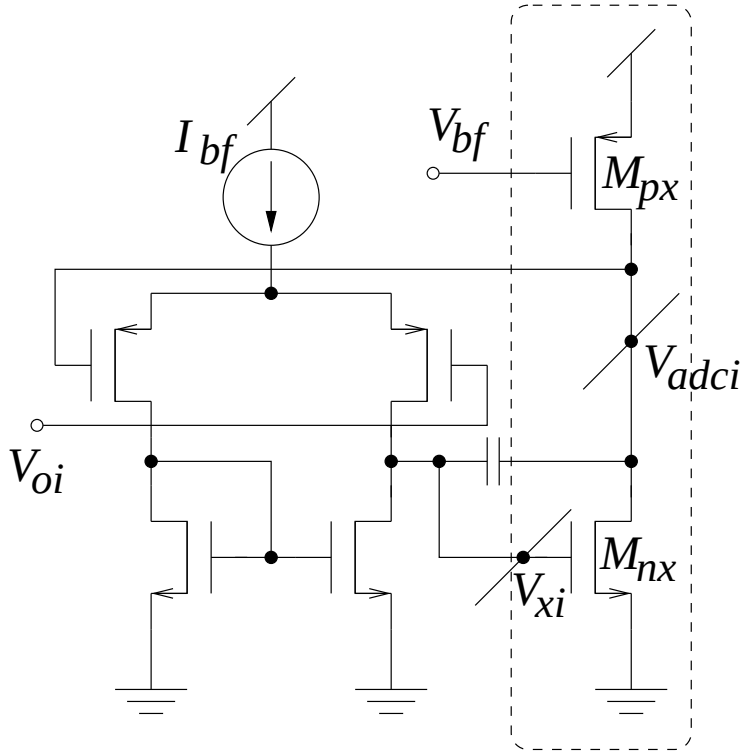

AER out
Address
Rqst
Ack
Pixel Array
Programmable Current Biasing (IPOTS)
Preamplifier Biasing Row

(a)


128
2
1
Replica of photodetector
Replica of preamplifier stage
Subpico ampere current mirror
Modified Replica of photodetector

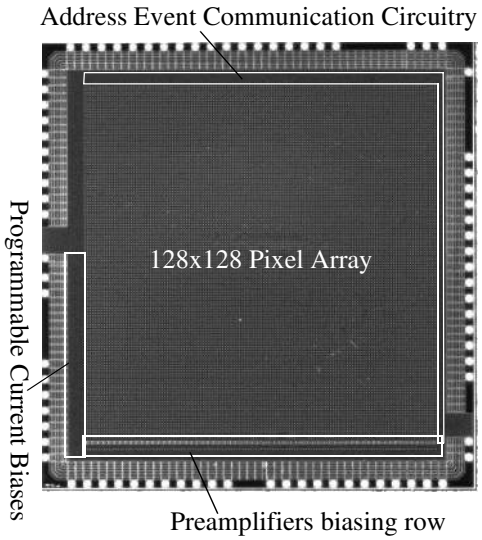
(b)

Figure 2

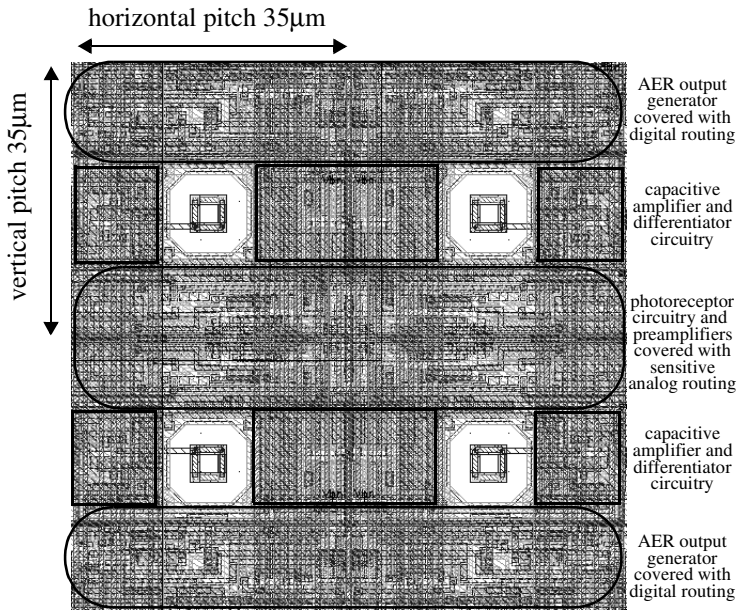


(c)

Figure 2


Address Event Communication Circuitry
128x128 Pixel Array
Programmable Current Biases
Preamplifiers biasing row

(a)


horizontal pitch 35µm
vertical pitch 35µm
AER output generator covered with digital routing
capacitive amplifier and differentiator circuitry
photoreceptor circuitry and preamplifiers covered with sensitive analog routing
capacitive amplifier and differentiator circuitry
AER output generator covered with digital routing

(b)

Figure 3

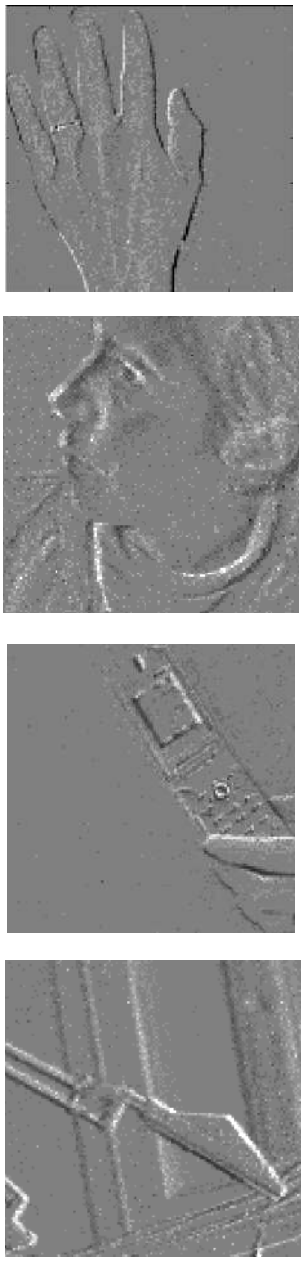
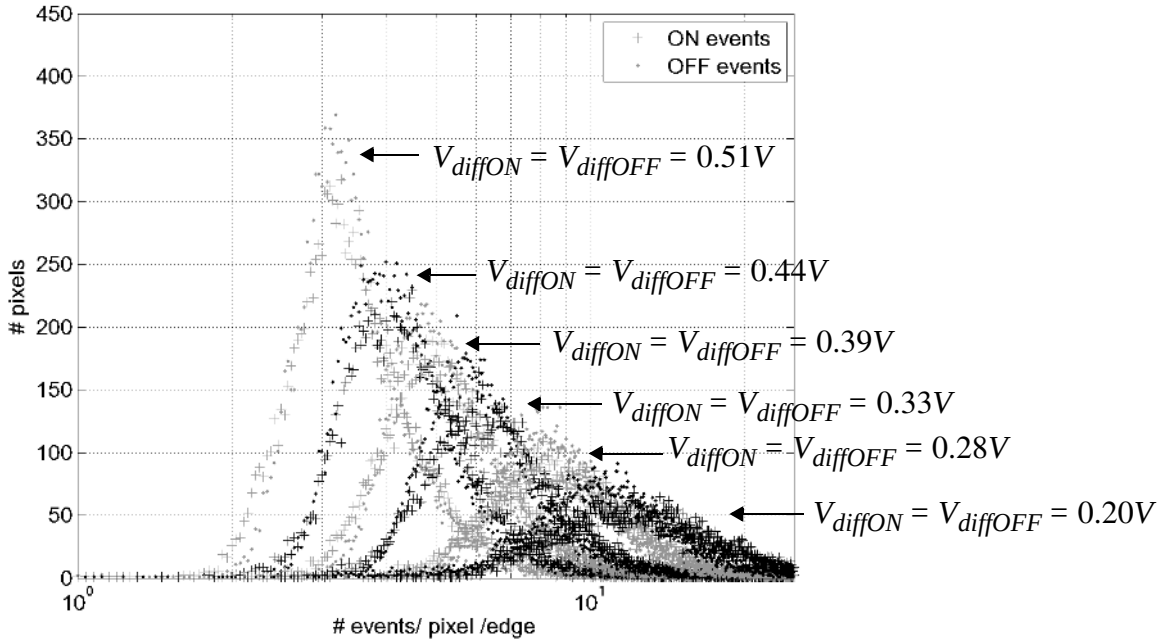
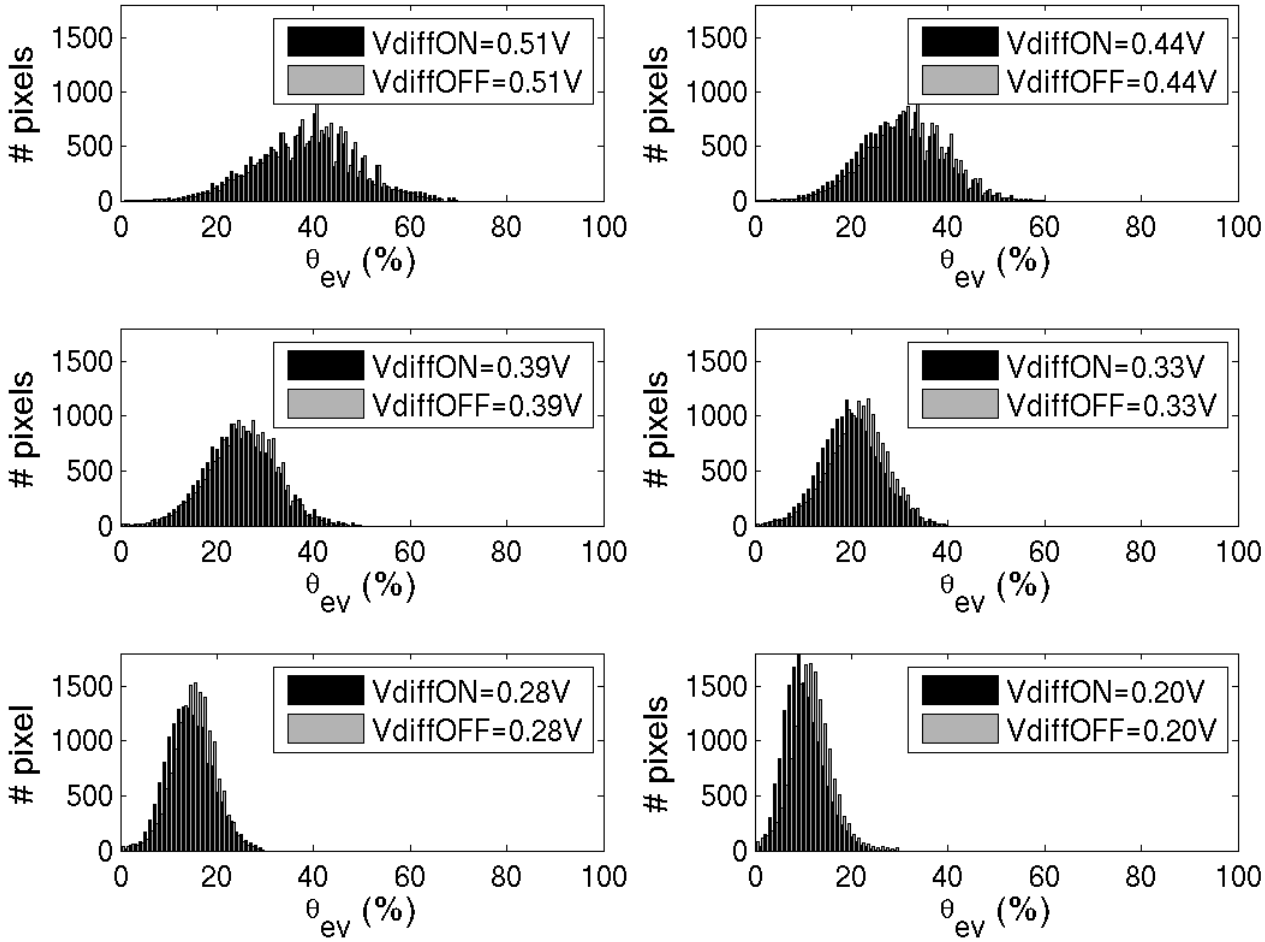


Figure 4.

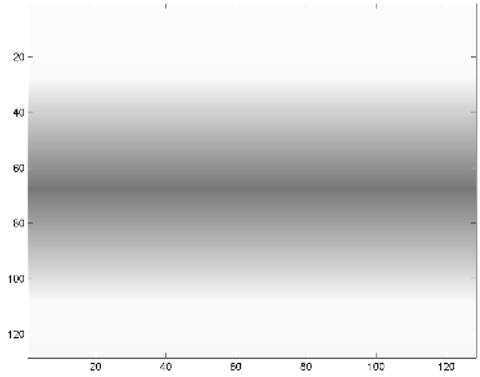
(a)


ON events
OFF events
$V_{diffON} = V_{diffOFF} = 0.51V$
$V_{diffON} = V_{diffOFF} = 0.44V$
$V_{diffON} = V_{diffOFF} = 0.39V$
$V_{diffON} = V_{diffOFF} = 0.33V$
$V_{diffON} = V_{diffOFF} = 0.28V$
$V_{diffON} = V_{diffOFF} = 0.20V$
pixels
events/ pixel /edge


VdiffON=0.51V
VdiffOFF=0.51V
VdiffON=0.44V
VdiffOFF=0.44V
VdiffON=0.39V
VdiffOFF=0.39V
VdiffON=0.33V
VdiffOFF=0.33V
VdiffON=0.28V
VdiffOFF=0.28V
VdiffON=0.20V
VdiffOFF=0.20V
# pixels
# pixel
θ_{ev} (%)

(b)

Figure 5



(c)

Figure 5

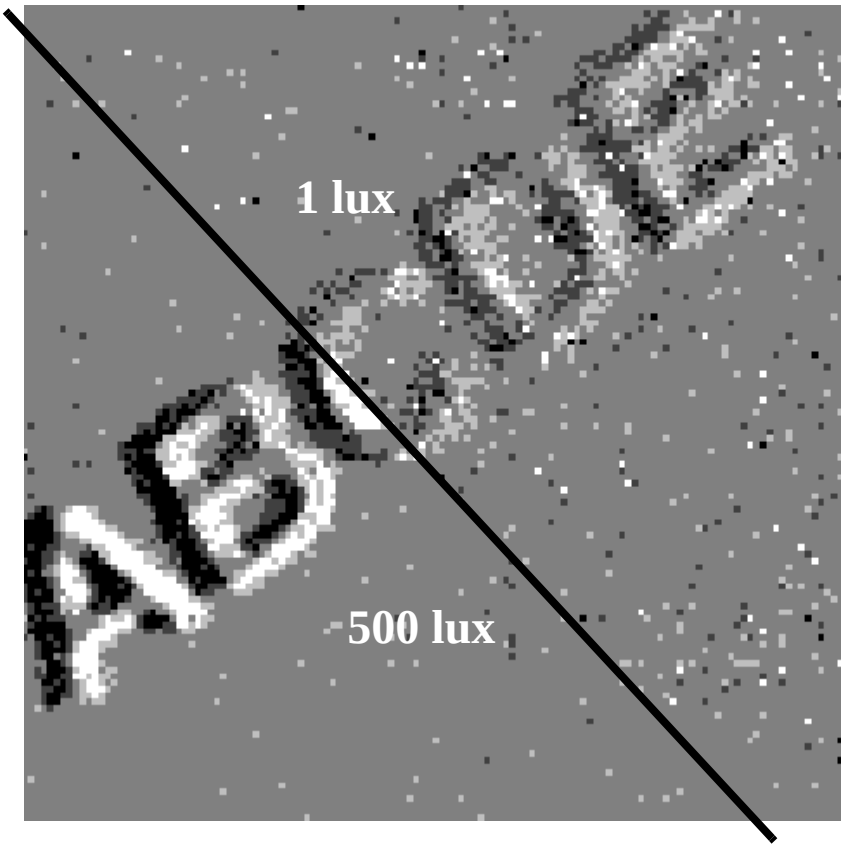


Figure 6

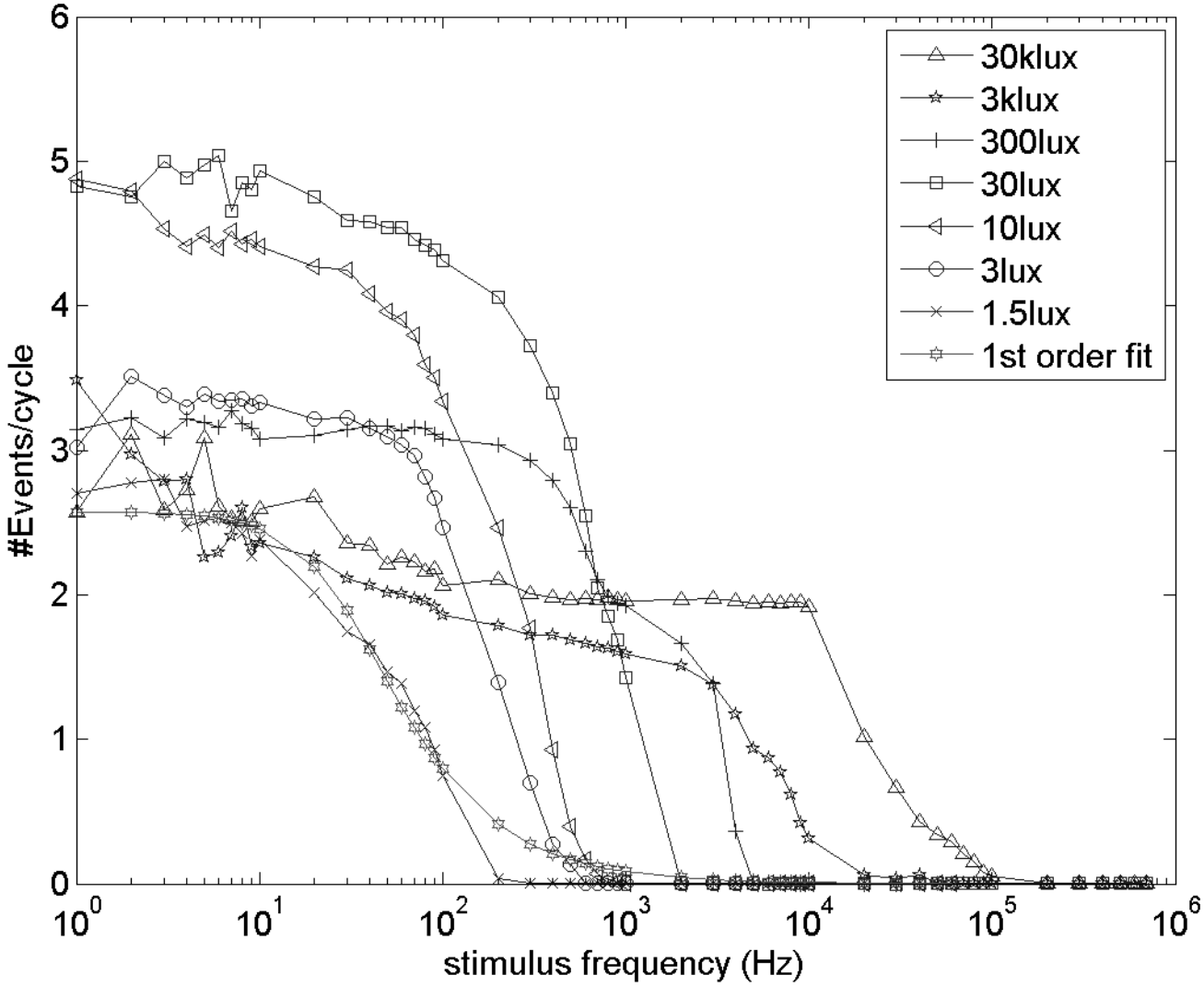

#Events/cycle
stimulus frequency (Hz)
30klux
3klux
300lux
30lux
10lux
3lux
1.5lux
1st order fit
0
1
2
3
4
5
6
10^0
10^1
10^2
10^3
10^4
10^5
10^6

Figure 7(a)

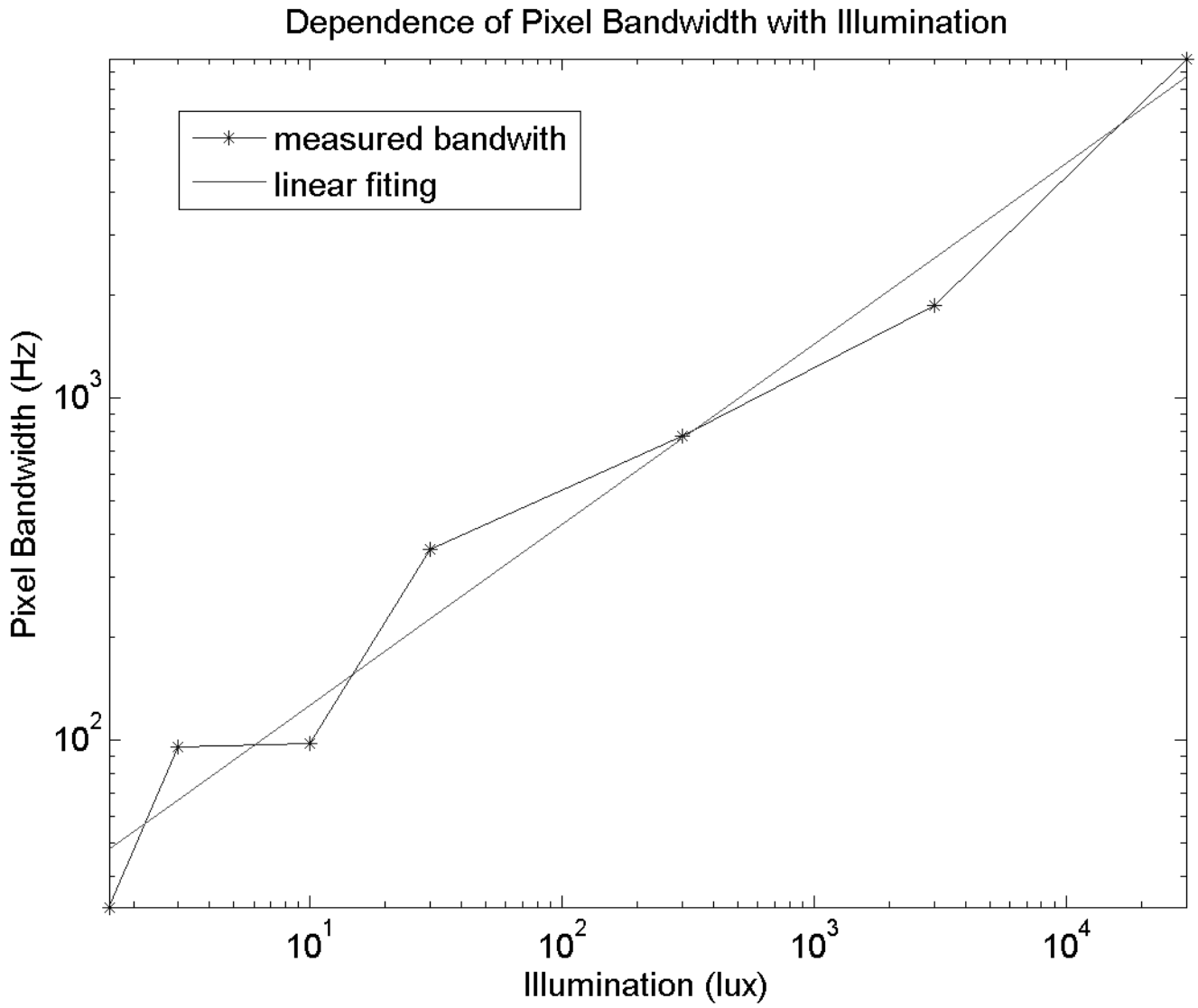

Dependence of Pixel Bandwidth with Illumination
measured bandwith
linear fiting
Pixel Bandwidth (Hz)
10^3
10^2
10^1
10^2
10^3
10^4
Illumination (lux)

Figure 7(b)

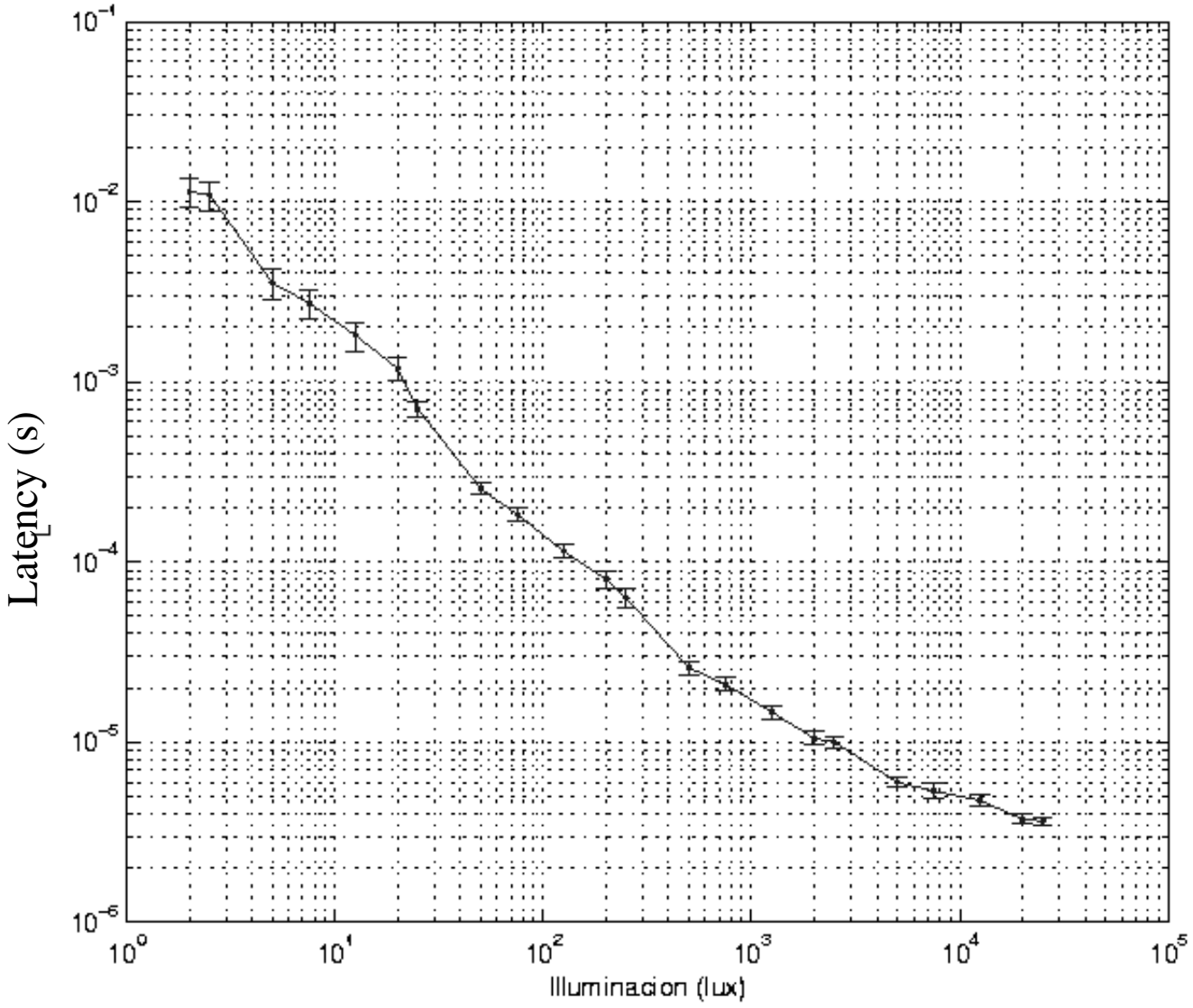
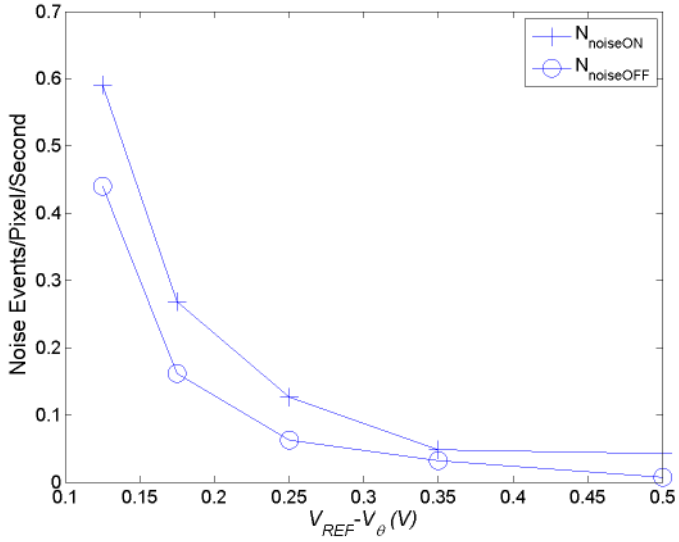

Latency (s)
10^{-1}
10^{-2}
10^{-3}
10^{-4}
10^{-5}
10^{-6}
10^{0}
10^{1}
10^{2}
10^{3}
10^{4}
10^{5}
Illumination (lux)

Figure 7(c)

(a)


Noise Events/Pixel/Second
V_{REF}-V_θ (V)
$N_{noiseON}$
$N_{noiseOFF}$

(b)

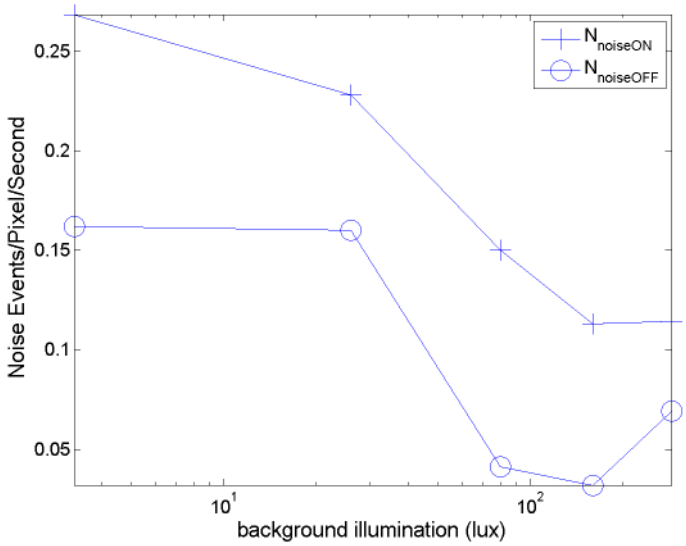

Noise Events/Pixel/Second
background illumination (lux)
$N_{noiseON}$
$N_{noiseOFF}$

Figure 8

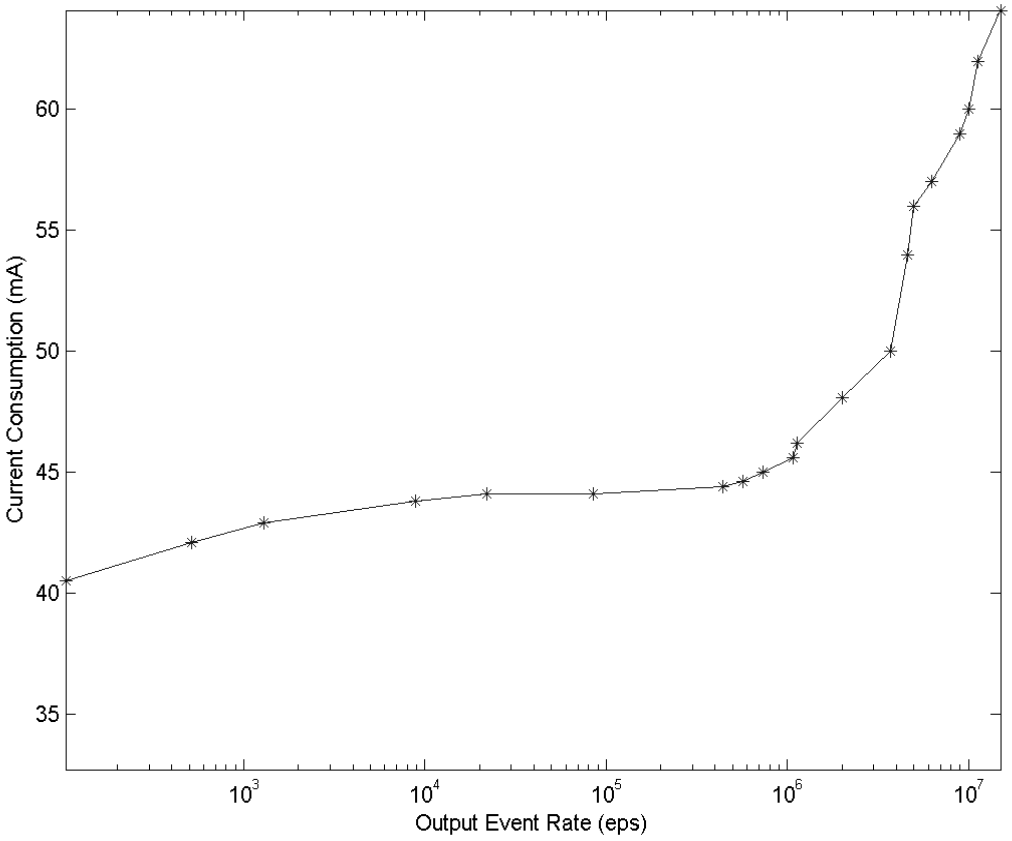

Current Consumption (mA)
60
55
50
45
40
35
10^3
10^4
10^5
10^6
10^7
Output Event Rate (eps)

Figure 9

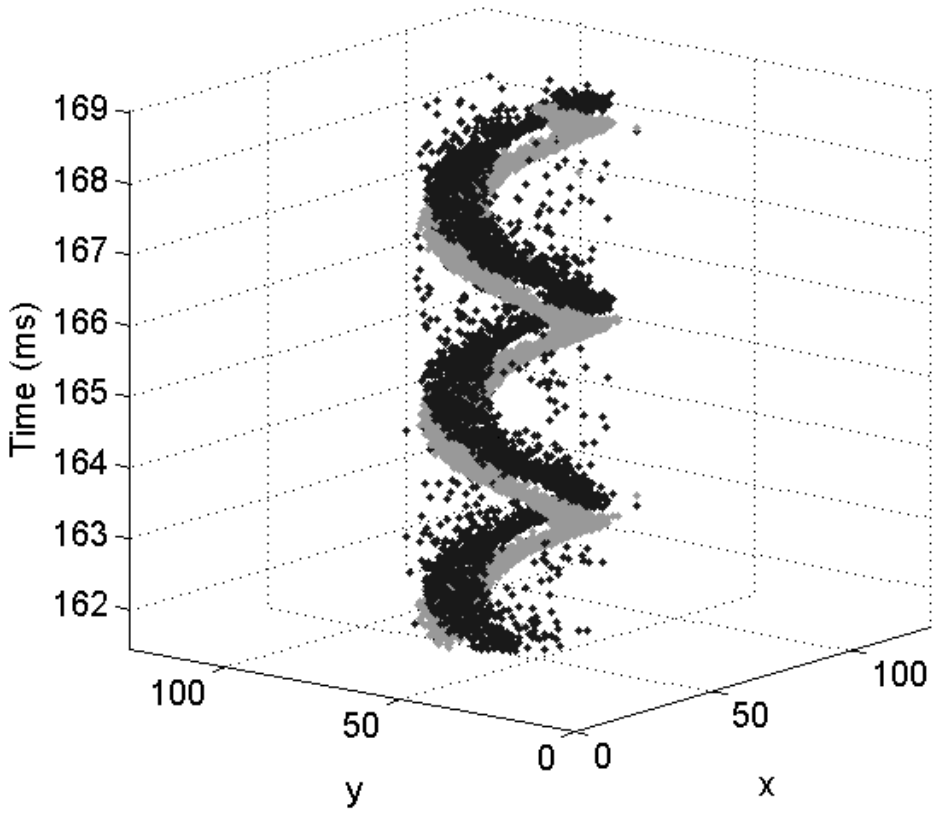
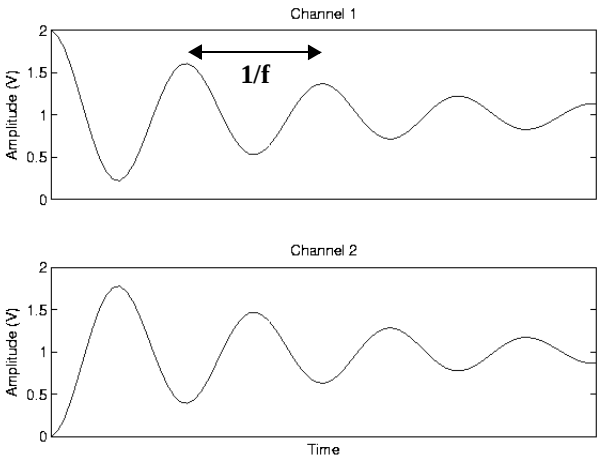
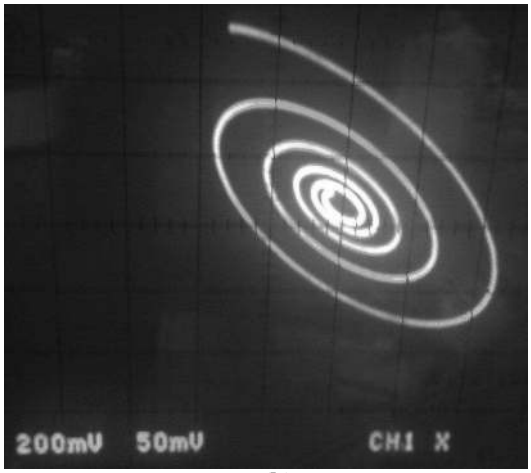


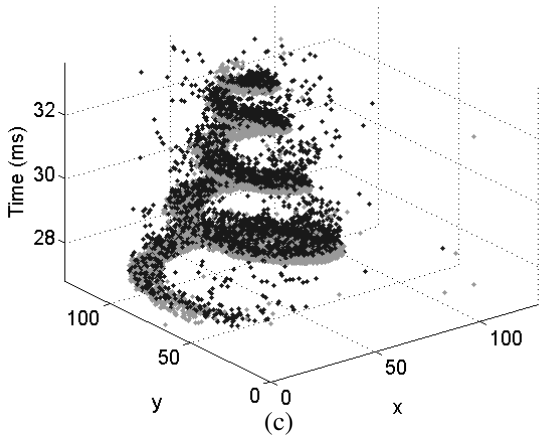
Figure 10



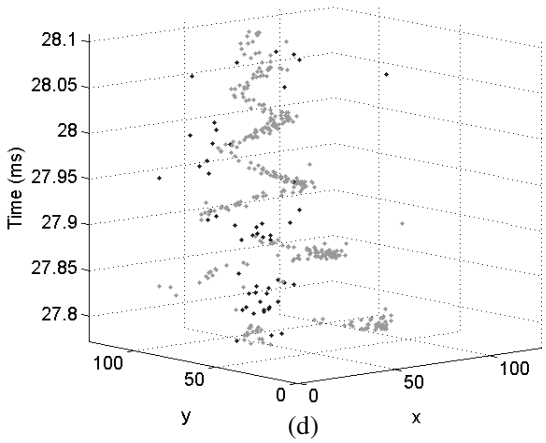
(a)



(b)



(c)



(d)

Figure 11

List of figure captions

Fig. 1. (a) Conceptual block diagram of pixel (b) schematic of the photoreceptor block, and (c) schematic of the preamplifier block

Fig. 2. (a) System level architecture. (b) Schematic of a preamplifier biasing cell. This cell is repeated 128 times along a row. (c) Detail of feedback amplifiers A_{f1} and A_{f2} in (b).

Fig. 3. (a) Microphotograph of the fabricated prototype, and (b) layout of the arrangement of 4 pixels.

Fig. 4. Sample images created by histogramming events. (a) Moving hand. (b) Moving head. (c) Moving cellular phone. (d) Moving camera watching lamp in front of window where outside object can be seen.

Fig. 5. (a) Histograms of the number of events generated per pixel per edge presentation for different threshold settings, and, (b) distribution of the positive and negative pixel contrast threshold for different settings of the threshold voltages. (c) Stimulus bar used with the TFT monitor.

Fig. 6. Snapshot capture for a factor 500 of intrascene illumination (1 to 500 lux)

Fig. 7. (a) Measured transfer function of the events per cycle as a function of the sinusoid frequency for different values of the illumination, (b) transfer function pole location at a function of the illumination, and (c) measured latency and latency deviation (error bars) versus the illumination.

Fig. 8. Noise characterizations. Average noise events generated per pixel per second (a) as function of threshold settings for 3lux illumination, and (b) as function of illumination for $|V_{REF} - V\theta| = 175mV$.

Fig. 9. Measured power consumption as a function of output event rate

Fig. 10. Spatio-temporal representation of events generated by rotating dot at 400Hz

Fig. 11. (a) Input signals applied to oscilloscope X-Y channels, and (b) corresponding trace in the oscilloscope display in X-Y mode captured with a commercial photograph camera. (c) Spatio-temporal representation of captured positive and negative events when the input stimulus is an spiral generated on the oscilloscope at a frequency of 500Hz, (d) and 10KHz.