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A 3-D Integrated Intra-Chip Free-Space Optical Interconnect for Many-Core Chips

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Abstract—This paper presents a new optical interconnect system for intra-chip communications based on free-space optics. It provides all-to-all direct communications using dedicated lasers and photodetectors, hence avoiding packet switching while offering ultra-low latency and scalable bandwidth. A technology demonstration prototype is built on a circuit board using fabricated germanium photodetectors, micro-lenses, commercial vertical-cavity surface-emitting lasers, and micro-mirrors. Transmission loss in an optical link of 10-mm distance and crosstalk between two adjacent links are measured as 5 dB and -26 dB, respectively. The measured small-signal bandwidth of the link is 10 GHz.

I. INTRODUCTION

Continuing device scaling, if not compensated, degrades performance and signal integrity of on-chip metal interconnects, hence limiting the performance of many-core microprocessors and high-speed systems-on-chip (SoC). The communications-centric nature of future high performance computing devices demands a fundamental change in intra- and inter-chip interconnect technologies. Optical interconnect exhibits inherent advantages in delay and bandwidth, hence eliminating the main limitations of its electrical counterparts [1], [2]. The key for optical interconnect's success is to lower power consumption and minimize the system complexity overhead.

Several signaling and networking schemes have been proposed for intra-chip optical interconnect. Applying a conventional packet-switching interconnect architecture to optical networks requires repeated electro-optic (E/O) and optoelectronic (O/E) conversions, diminishing the advantages of optical signaling. To avoid packet-switching, bus or ring structures can be used, which rely on wavelength division multiplexing (WDM) to achieve large bandwidth [3], [4]. These systems, however, typically require precise E/O modulators with accurate wavelengths and minimal transmission losses, hence difficult to realize in large-scale systems. In comparison,

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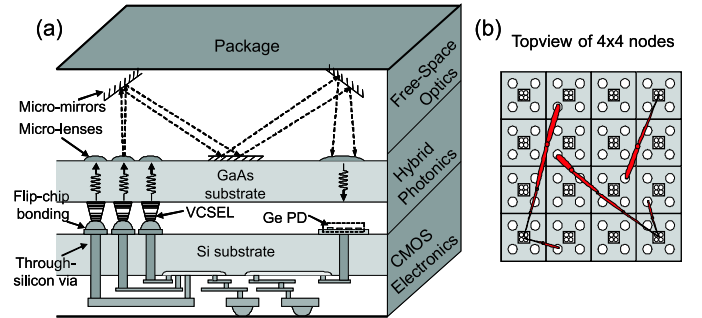


Fig. 1. (a) Cross-sectional and (b) top view of an intra-chip free-space optical interconnect system in a 3-D integrated chip stack. The VCSEL arrays are in the center and the photodetectors are on the periphery within each node.

inter-chip optical interconnect mostly rely on point-to-point links using directly modulated lasers integrated above silicon chips and waveguides integrated on the circuit board [5], [6].

Alternatively, free space optics can be used instead of waveguides in optical interconnect to eliminate the routing/networking complexity. Vertical-cavity surface-emitting lasers (VCSELs) and normal-incidence photodetectors (PDs) can be linked by a free-space optics fabric made of mirrors and lenses. For example, systems based on planar optics [7], macro-optics [8], [9], and microoptics [10], [11] have been demonstrated for inter- and intra-chip applications.

In this paper, we propose a new optical interconnect system specifically developed for intra-chip communications in many-core microprocessors and SoCs based on free space optics. Different from earlier work, this is a multidisciplinary approach that synergistically integrate photonics devices, circuits and optics with system and architecture design.

II. INTRA-CHIP FREE-SPACE OPTICAL INTERCONNECT

In the proposed intra-chip optical interconnect system, GaAs photonics and free-space optics layers are placed on top of the CMOS electronics layer via 3-D integration (Fig. 1). VCSELs in the GaAs photonics layer serve as light sources, hence removing the need for external multi-wavelength lasers used in WDM systems. Each light beam from the digitally modulated, backside-emitting VCSELs is collimated through a dedicated micro-lens, built at the back of the GaAs substrate, which is transparent at the target wavelength. The collimated light bounces from a series of micro-mirrors, implemented on the chip package using low-loss metal coatings. Then, it is focused by another micro-lens onto a PD, built with a thin germanium (Ge) layer on the silicon substrate. In the electronics layer, the

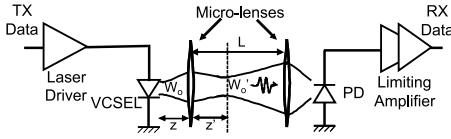


Fig. 2. Intra-chip FSOI link schematic.

transmit and received electrical signals are converted from/to digital data by the transceiver electronics.

This *free-space optical interconnect* (FSOI) system uses point-to-point links to construct an all-to-all intra-chip communication network. Multi-bounce beam guiding scheme enables a single thin transmission medium to provide free-space links between every VCSEL-PD pair at arbitrary locations. Hence, it offers significant signaling and networking advantages over electrical and other optical interconnects. First, FSOI avoids packet-switching and the associated intermediate routing and buffering delays in electrical networks or packet-switching optical networks. Hence, it exhibits low propagation delay, providing low latency. In addition, the communication links are formed in a fully distributed fashion with minimal arbitration, reducing the arbitration latency in large-scale systems. Second, it exhibits low loss, minimal dispersion and no bandwidth degradation regardless of topological distance. It eliminates the loss and crosstalk due to large number of waveguide crossings in densely routed waveguide-based optical interconnects, which limit the optical network performance. Third, it saves significant amount of energy by a) eliminating packet-switching related energy consumption, b) powering VCSELs down in low duty-cycle operation, and c) avoiding thermal tuning of sensitive E/O modulators in WDM systems. Fourth, the fully distributed nature of FSOI renders this scheme highly scalable (see Sec.III-d). In addition, placing optics and electronics on separate planes accommodates their different technological and scaling constraints. Finally, FSOI's good signal integrity simplifies optical transceiver electronics, e.g., removing the need for equalization in high-speed electrical interconnects.

III. FSOI DESIGN

In the following, we demonstrate the design of the proposed FSOI system within a typical many-core microprocessor. The target chip is assumed to have $2.3 \times 2.3\text{-cm}^2$ area, the chip size for high performance processors at introduction [12]. The VCSELs have $20\text{-}\mu\text{m}$ device size and $5\text{-}\mu\text{m}$ aperture size. The $47 \times 47\text{-}\mu\text{m}^2$ PDs are based on our fabricated Ge-on-Si PDs (see Sec.IV). The micro-lenses and micro-mirror sizes are scaled with the number of nodes (see Sec.III-d). Predicting technology model (PTM) [13] is used for transistor models.

a) Optics: The optical wavelength is chosen as 980 nm, a good compromise between GaAs VCSEL and Ge PD performance. At this wavelength, the far field $1/e^2$ VCSEL full-angle divergence is estimated as 16° . Micro-lenses at the backside of a $625\text{-}\mu\text{m}$ thick GaAs substrate, each of which has an aperture size three times of the beam radius [10], are covered with SiN anti-reflection coating to eliminate 1.5-dB/lens loss due to reflections at the air/GaAs interface. These micro-lenses can be fabricated using regular photolithography because of their

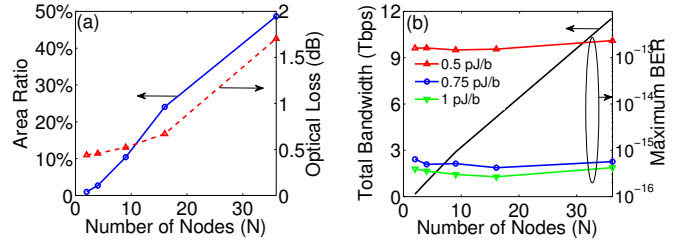


Fig. 3. (a) The area coverage ratio of VCSELs, PDs and the maximum optical path loss, and (b) BER and bandwidth at different energy efficiencies with respect to number of nodes.

small thickness (as compared to [8]). Correspondingly, the required GaAs substrate thickness is small and hence, easy for wafer-level bonding. Gold coated mirrors with 98% reflection (0.09-dB loss) are placed 1 mm from the micro-lenses on the package and at the backside of the GaAs substrate.

b) Signaling: To evaluate interconnect performance, a single-bit FSOI link is analyzed for the longest optical path of 3.24 cm, corresponding to a 115-ps latency, which is diagonally crossing the chip with five bounces from the mirror. Based on device simulation in DAVINCI, the VCSEL exhibits a $170\text{-}\Omega$ differential series resistance and 76-fF capacitance with a threshold current of 0.15 mA; the PD has a 0.4-A/W responsivity at 980 nm with 40-fF capacitance. As shown in Figure 2, a CMOS optical transceiver is designed using 16-nm PTM device parameters. The link bandwidth is calculated as 13 GHz for 0.4-mW optical power, and the BER is less than 10^{-12} with 0.5-pJ/b energy efficiency at 10-Gb/s data rate.

c) Networking: There are N communication nodes in this system, and each link between a pair of nodes has 8 bits. Hence, each node has $(N - 1) \times 8$ VCSELs. To utilize the sporadic nature of intra-chip communications and to save chip area, each node has 4×8 PDs. By intentionally avoiding arbitration, data collision at PDs is allowed, and is detected by the microprocessor; then a confirmation signal is sent to the transmit node through a separate VCSEL-PD link to retransmit the data [14]. Given a data rate of 10-Gbps per VCSEL-PD pair, the bandwidth of a 8-bit link is 80 Gbps, and aggregated interconnect system bandwidth is $N \times 320$ Gbps.

d) Scaling: A state-of-the-art microprocessor at 45-nm technology has 8 cores, doubling every generation, increasing to 128 at 11-nm technology node in a $2.3 \times 2.3\text{-cm}^2$ fixed chip area. In our system, a communication node is shared between four adjacent cores, similar to [4]. In this one-lens-per-bit design, the area occupied by the optical components depends on the lens sizes. To facilitate the mirror placement, less than half of the chip area is covered by micro-lenses. PD lens is fixed at $250\text{ }\mu\text{m}$ for all number of nodes, whereas VCSEL lens scales from $250\text{ }\mu\text{m}$ for 2 nodes to $136\text{ }\mu\text{m}$ for 36 nodes. Correspondingly, it achieves maximum bandwidth densities of 4 Tbps/cm² and 6.25 Tbps/cm², respectively, limited by the Gaussian beam divergence. For 36 nodes, the system can achieve a maximum path loss of 1.7 dB and area coverage of 48% (Fig. 3-a) with a BER below 10^{-12} at 0.5-pJ/b energy efficiency and 10-Tbps aggregate bandwidth (Fig. 3-b). Therefore, this scheme can be applied to chips with 144 cores, corresponding to 11-nm node on the technology

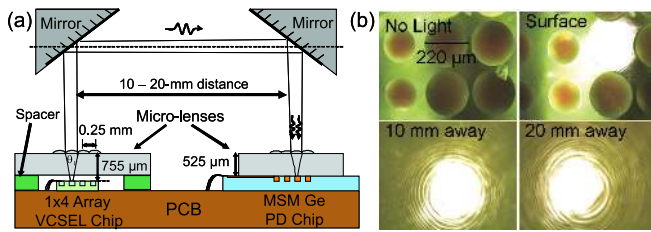


Fig. 4. (a) 2-D cross-section of FSOI, and (b) image of the beam collimated by VCSEL lens at different distances. The beam size is $240\ \mu\text{m}$ and $250\ \mu\text{m}$, corresponding to 1.5 and 1.9-dB clipping losses at 1 cm and 2 cm, respectively.

roadmap. For larger chip size, number of nodes or number of bits, micro-lenses with larger numerical aperture (NA) can be built on a thicker GaAs or fused silica substrate and used for all VCSELs in a 8-bit link, i.e. one-lens-per-link, to enable larger bandwidth density.

IV. PROTOTYPE AND FSOI MEASUREMENT RESULTS

A prototype FSOI system is built on a printed circuit board (PCB) using micro-lenses, micro-mirrors, PDs, and VCSELs. The VCSELs are a commercial 1×4 array (Finisar HFE8004-103), with 2-mW optical power at 850 nm, 40% conversion efficiency, 30° full-angle beam divergence and 10-Gb/s speed. The micro-lenses are built on a $525\text{-}\mu\text{m}$ thick fused silica substrate by melting and reflowing the $10\text{-}\mu\text{m}$ thick and $220\text{-}\mu\text{m}$ diameter cylindrical photoresist, limited by the $250\text{-}\mu\text{m}$ VCSEL-to-VCSEL pitch size. The resultant spherical shape has a 1.22-mm radius of curvature and a corresponding focal point of $730\ \mu\text{m}$ from the surface of the lenslet. The fabricated 1×4 array PDs are $47 \times 47\text{-}\mu\text{m}^2$ metal-semiconductor-metal Ge PDs with a thin layer of undoped amorphous-silicon on the substrate, enabling low dark current and large bandwidth. The PD has a 0.23-A/W responsivity without anti-reflection coating and a 13-GHz bandwidth at 7-V bias and 850 nm [15].

As shown in Figure 4, the VCSELs and PDs are wirebonded to the PCBs with $50\text{-}\Omega$ transmission lines, connected to the instruments via RF connectors at the edge. Two micro-lens arrays are UV-cured to spacers on top of the VCSELs with a sufficiently wide gap for the wirebonds, and directly onto PDs. The VCSEL chip is $230\ \mu\text{m}$ from the back surface and $25\ \mu\text{m}$ from the focal point of the lens. The 96% reflective mirrors are mounted 1 mm away from the top of the micro-lenses with 45° angle. The optical transmission for a specific link and the optical crosstalk of adjacent links with respect to distance are shown in Fig. 5-a. At 0.5-mW laser optical power, the transmission loss is 5 dB at a 10-mm distance and increases to 6.5 dB at 26 mm. The crosstalk power is -29 dB at 10 mm and increases to -25 dB at 26 mm. The small-signal bandwidth of the link is measured as 10-GHz and does not change with distance (Fig. 5-b). 1.25-dB and 1.5-dB optical power clipped at the VCSEL lens and PD lens at 1 cm are predominantly due to the large divergence angle of the commercial VCSEL in conjunction with the small NA of the lenses. To eliminate these clipping losses, smaller VCSEL beam divergence and/or a larger aperture size lenses with the larger focal length can be used at both ends [10]. The reflection losses can be mitigated by using low-loss metal for mirrors and anti-reflection coating on the lenses.

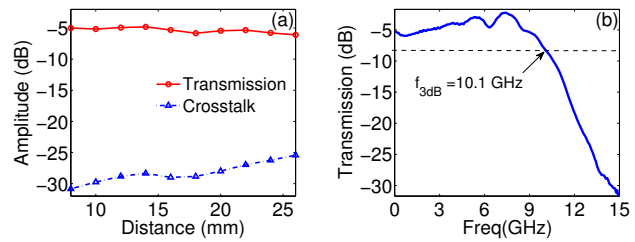


Fig. 5. (a) Transmission and crosstalk at different link distances, and (b) small-signal bandwidth at $L=1\ \text{cm}$. Note that the optical transmission changes between -5 and -6.5 dB due to the little change in the beam spot size.

V. CONCLUSION

A novel intra-chip optical interconnect system using free-space optics and 3-D integrated photonic devices is proposed for many-core processors and SoCs. This system achieves direct communications between individual cores with low latency and loss, while enabling a scalable bandwidth. For technology demonstration purposes, a prototype using individual arrays of VCSELs, micro-lenses, micro-mirrors, and photodetectors has been built on a PCB carrier. The prototype achieves less than 6.5-dB loss and -25-dB crosstalk power up to 2.6 cm with more than 10-GHz bandwidth.

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