A 3-Gb/s Optical Detector in Standard CMOS for 850-nm Optical Communication

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***Abstract*—This paper presents a monolithic optical detector, consisting of an integrated photodiode and a preamplifier in a standard 0.18-μm CMOS technology. A data rate of 3 Gb/s at BER $< 10^{-11}$ was achieved for $\lambda = 850$ nm with 25-μW peak-peak optical power. This data rate is more than four times than that of current state-of-the-art optical detectors in standard CMOS reported so far. High-speed operation is achieved without reducing circuit responsivity by using an inherently robust analog equalizer that compensates (in gain and phase) for the photodiode roll-off over more than three decades. The presented solution is applicable to various photodiode structures, wavelengths, and CMOS generations.**

***Index Terms*—CMOS analog integrated circuits, data communication, equalizers, optical communication, optical receivers, photodiodes, robustness issues.**

I. Introduction

FOR long-distance data communication channels, high-speed fiber-optic links have replaced electrical interconnections. Nowadays, detectors for long-haul optical communication are mainly multidie solutions implemented in dedicated (and therefore expensive) technologies such as GaAs [1], [2] and InP–InGaAs [3]–[5]. The use of these expensive systems is justified by the large number of users per channel: the cost per user is low.

For short-distance communication (e.g., LAN, board-to-board, and chip-to-chip), the communication channels are typically not shared by multiple users. Especially, for these applications, cost aspects are crucial, and hence the long-haul solutions cannot be used. To enable cost-effective implementation of optical short-distance interconnect, low-cost plastic fibers, lasers, and standard technologies to implement the electronics should be used, which already determines a number of boundary conditions for the optical system. First, the core diameter of low-cost plastic fibers is about 50 μm which fixes the photodiode area in optical detectors to about 50 μm $\times$ 50 μm. Second, the lasers that can be used in combination with silicon photodiodes, for high data rates, all operate at relatively long wavelengths. Nowadays, fast lasers at the lower end of the wavelength spectrum operate at 850 nm; the work in this paper uses these 850-nm lasers. Third, because of the low cost requirement for the electronics, the complete optical detector must preferably be fully implementable in today's mainstream technology: CMOS. This will not only enable optical communication directly to CMOS chips, but also opens the possibility to (cost-effectively) implement matrices of optical detectors on a single CMOS chip that operates on many parallel optical channels. An important associated advantage of fully integrated optical detectors is that ground-bounce issues, ESD problems, and bond-wire induced problems (that may be encountered with electrical input signals, including electrical connections in a multidie optical detector/front-end) are largely eliminated.

The major roadblock in current integrated optical detectors in standard CMOS technology is the too-low data rate at conventional wavelengths: for straightforward implementations in standard CMOS technology, the bit rate is limited to tens of Mb/s, see, e.g., [6] for a short discussion. This low speed is intrinsic to silicon photodiodes, due to the occurrence of slow diffusive carriers. These slow diffusive carriers are carriers that are generated relatively deep in the silicon and diffuse slowly to the depletion layer in the photodiode where the actual detection takes place.

In literature, a number of ways to boost the speed in monolithically integrated detectors in CMOS can be found; all methods try to eliminate the slow diffusive carriers. Most of these methods require nonstandard CMOS technology, which is in clear contradiction with the monolithical integration aspect. In [7], a buried oxide layer is added to standard CMOS to prevent charge from slowly diffusing back to the junction. A similar solution is presented in [8] where the optical receiver is implemented in SOI. Other solutions include the generation of a very thick depletion layer by applying high voltages or by the introduction of very lightly doped layers [6], [9]–[11]. A different way to effectively cancel the effect of slowly diffusive carriers in fully standard CMOS without the need for very high voltages is presented in [12] and [13] and achieves 700 Mb/s by subtraction of two diode responses. This solution increases the bit rate considerably, but comes at the cost of lowered responsivity and sensitivity. For stand-alone applications non-CMOS technologies like BiCMOS may be preferred due to their intrinsically better properties for optical receivers;[1] a good overview is given in, e.g., [14]. However, these non-CMOS implementations clearly cannot be monolithically integrated in larger (CMOS) ICs.

In this paper, we present a high-speed optical detector that can be implemented in fully standard CMOS technology [15].

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[1]Technologies such as BiCMOS have a number of advantages compared to CMOS. First, the supply voltage typically is well above that for nowadays CMOS which can be used to speed up photodiodes. Second, an on-chip charge-pump can be used to boost the voltages even more. Third, usually these processes offer a multitude of layers, e.g., buried layers, that can be used to eliminate slow carriers and in this way speed up the photodiode's response.

The overall speed is more than four times higher than that of the state-of-the-art CMOS optical receivers in [12] and [13] without a sensitivity or responsivity penalty. This results in measured 3-Gb/s data rates for $\lambda = 850$ nm at -19 dBm optical power and BER $= 10^{-11}$.

The paper is organized as follows. Section II presents analyses of the frequency behavior of a CMOS photodiode. It will be shown that, for $\lambda = 850$ nm, the diode bandwidth is in the low megahertz range, which presents the main speed bottleneck of a monolithic optical receiver in CMOS. Sections III and IV present the system-level design and the circuit-level design, respectively, of a preamplifier circuit including an analog equalizer. The presented circuit enables the usage of the slow silicon photodiodes for data rates in the low gigahertz range, without reducing responsivity. Section V discusses robustness issues for the designed circuit; it will be shown that this analog equalization is inherently robust. Also, the impact of different wavelengths is briefly discussed. Section VI discusses usage of different CMOS generations. Section VII presents a number of measurements that illustrate correct operation and robustness or the proposed method. Section VIII concludes this paper.

II. Bandwidth of CMOS Photodiodes

The bandwidth of photodiodes can be broken down into two components: intrinsic and extrinsic bandwidth. The *intrinsic bandwidth* is related to the physical speed at which optically generated carriers are collected by the photodiode; this speed is limited by diffusion and drift of carriers and will be discussed in Section II-A. The *extrinsic bandwidth* corresponds to the in-circuit electrical bandwidth and hence is determined by the photodiode's capacitance and the input impedance of the preamplifier; a short discussion is given in Section II-B.

A. Intrinsic Photodiode Bandwidth

In CMOS, just a few different photodiode structures can be realized: there are typically two types of wells (n-well and p-well) and two types of shallow implants (n+ and p+) that are typically used for source and drain diffusions. Other implants (e.g., Vt-adjust, halo, pockets, and ...) are typically implanted using the well masks or the shallow implant masks and therefore cannot be used separately; they will be ignored in this paper. For the analyses in this section, p-type substrates are assumed, and the differences between high-resistive and low-resistive versions are briefly discussed. Using this set of standard CMOS implants, we can realize three different types of junctions that can be used to implement a photodiode:

- nwell/p-substrate, see Fig. 1;
- nwell/p+;
- pwell/n+.

Note that a photodiode may consist of multiple junction types, leading to, e.g., a p+/nwell/p-substrate photodiode. Each of the junctions has its own specific frequency behavior and size dependency; these will be reviewed briefly in the next subsections. More detailed analyses can be found in, e.g., [17]–[19] and [20]. A short summary and a benchmark of the various photodiodes are given in Section II-A4.

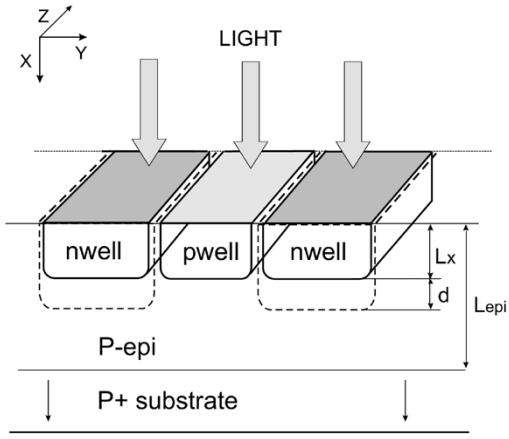

Fig. 1. Finger n-well/p-substrate photodiode with low-ohmic substrate in standard CMOS technology.

1) N-Well/P-Substrate Junction: The total photocurrent of any junction has three components: diffusion current in the n- and p-regions and drift current in the depletion layer in between. For the n-well/p-substrate junction, the total current is

$$i_{\text{int, total}} = i_{\text{diff, nwell}} + i_{\text{diff, p-sub}} + i_{\text{drift}}. \tag{1}$$

To get insight into physical bandwidth limitations, the photodiode response on a Dirac light pulse was calculated for every type of junction. The resulting excess carrier profiles and the corresponding current densities follow from the Laplace transform of the time-domain diffusion equation [12].

The *p-substrate diffusion current* component was solved using a one-dimensional (1-D) (vertical) diffusion equation. To estimate the difference between a high-ohmic substrate and a low-ohmic substrate, the construction in Fig. 1 is used: two p-substrate layers on top of each other. The upper layer is assumed to be high-ohmic and has a thickness L_{epi}, the lower layer is low-ohmic. With this, a finite L_{epi} corresponds to low-ohmic substrates, and an infinite L_{epi} complies with high-ohmic substrates. The boundary conditions for the diffusion equations follow from the continuity of both carrier densities and current density [21]; between the two substrate layers, it follows that

$$-qD_{n1}\frac{\partial n_1(x)}{\partial x}\bigg|_{x=L_{\text{epi}}} = -qD_{n2}\frac{\partial n_2(x)}{\partial x}\bigg|_{x=L_{\text{epi}}} \tag{2}$$

and

$$n_1(L_{\text{epi}}) = n_2(L_{\text{epi}}) \tag{3}$$

where D_{n1}, D_{n2} represent the diffusion coefficients and n_1 and n_2 are the density of the minority carriers in the high-ohmic and low-ohmic layers, respectively.

At $\lambda = 850$ nm, the absorption length in silicon is about 28 μm, which is much deeper than the depth of any junction. Consequently, most carriers are generated far away from junctions: deep inside the substrate. The impact of this is that both the substrate current is dominant in the overall photodiode response and that the speed of this substrate current is low.

For a typical 0.18-μm CMOS process, the -3-dB frequency is around 3.5 MHz for high-ohmic substrates. For low-ohmic

substrates, the thickness of the high-ohmic upper layer was assumed to be several microns, which yields a −3-dB frequency around a whopping 5 MHz. For both the high-ohmic and the low-ohmic substrates, the substrate current dominates the total photodiode response for frequencies up to several hundreds megahertz. The roll-off of the substrate current component ranges from about −3 dB/decade at lower frequencies to −10 dB/decade at higher frequencies.

The *n-well diffusion current* component was solved in two dimensions following a procedure similar to that in [12]. For the calculations, the photodiode surface is assumed to be reflective (i.e., the normal component of the gradient of the carrier density is zero) since the surface recombination process is slow compared to the frequencies of interest in this paper; the electron densities on the other three sides are assumed to be zero. It follows that the smallest dimension of the n-well (either the depth or the width) determines the bandwidth [12], [17]. For a 0.18-μm CMOS process and $\lambda = 850$ nm, the −3-dB frequency is between 450 MHz (for wide n-wells) to over 900 MHz (for narrow n-wells). The roll-off of this component of the overall response is about −10 dB/decade; this low roll-off results from the combined diffusion processes of the distributed generated carriers.

The *drift current* component is due to electron–hole pairs generated inside the depletion layer. It is usually assumed that carriers have the saturation velocity throughout the depletion layer. At constant velocity v_s, the bandwidth of the depletion layer is then about $f_{3\ \mathrm{dB\ drift}} = 0.4 \cdot (v_s)/(W_{\mathrm{depletion}})$ [16]. In this relation, $W_{\mathrm{depletion}}$ is the depletion layer's thickness. However, in our case, the junction that is dominant in the photocurrent, the n-well/p-substrate junction, is both lightly doped and weakly biased, for which case the generated carriers do not reach saturation speed. To get a more realistic bandwidth figure, we included the effects of the position-dependent electrical field in the depletion layer and of mobility reduction to estimate the average transit time and bandwidth.

For 0.18-μm CMOS, the estimated bandwidth of the drift current component is about 10 GHz, which is much higher than that of both diffusion currents. To roll-off at higher frequencies is about −10 dB/decade. In the remainder of this paper, any frequency dependency of this drift current is neglected for simplicity reasons.

Fig. 2 illustrates the physical effects that take place inside a p+/n-well/p-substrate photodiode, after illumination using a Dirac pulse at $t = 0$ with $\lambda = 850$ nm. The charge generated at $t = 0$ as a function of the depth into the silicon is represented by the upper (continuous) curve. Both the light intensity and the generated charge density decrease exponentially with the depth in the silicon. At 850-nm incident light, the intensity decreases by 50% every 9 μm, which is much larger than the depth of any junction in standard CMOS technology. For comparison reasons, the photodiode structure is sketched on scale below the graph. In Fig. 2, the simulated charge distributions at different time instances illustrate (in the time domain) the fast response of the p+/n-well junction, the somewhat slower response of the n-well, and the very slow response of the charge generated in the p-substrate. For illustration purposes, the time

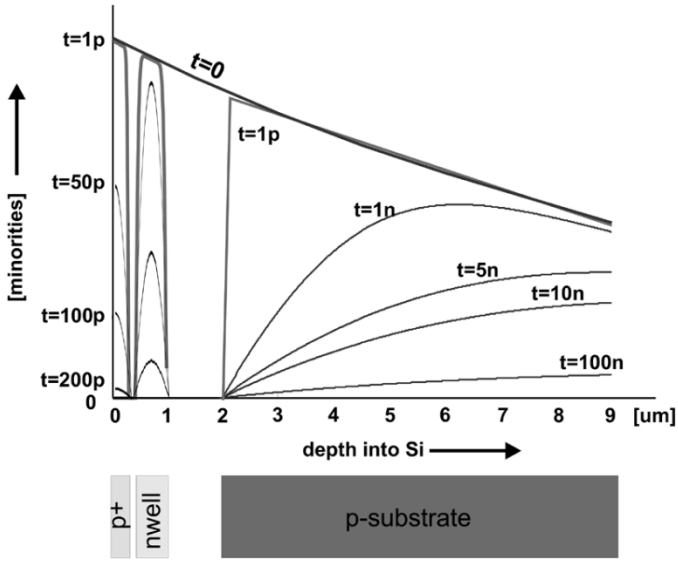

Fig. 2. Simulated charge distributions in a p+/n-well/p-substrate photodiode after illumination using a Dirac light pulse at $t = 0$, $\lambda = 850$ nm. The charge profiles at a number of time instances illustrate the speed of response in the time domain in different parts of the photodiode; photodiode dimensions are shown below the graph. Time instances are identical for the p+ and nwell part; but are different for the p-substrate profiles.

instances of the charge profiles in p+ and in the n-well are identical; the times in the p-substrate are quite different.

Fig. 3 shows the calculated intrinsic frequency responses of two finger n-well/p-substrate diodes in a standard 0.18-μm CMOS process. To clearly see the contributions of the various parts of the photodiodes, a breakdown into current components is also shown. Furthermore, two layout structures are assumed to illustrate the effect of the photodiode layout on the speed: one of these photodiodes therefore has a small n-well width (2 μm) and the other has a large n-well width. Note that the roll-off in the overall photodiode responses start around 1 MHz and ranges from about −3 to −5 dB/decade for over four decades.

The figure also illustrates that the photodiode layout only has a small effect on the overall response. This is because the layout mainly has an effect on the nondominant current components in the overall photodiode response.[2] It also follows from the calculations that using a low-ohmic substrate instead of an high-ohmic one increases the speed of the substrate current component by about 50%, which is due to the higher recombination rate in the low-ohmic regions.[3]

A typical match between calculations and measurements of photodiodes in 0.18-μm CMOS technology is shown in Fig. 4.

[2]For narrow n-wells not only is the bottom of the n-well relevant, but the sides of the n-well increase the charge gradient as well. This higher gradient speeds up the diffusion and hence speeds up the response. For n-wells much wider than the depth, there's no significant contribution of the sides of the n-well on the overall speed.

[3]In Fig. 2, this would correspond to a forced near-zero charge concentration in the low-ohmic bulk, starting right below the epilayer, typically a few microns deep into the silicon. The charge profile in the p-substrate would then be just a few microns deep, with zero concentration at the n-well-boundary and at the low-ohmic layer's edge. This is similar to the charge profile in the n-well region in Fig. 2. Overall diffusion in the p-substrate would be faster at the cost of responsivity: a lot of carriers diffuse downwards into the low-ohmic layer instead of in the direction of the n-well.

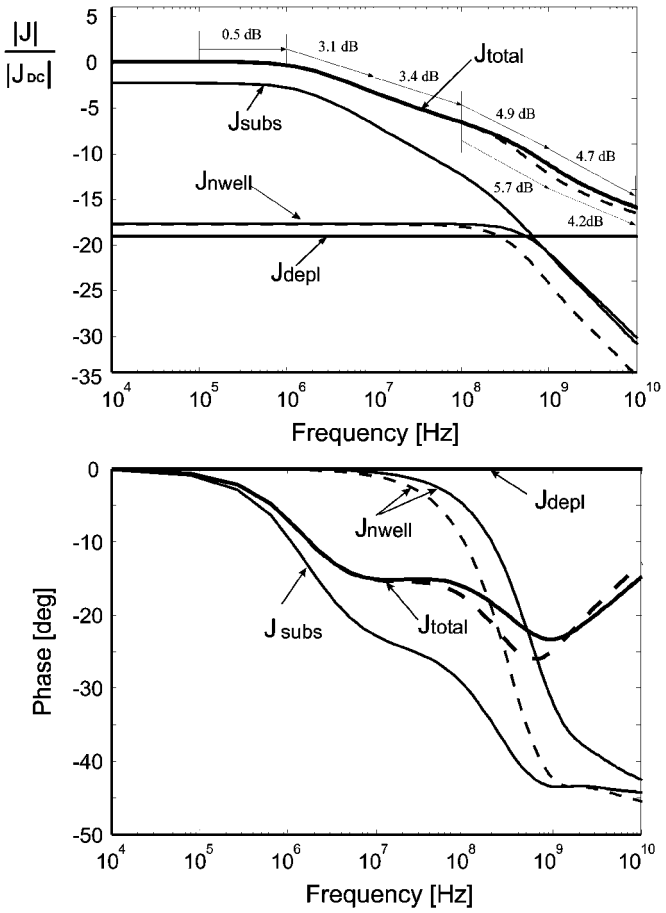

Fig. 3. Calculated amplitude response of n-well/p-substrate photodiode with a low-ohmic substrate: 2 μm (solid lines) and 10-μ n-well width (dashed lines) for $\lambda = 850$ nm.

For the calculations, only process data were used; no calibrations on measurements were done.

2) N-well/P+ Junction: A different type of junction is the n-well/p+ junction. This junction resembles a scaled-down (and complementary) version of the n-well/p-substrate junction. The major difference with the previous type of junction is that only carriers generated near the n-well/p+ junction contribute to the photocurrent. Carriers generated near the n-well/p-substrate junction and carriers that are generated in the substrate do not contribute to the current in the n-well/p+ junction; they are collected by the n-well/p-substrate junction. Because in this way carriers that are generated deeper than about 1 μm into the silicon do not contribute to the photocurrent, both the speed of this photodiode is high and the responsivity is decreased significantly.

In a standard 0.18-μm CMOS process, the intrinsic speed of an n-well/p+ junction for $\lambda = 850$ nm is around 3 GHz. This 3 GHz is about three decades higher than that of the previously discussed junction types, while the responsivity is about 18 dB lower.

3) P-well/N+ Junction: The p-well/n+ junction is the complement of the previously discussed n-well/p+ junction. The only difference is that the diffusion constants in the two regions are different. It may be clear that this type of junction has about the same performance, advantages, and disadvantages as the n-well/p+ junction.

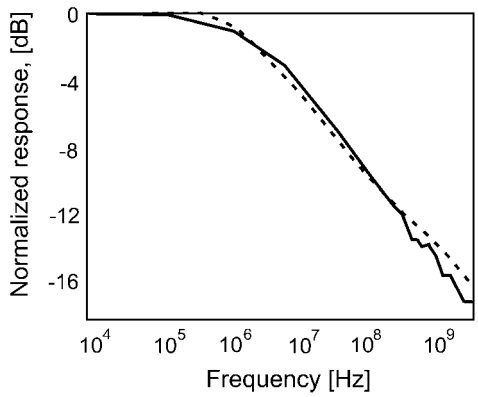

Fig. 4. Measured and calculated responses of an n-well/p-substrate photodiode with 2 μm n-well width at $\lambda = 850$ nm.

TABLE I
PERFORMANCE SUMMARY OF VARIOUS PHOTODIODES IN A STANDARD 0.18-μm CMOS TECHNOLOGY AT $\lambda = 850$ nm

type	relative DC responsivity	cut-off frequency	average slope
p+/nwell/p-sub			
low-ohmic substrate	0 dB	1.8 MHz	-3.1 dB/dec
high-ohmic substrate	3 dB	1.2 MHz	-3.9 dB/dec
nwell/p-substrate			
low-ohmic substrate			
2um wide nwell	0 dB	1 MHz	-3.9 dB/dec
10um wide nwell	0 dB	1 MHz	-4.4 dB/dec
nwell/p-substrate			
high-ohmic substrate			
2um wide nwell	3 dB	600 kHz	-4.7 dB/dec
10um wide nwell	3 dB	600 kHz	-5.3 dB/dec
p+/nwell	-18 dB	3 GHz	-7 dB/dec

4) Summary: In the previous subsection, a short discussion of photodiode structures and their performance was given for 0.18-μm CMOS at $\lambda = 850$ nm. It follows that the roll-off of the intrinsic response of photodiodes is low: between -3 and -10 dB/decade. Because of this low roll-off, the photodiodes cannot be compared based on just their -3-dB bandwidths and their relative responsivity.

For ordinary systems, the -3-dB frequency is the frequency at which the dc and ac asymptotes cross. For systems where the total response is the sum of many contributions, the -3-dB frequency is almost meaningless. In the remainder of this section, we will therefore use the cut-off frequency, which is again the frequency at which the dc and ac asymptotes of the total response cross. The performance of a number of photodiodes that can be realized in CMOS for $\lambda = 850$ nm are listed in Table I. In the table, the responsivity is normalized with respect to the maximum responsivity in a low-ohmic substrate.

At first sight, the shallow p+/n-well photodiode may appear to posses the best tradeoff between speed and responsivity: a cut-off frequency that is 3.5 decades higher comes at the cost of 18-dB responsivity. However, for nonfirst-order systems, the tradeoff is not a linear one. For comparison of the performance

TABLE II
FOM FOR THE INTRINSIC PERFORMANCE OF THE PHOTODIODES IN TABLE I FOR $f_{\mathrm{ref}} = 1.5$ GHz

type	relative FOM_i
p+/nwell/p-sub	
low-ohmic substrate	1
high-ohmic substrate	0.997
nwell/p-substrate	
low-ohmic substrate	
2um wide nwell	0.73
10um wide nwell	0.6
nwell/p-substrate	
high-ohmic substrate	
2um wide nwell	0.68
10um wide nwell	0.54
p+/nwell	0.49

of the intrinsic performance of photodiodes, a new figure of merit (FOM_i) is introduced. In analogy to the gain–bandwidth product in amplifiers, a good FOM_i is the responsitivy at a certain reference frequency $\mathrm{resp}(f_{\mathrm{ref}})$. Assume that this reference frequency is much higher than the cut-off frequency $f_{\mathrm{cut-off}}$

$$\mathrm{FOM}_i = \mathrm{resp}(f_{\mathrm{ref}}) = \mathrm{resp}(0) \cdot \left(\frac{f_{\mathrm{cut-off}}}{f_{\mathrm{ref}}} \right)^s \qquad (4)$$

where the factor s is the ratio between roll-off of the intrinsic photodiode response and first-order roll-off (-20 dB/decade). Note that the roll-off of the diode is the average roll-off in the frequency band starting at the cut-off frequency up to the highest frequency of interest

$$s = \frac{\text{roll off}}{-20\,\mathrm{dB/decade}}. \qquad (5)$$

For first-order systems, this FOM equals the ratio between the gain–bandwidth product and the reference frequency. The resulting FOMs for the photodiodes in Table I are shown in Table II, assuming a reference frequency of 1.5 GHz which corresponds to 3-Gb/s data rate.

It follows that the photodiodes on low-ohmic substrates have the highest performance. Furthermore, narrow finger structures perform a little better than wide finger structures do, although the impact of layout optimization is not significant at $\lambda = 850$ nm. The best structure is clearly the complex p+/n-well/p-substrate photodiode; the second best is the simpler n-well/p-substrate one.

B. Extrinsic Photodiode Bandwidth

The in-circuit bandwidth of a photodiode is determined by both the intrinsic bandwidth that is related to mainly diffusion processes inside the photodiode and the extrinsic bandwidth that is determined by the impedance of the photodiode in combination with the input impedance of the preamplifier. In this section, it is assumed that the area of the photodiode roughly equals the cross section of a multimode fiber: $50 \times 50\ \mu\mathrm{m}^2$.

TABLE III
PARASITIC CAPACITANCE AND EXTRINSIC FOMS FOR DIFFERENT PHOTODIODE STRUCTURES AND GEOMETRIES. THE TOTAL PHOTODIODE AREA IS $50 \times 50\ \mu\mathrm{m}^2$

type	capacitance	$FOM_{ex}(3GHz)$
p+/nwell/p-sub		
low-ohmic substrate		
2um wide nwell	3.6 pF	15 Ω
10um wide nwell	2.2 pF	24 Ω
nwell/p-substrate		
low-ohmic substrate		
2um wide nwell	1.6 pF	33 Ω
10um wide nwell	0.6 pF	88 Ω
p+/nwell	2 pF	26 Ω

For integrated photodiodes, parasitics like pad capacitances and series inductance are not present, while, e.g., series resistance and the capacitance of interconnect is negligibly small. The impedance of the photodiode is hence dominated by junction capacitance and is

$$C_{\mathrm{total}} = A \cdot C_{\mathrm{specific,bottom}} + L_{\mathrm{sides}} \cdot x_{\mathrm{junction}} \cdot C_{\mathrm{specific,side}}$$

where A denotes the total bottom area of the junction, L_{sides} is the total perimeter, x_{junction} is the junction depth, and C_{specific} is the specific junction capacitance. This specific capacitance of a junction is a function of the dope level: more heavily doped junctions yield a higher C_{specific}. Typically, photodiodes consisting of a few large junctions have a lower total capacitance than photodiodes built up of many smaller junctions, because of the significantly lower side-wall contributions.

Table III shows the parasitic capacitance calculated for the photodiodes in low-ohmic substrates in Table II. Whereas the finger-widths have only a small impact on the intrinsic behavior of the photodiodes (see Table II), there is a significant impact on their parasitic capacitance values.

From a circuit point of view, a reasonable FOM for the extrinsic behavior of photodiodes $\mathrm{FOM}_{\mathrm{ex}}$ is the required input resistance to reach a certain bandwidth, assuming an ideal preamplifier with a purely capacitive input impedance. This FOM is proportional to the ease of implementing a suitable preamplifier input stage for the photodiode. The $\mathrm{FOM}_{\mathrm{ex}}$ calculated for an electrical bandwidth of 3 GHz are also shown in Table III.

C. Total Photodiode Performance

Sections II-A and II-B present analyses in the intrinsic and extrinsic performance of photodiodes. Of these two performance indicators, the extrinsic performance results in demands on input impedance of the preamplifier circuitry in order to reach a certain data rate.

Combining the FOMs for the intrinsic and extrinsic performance of CMOS photodiodes, shown in Tables II and III, it follows that there is no such thing as the "best photodiode" based on only photodiode properties. The selection of the best photodiode for our application hence includes system and circuit aspects; the selection is made in Section III.

III. Optical Detector: System-Level Design

It follows from the analyses in the previous section and from measurements that the roll-off in the photodiode's *intrinsic* response is low. For nowadays CMOS technology and for 850-nm light, the roll-off for good photodiodes is between -3 and -5 dB/decade in the frequency range from a few megahertz up to a few gigahertz. This frequency range is typically upper-limited by the electrical (in-circuit) bandwidth of the photodiode.

For frequencies higher than the electrical bandwidth, the roll-off is dominated by the electrical in-circuit behavior of the photodiode and consequently the roll-off then is at least -20 dB/decade. The electrical bandwidth of the photodiode is determined by (mainly) the photodiode's capacitance and the preamplifier's input impedance. The electrical bandwidth can usually be increased sufficiently at the cost of power consumption in the preamplifier.

A. Compensating the Intrinsic Bandwidth

The low roll-off region in the response, extending over several decades, is intrinsic to photodiodes in standard CMOS technology at $\lambda = 850$ nm and severely limits the maximum bit rate in optical receivers [12], [13]. Increasing the maximum bit rate is usually done by elimination of the bulk current component from the overall photodiode response. This increases the bit rates up to 700 Mb/s at the cost of nonstandard CMOS processes and responsivity (e.g., [7], [9], [8]) or at the cost of only responsivity [12], [13]. Note that the exchange of bandwidth and responsivity is also present when going from a p+/n-well/p-substrate photodiode to a p+/n-well photodiode. As shown in Table II, this yields a bad intrinsic photodiode performance and a suboptimal extrinsic performance.

The low roll-off property of the photodiode's response enables the efficient use of a relatively simple analog equalizer to compensate for it.[4] In this way, standard CMOS photodiodes can be used for high bit rates without sacrificing responsivity. The required equalization characteristic is the complement of the photodiode response: it has a low roll-up characteristic. Fig. 5 shows a way to mimic a low roll-up characteristic: summation of the outputs of four first-order high-pass sections and the original input signal. Robustness issues of this equalizer are discussed in Section V.

The block diagram of the optical detector circuit, including photodiode, TIA, and equalizer, is shown in Fig. 6. For the designed optical detector system, the target bit rate was 3 Gb/s. Accepting a small amount of intersymbol interference (ISI), the equalization of the intrinsic photodiode bandwidth must be at least up to 1 GHz.[5] The input impedance of the preamplifier is designed to give an electrical bandwidth significantly higher than this equalization range.

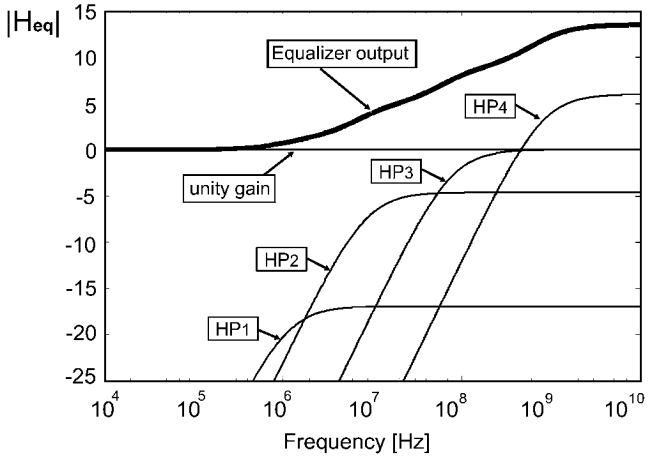

Fig. 5. Analog equalizer transfer characteristics: the summed response of a unity gain path and four high-pass sections.

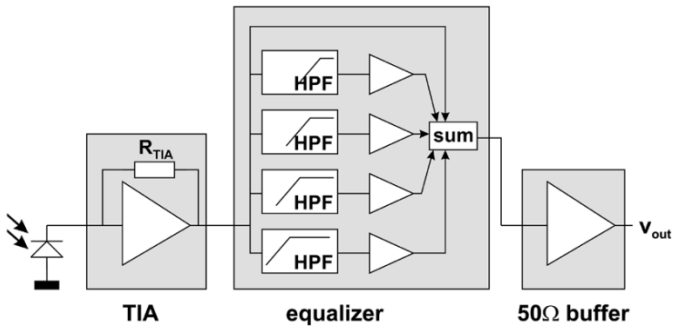

Fig. 6. Block diagram of the optical detector: an integrated photodiode and preamplifier including a TIA input stage and an analog equalizer. The 50-Ω buffer is included for measurements.

B. Impact of the Extrinsic Bandwidth Requirements

The intrinsic low roll-off of photodiodes can efficiently be compensated for using an analog equalizer. Then, the remaining bottle necks for high-speed operation are in the electrical bandwidth limitations and in the reachable BER; the first topic is discussed in this section while BER issues are addressed in Section III-C.

The electrical bandwidth of a photodiode-TIA system is usually determined by the pole at the input of the TIA, formed by the total input capacitance seen at the input node and by the input resistance. Typically the demand on input resistance translates directly in a lower bound on the bias current in the input stage. For the input stage used in our design, the input resistance equals $1/g_m$ of the input transistor. Assuming a certain effective gate–source overdrive voltage $(V_{\rm GS} - V_T)$, the input resistance can be decreased by simultaneously increasing the transistor width W and its bias current I_D

$$r_{\rm in} = \frac{1}{g_m} \propto \frac{1}{I_D} \propto \frac{1}{W} \quad \text{at constant } (V_{\rm GS} - V_T).$$

If the diode capacitance is dominant in the total capacitance at the input of the TIA, the capacitance at the input node is $C_{\rm in} \approx C_{\rm diode}$ and then $r_{\rm in} \approx {\rm FOM}_{\rm ex}$. As a good approximation then

[4]Equalization in itself is not a new technique, see, e.g., [22] for an overview of techniques and applications. However, usually the technique is applied to equalize for the channel response, which typically exhibits a relatively steep roll-off and which requires adaptive equalization. In this paper, equalization is introduced to compensate for the response of the integrated detection device (the photodiode) while the low roll-off property of the photodiode is exploited maximally.

[5]A higher bandwidth results in lower ISI and hence better sensitivity of lower BER, but comes at the cost of a higher power consumption. The 1-GHz bandwidth is sufficient to reach sufficiently low BER figures at near minimum power consumption at 3 Gb/s.

the bias current of the input stage I_D is inversely proportional to the extrinsic $\mathrm{FOM_{ex}}$ shown in Table III. Note that for real TIA's $C_{\mathrm{in}} > C_{\mathrm{diode}}$ resulting in requiring $r_{\mathrm{in}} < \mathrm{FOM_{ex}}$.

C. Impact of Noise: Getting a High BER

For data channels, not only is the bare data rate important, but good data quality is also essential. As discussed in detail in, e.g., [12], the BER in channels with a signal-to-noise ratio (SNR) and having ISI is

$$\mathrm{BER} = \frac{1}{2}\mathrm{erfc}\left(\frac{S}{\sqrt{\mathrm{ISI}_v^2 + N^2}}\right) \tag{6}$$

where ISI_v is the statistical variation of the ISI, and S and N are the signal and noise values, respectively. Sufficiently low ISI values are insured by proper equalization of the channel, i.e., using equalization of the intrinsic photodiode response. It follows that, for a 3-Gb/s data rate with BER $= 10^{-12}$, the required SNR is about 8.

Typically, the noise is mainly due to the input stage of the preamplifier and to the (shot) noise generated by the photodiode. This photodiode (shot) noise current is the combined effect of the dark current noise and the quantum noise, due to the generated photocurrent. The noise generated by the input stage is a function of its circuit architecture and its bias conditions. With the same assumption as in Section III-B, certain data rate and BER requirements yield (for a certain photodiode and optical power) a lower bound on the bias current I_D of the input stage.

D. Photodiode Selection

In the optical detector system, an analog equalizer will be used to compensate for the intrinsic low roll-off of photodiodes. For sufficiently high data rates, the electrical bandwidth must be sufficiently high. The intrinsic FOM_i and the extrinsic $\mathrm{FOM_{ex}}$ indicate their (relative) easy of application; they are summarized in Table IV.

For high data rates at low BER, both the demands on low TIA input resistance r_{in} and on sufficient SNR place lower bounds on the input stage's bias current. The third column in Table IV shows which of these two are dominant in the required bias current for the TIA circuit used in this study. It follows from Table IV that the power consumption for the TIA input stage for both p+/n-well/p-subphotodiodes is larger than that for the n-well/p-substrate diodes, due to the required lower input resistances. Furthermore, the power consumption for the two n-well/p-substrate photodiodes is the same because there it is determined by the SNR requirements. Of these two photodiodes, the narrow-finger-width photodiodes have better intrinsic behavior. This narrow-finger n-well/p-substrate photodiode is therefore used in the optical detector system: it is the best performing photodiode in the power budget determined by the BER.

IV. Preamplifier: Circuit-Level Design

To get a sufficiently low input impedance and low noise figure, the input stage of the preamplifier is a standard TIA circuit, as shown in Fig. 7. The transresistance of this amplifier is about 850 Ω, while for sufficiently low noise operation the bias current of $M1$ is 7 mA. The input resistance of the TIA for these bias conditions is about 22 Ω.[6]

The equalizer is designed to have a response complementary to that of the photodiode's intrinsic response, shown in Fig. 4. In the block diagram shown in Fig. 6, the low roll-up is realized by summation of the original signal to four high-passed versions. The number of high-pass sections is based on the required equalization accuracy: less sections give an equalization that is too coarse while four sections are sufficient. More sections could be used, resulting in a slight increase in performance at the cost of power and area consumption. Many more sections are useless due to component spread. The total equalizer can be implemented in one equalization stage; however, for reasons of power and area efficiency, the circuit implements the equalizer in two stages: a gain section with frequency-dependent source degeneration implementing three out of the four high-pass sections and one high-pass section merged into a preceding gain stage. This latter stage is an inductive peaking section [25]. The total circuit is shown in Fig. 7.

TABLE IV
FOMs and the Dominant Effect for the Input Stage's Bias Current for Different Photodiode Structures and Geometries; The Total Photodiode Area Is $50 \times 50\ \mu\mathrm{m}^2$

type	FOM_i	FOM_{ex}	dominant for I_D
p+/nwell/p-sub			
low-ohmic substrate			
2um wide nwell	1	15 Ω	r_{in}
10um wide nwell	1	24 Ω	r_{in}
nwell/p-substrate			
low-ohmic substrate			
2um wide nwell	0.73	33 Ω	SNR
10um wide nwell	0.6	88 Ω	SNR

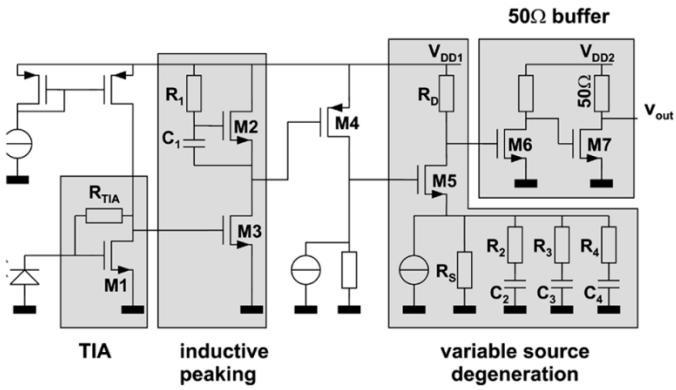

Fig. 7. Circuit topology of the preamplifier including an analog equalizer.

[6]Note that an *ideal* TIA with 22-Ω input resistance can be used in combination with the wide p+/n-well/p-substrate photodiode. A real circuit implementation however increases the capacitance at the input node, which results in requiring a lower r_{in}; for our implementation, the total input capacitance is about 0.5 pF.

The frequency responses of the inductive peaking section $H_{\rm ip}(s)$ and of the source degeneration section $H_{\rm sd}(s)$ are (simplified)

$$\begin{aligned} H_{\rm ip}(s) &\approx -\frac{gm_{m3}}{gm_{m2}} \cdot \frac{1+s\cdot R_1C_1}{1+s\cdot C_1/gm_{m2}} \\ H_{\rm sd}(s) &\approx -\frac{gm_{m5}R_D}{1+gm_{m5}Z_s} \\ &\approx -\frac{R_D}{Z_s} \\ &= -\frac{R_D}{R_s} - \frac{R_D}{1+sR_2C_2} - \frac{R_D}{1+sR_3C_3} - \frac{R_D}{1+sR_4C_4}. \end{aligned}$$

The overall response of the equalizer stages, $H_{\rm ip}(s)\cdot H_{\rm sd}(s)$, is designed to mimic the required low roll-up characteristic.

A 50 Ω buffer is added to the circuit to drive the measurement setup. This buffer consists of two cascaded common-source stages; the last one having a 50-Ω drain resistor.

V. Robustness

Robustness is a major issue for any equalizer: a high sensitivity, e.g., for spread in the various components in the equalizer or for the wavelength of the light would require adaptive equalization for robust operation.[7] Typically adaptive equalization increases the complexity considerably. It will be derived in this section that the proposed equalizer is inherently robust against spread because of the low roll-up property of the equalizer. Measurements on robustness to confirm the findings in this section are presented in Section VII-C. Note that a side effect of the feedforward circuit implementation of the equalizer and the absence of the need for adaptation is that the system is unconditionally stable.

In ICs, typically two types of spread occur. Firstly, there is intradie spread or component mismatch that results in relatively small *relative* spread between components on the same die. This relative spread is typically lower than 1% and can be neglected with respect to the second type of spread. This second type of spread is a interbatch spread that results in a significant spread in component values that strongly correlate per die. This interbatch spread can amount to a 20% shift in the *RC* products in our equalizer, whereby all *RC* products shift in the same direction. Fig. 8 shows the impact of this spread on the equalizer characteristic.

The gain error due to a correlated shift of the whole equalization curve can easily be estimated by combining the shift and the slope of the equalization curve. A frequency shift by a factor $(1+\Delta)$ of the whole curve yields a gain error equal to

$$\frac{\Delta\text{gain}}{\text{gain}} \approx (1+\Delta)^{-s} - 1$$

or, expressing the frequency change and gain change in decibels,

$$\Delta\text{gain[dB]} \approx -\Delta\text{[dB]}\cdot s. \tag{7}$$

[7]We do not address robustness issues of the equalizer for *high* input amplitudes: the presented work aims at high bit rates at small input signals. At too high input signals, the equalizer may saturate in which case the equalizer effectively does not work anymore; then the performance of the optical receiver decreases considerably. This can be solved straightforwardly using a variable gain stage or a switchable gain stage as done in many receivers.

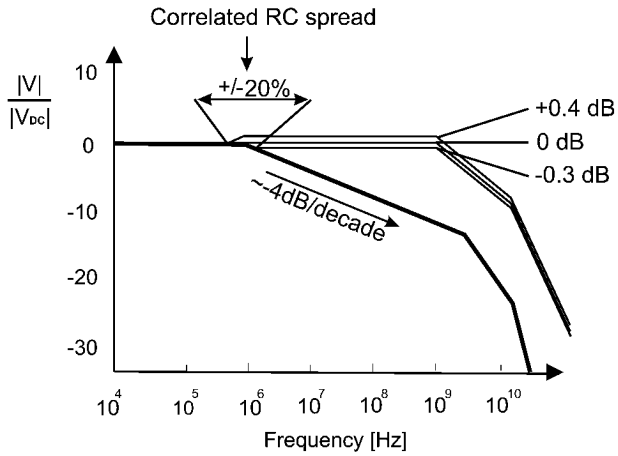

Fig. 8. Asymptotic approximation of ±20% shift in the *RC* products in the equalizer on the total system response. The lower curve is the nonequalized response, and the higher curves are the nominal equalized response and the +20% and −20% responses.

As an example, −20% and 20% spread for the total equalization curve yields, at an intrinsic roll-off of −4 dB/decade, a gain spread of only +0.4 dB, respectively −0.3 dB in the overall response. Furthermore, it is important to note that the error in the total frequency response of the system is in a small frequency band located around the cut-off frequency of the photodiode. An error in the total equalization characteristic results in ISI only if input frequencies are present in this frequency range. In our system, the gain errors are around 1 MHz, while the bit rate is around 3 Gb/s: the low gain error due to spread results in only a very small increase in the ISI, which can be compensated by a very small increase in optical input power. The main effect of component spread, and the resulting shift in the equalization characteristic, is a changed gain.

These findings are illustrated by the change in the time response on an (optical) bit (with a square-wave shape and 0.5-ns pulse duration), shown in Fig. 9. The upper three curves in Fig. 9 show the output signal of the optical receiver including equalization, with −20%, 0%, and +20% spread in the filter poles with respect to our nominal design. It follows that the effect of this spread is relatively small. As a comparison, the lower curve corresponds to the same system, now with a bypassed equalizer.

The impact of the spread on the performance of the optical detector system is more easily seen in Fig. 10. The curve in that figure shows the simulated eye amplitude at the output of the detector, as a function of spread in the equalizer's poles. Our nominal design is indicated by the vertical dotted line; note that this design is nonoptimum which is due to a design error. The dots in the figure are measurement data and are discussed in Section VII-C.

In the proposed optical detector, the *intrinsic* response of the photodiode is equalized. This intrinsic response is due to the combined effects of many diffusion currents; this response hence depends on the diffusion constants for carriers. These diffusion constants, in turn, depend mainly on doping levels and on the temperature. The dope-level dependency manifests itself in different temperature dependencies for the various parts in the photodiode. For the dominant current contribution, the substrate current, the temperature dependency follows

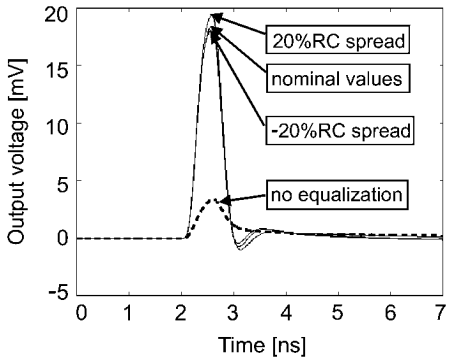

Fig. 9. Simulated symbol response of the optical detector: for the nominal case, with and without spread, and for the nonequalized case.

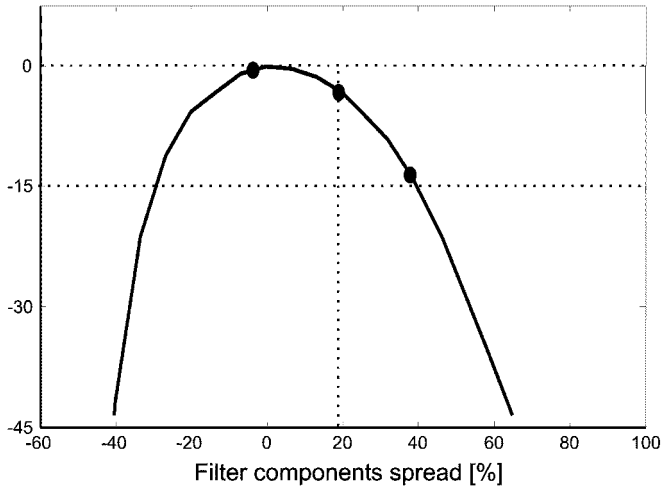

Fig. 10. Simulated relative eye-amplitude change at the equalizer's output as a function of the spread in *RC* and some measurement results (dots).

directly from the Einstein relation and well-known expressions for carrier mobility, e.g., in [23] as

$$\begin{array}{llll} \mu_n & \propto T^{-2.3\pm0.1} & \mu_p \propto T^{-2.2\pm0.1} \\ D_n & \propto T^{-1.3\pm0.1} & D_p \propto T^{-1.2\pm0.1}. \end{array}$$

It follows from these relations that, for a temperature range from, e.g., 230 K to 370 K, the diffusion constant are changed by 38% and −30%, respectively, with respect to that at room temperature. With the earlier findings for spread in equalizer parameters this yields a (deterministic) gain error of up to ±0.6 dB.

The system as presented in this paper is designed to work on one specific wavelength of the incident light. In this paper, the expected spread on the wavelength is assumed to be negligibly small; however, the impact of different wavelengths on the system's performance can easily be estimated. The major effect of different wavelengths on the physical behavior of the photodiode is that the penetration depth of the light is a strong function of the wavelength (see, e.g., [24]). For example, at 850-nm light, the depth at which 50% of the light is absorbed is about 9 μm, while it is 3.5 μm at $\lambda = 700$ nm, 1.8 μm at $\lambda = 600$ nm, and down to only 0.7 μm at $\lambda = 500$ nm. Therefore, at shorter wavelengths, the light is absorbed in faster parts of the photodiode: lower wavelengths intrinsically imply a much faster response of CMOS photodiodes [19], [20].

The impact of *spread* in wavelengths for a fixed equalizer is similar to that of equalizer spread using a fixed wavelength. A limited spread in the wavelength therefore mainly yields a spread in gain. For *large* spread, there might be an additional significant increase in ISI which can easily be compensated for by switching on or off of high-pass sections in the equalizer.

VI. Impact of Technology

In this paper, the main focus is on optical detectors for 850-nm light in CMOS. Our demonstrator circuit was realized in a standard 0.18-μm CMOS process, without any process options and without using or generating high voltages to speed up the photodiode's response. The effect of going to newer CMOS technologies can easily be estimated using, e.g., Fig. 2: in newer (bulk-CMOS) technologies, the device dimensions shrink. At a constant wavelength of the incident light, this implies that relatively much less photocurrent is generated in the fast parts of photodiodes and that at the same time somewhat more photocurrent is generated in the slow substrate. For high-ohmic substrates, this would result in somewhat slower photodiodes that still can be used at high bit rates using an appropriate equalizer. For low-ohmic substrates (and assuming that the epilayer thickness also shrinks), the photodiode will be faster but will also have a somewhat lower responsivity. Also, in this case, the photodiode can easily operate at high bit rates if a suitable equalizer is used. The impact of different wavelengths was discussed in Section V.

VII. Experimental Results

Fig. 11 shows the chip microphotograph of the integrated optical detector, including the n-well/p-substrate photodiode and the preamplifier with equalizer. As discussed in Section III-D, a minimal n-well-distance finger photodiode with 2-μm finger size is used as a photodetector. The size of the photodiode is 50×50 μm^2, yielding a junction capacitance equal to 1.6 pF. An 850-nm VCSEL and a multimode fiber are used as a light source for measuring the system performance. The power-supply voltage was 1.8 V. The complete optical detector system consumes approximately 34 mW +16 mW for the 50-Ω output buffer for evaluation.

A. Measurement of the System Without Equalizer

Fig. 12(a) shows an eye diagram for the optical detector, without equalizer, at 50 Mb/s, and with a peak–peak light input power of 25 μW (−19 dBm). For this eye diagram, the BER $= 10^{-7}$, measured using a bitstream of length $2^{31} - 1$ on an Anritsu MP1632C analyzer. For the system without equalizer, the calculated maximal speed for BER $< 10^{-11}$ is 10 Mb/s; no measurements could be done for verification of this figure because this bit rate is too low for the used data analyzer.

B. Measurement on the System With Equalizer

Fig. 12(b) shows the measured eye diagram at 3 Gb/s for the optical detector system including the analog equalizer. Also, for this measurement, the peak–peak light input power is 25 μW. For the eye diagram in Fig. 12(b) the BER $= 10^{-11}$.

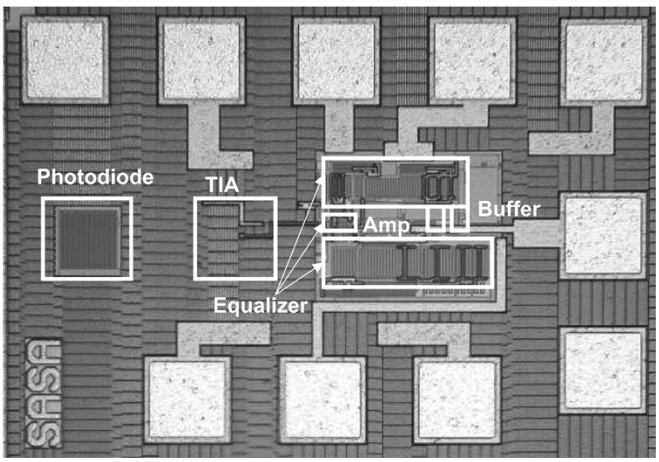

Fig. 11. Chip microphotograph of the integrated n-well/p-substrate photodiode and preamplifier with an analog equalizer in standard CMOS.

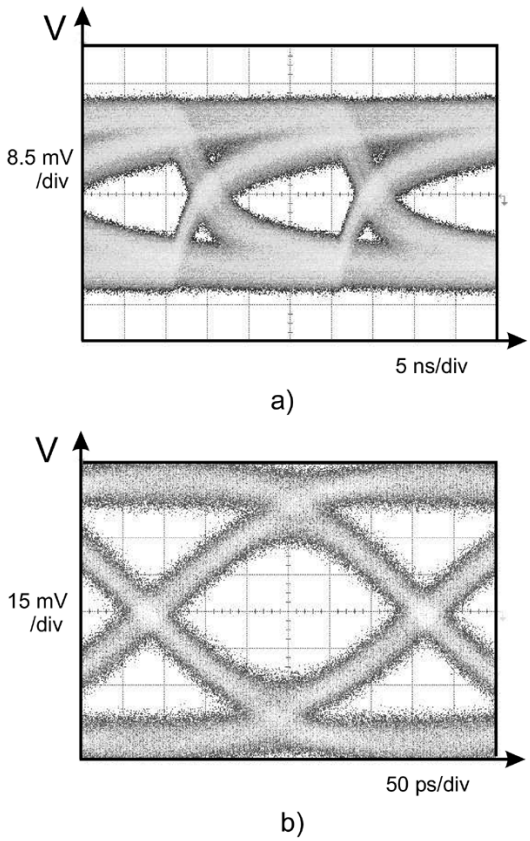

Fig. 12. Eye diagram of the n-well/p-substrate CMOS photodiodes for -19-dBm optical power (a) without equalizer at 50 Mb/s, BER $= 10^{-7}$, and (b) with an analog equalizer at 3 Gb/s, BER $= 10^{-11}$.

The measured BER as a function of the the average light input power, at 3 Gb/s, is represented by the solid curve in Fig. 13; the dots indicate measured values. The sensitivity at a BER of 10^{-11} is around -19 dBm; note the strong relation between BER and optical input power.

C. Robustness of the Proposed System

For verification of the spread insensitivity of the system, both spread in the photodiode and spread in the equalizer circuit are measured.

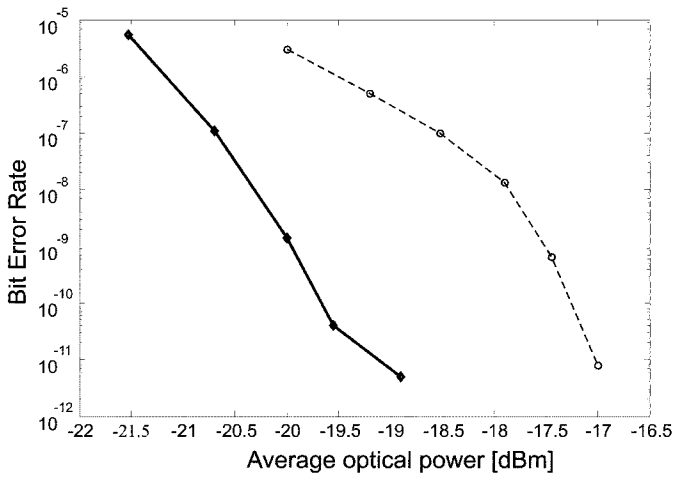

Fig. 13. BER as a function of the input optical power; the solid curve is for the system at 3 Gb/s and the dashed curve is for spread sensitivity estimations, using a p+/n-well/p-substrate diode at 2.5 Gb/s; markers are measured data.

To measure the impact of photodiode spread, the optical detector circuit was also implemented using a different photodiode, a p+/n-well/p-substrate photodiode instead of the n-well/p-substrate photodiode, with the same preamplifier and equalizer circuit. With this replacement, the equalizer parameters are not optimized for the used photodiode, yielding suboptimal performance. A measured eye diagram at 2.5 Gb/s and 40 μW peak–peak optical power is shown in Fig. 14. The dashed curve in Fig. 13 shows the measured BER as a function of the light input power at 2.5 Gb/s. It can be concluded that, even with the introduced huge spread in the intrinsic photodiode, the optical detector system can operate at 2.5 Gb/s at the expense of a relatively modest increase in input power.

To estimate the impact of spread in the equalizer parameters on the overall performance, in the layout measures were taken to enable changing the value of all *RC* filter components using focused ion beam (FIB) removal of interconnect. For the measurements, we introduced about -20% and $+20\%$ change in the equalizer characteristic with respect to our nominal design. The measured eye diagrams for these situation are shown in Fig. 15; the eye diagram amplitudes as a function of the introduced spread are represented by the dots in Fig. 10. These measurements confirm that the equalizer is inherently robust against spread; adaptive equalization is not required. As a side effect, these measurements show the nonoptimality of our design.

The previous measurement results were obtained at room temperature. The sensitivity to the temperature of the optical detector was determined using BER and eye-amplitude measurements for a number of temperatures. For a change in temperature of 25 K, the measured photosensitivity at a 3-Gb/s data rate decreases by only 0.3 dB with respect to that at room temperature. At a 75 K temperature increase, the decrease in sensitivity amounts to 1.7 dB. These results confirm that the optical detector system is fairly robust against temperature changes.

VIII. Conclusion

This paper presents an optical detector that is monolithically implemented in a standard 0.18-μm CMOS process. The pro-

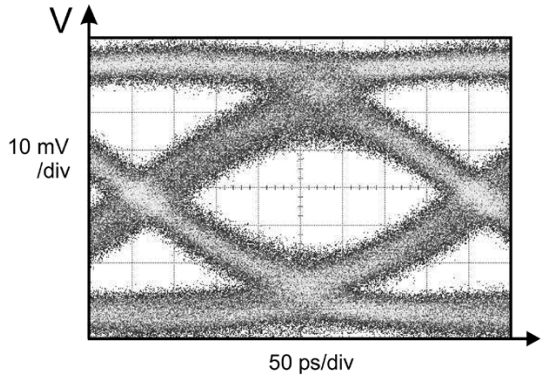

Fig. 14. Spread sensistivity estimation: 2.5 Gb/s eye diagram for the p+/n-well/p-substrate CMOS photodiodes with analog equalizer dimensioned for the n-well/p-substrate diode at -17 dBm optical power, yielding BER $= 10^{-11}$.

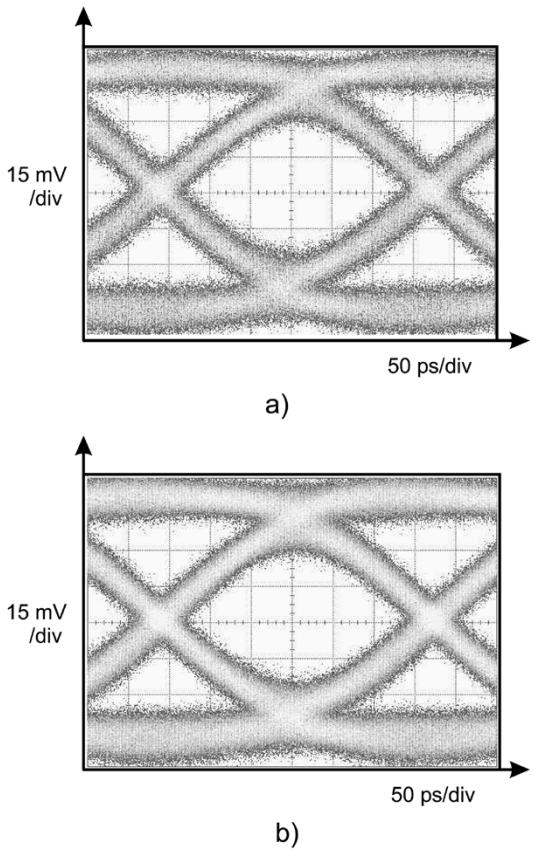

Fig. 15. Spread-sensistivity estimation: 3 Gb/s eye diagram for the optical detector with introduced $+20\%$ and -20% change in the equalizer characteristic at -19-dBm optical power, yielding BER $= 10^{-10}$.

posed system includes an inherently robust analog equalizer to correct the photodiode's intrinsic response, resulting in a 3-Gb/s data rate at -19-dBm light input power and BER $< 10^{-11}$. This data rate is over a factor of four higher than that of state-of-the-art fully integrated CMOS detectors for $\lambda = 850$ nm. Although the presented design is for $\lambda = 850$ nm, the approach is suitable for all wavelengths in the range from $\lambda =$500 nm to 850 nm. For even shorter wavelengths, equalization may not be required to obtain high data rates due to the low penetration depth at short wavelengths.

The equalization is inherently robust against spread due to the low roll-off of the photodiode intrinsic response; no adaptive equalization is required. Changes up to, e.g., 30% in temperature or in equalizer parameters result a modest performance degradation in terms of sensitivity and bit rate. Because the temperature deterministically affects the photodiode response, it could be minimized by a simple feedforward control network.

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