A 30-MHz, 90-ppm/℃ Fully-integrated Clock Reference Generator with Frequency-locked Loop

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***Abstract*— A temperature- and supply-independent clock generator has been developed using 0.35-μm CMOS technology. This generator is based on a simple frequency-locked loop technique and can be implemented monolithically without using LC resonant circuits, quartz resonators, and MEMS oscillators. A sample device that is tunable over a wide frequency range of 2-100 MHz was designed and fabricated. It showed a temperature coefficient of 90 ppm/℃, a line regulation of 4%/V, and a power dissipation of 180 μW, at a frequency of 30 MHz. The process sensitivity (σ/μ) was 2.7%. This clock generator can be used as an on-chip reference clock circuit.**

I. Introduction

Clock reference circuits are one of the important building blocks for digital and mixed-signal circuits and wireless systems in microelectronics. Quartz crystal oscillators are usually used to provide highly accurate reference clocks, but they are incompatible with standard CMOS processes and cannot be integrated monolithically with other circuit components. On-chip reference clock circuits have therefore been required for low-cost LSI applications such as implantable medical devices, sensor networks, and portable mobile devices.

Various on-chip clock circuits have been reported [1]-[4]. These circuits can generate highly stable, precise reference clocks but have room for improvement because of their large power dissipation (around 1.5-50 mW), large area (over 1 mm^2), and use of MEMS technology incompatible with standard CMOS processes. Low-power clock generators based on relaxation oscillation have been proposed [5]-[7]. The circuits are simple and have low-power configuration. However, they require temperature-insensitive reference voltages and currents to achieve reference clocks that are independent of temperature.

To solve these problems, we developed a fully-integrated clock reference circuit that can be operated with low-power dissipation for low-cost and low-power LSI applications. The circuit is based on a simple frequency-locked loop and needs no reference voltage and current but can generate a clock frequency that is insensitive to temperature and supply voltage. The frequency of the clock can be adjusted over a wide range of 2-100 MHz. The following sections describe this reference circuit.

II. Circuit configuration

Figure 1 shows a block diagram of our clock generator. The circuit generates a clock pulse using a frequency-locked loop technique. The circuit consists of a bias current circuit, a current comparator, a voltage-controlled oscillator (VCO), and a D/A converter based on frequency-to-current conversion, and these circuit elements form a feedback loop. The current comparator detects the difference between a bias current I_{BIAS} and the output current I_{OUT} of the frequency-to-current converter and generates output voltage V_{OUT} proportional to the difference. The VCO accepts the output voltage V_{OUT} and produces oscillation pulses with a frequency f_{OUT} dependent on V_{OUT}. The frequency-to-current converter accepts the oscillation pulses and generates output current I_{OUT} proportional to f_{OUT}. Then the current comparator again compares currents I_{BIAS} and I_{OUT} to produce a readjusted V_{OUT}. This feedback operation is repeated to make I_{OUT} equal to I_{BIAS}. The resulting clock frequency f_{OUT} is independent of temperature and power supply voltage.

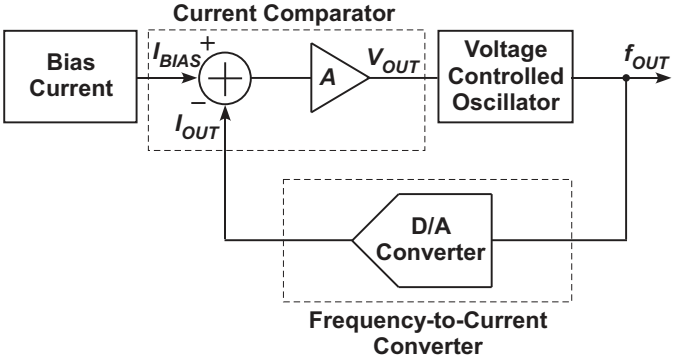

Fig. 1. Block diagram of our clock reference generator.

Figure 2 shows the entire configuration of our clock generator. The following sections describe the operation of the generator in detail.

A. Operation Principle

1) Bias Current Circuit: The bias current circuit consists of a voltage-to-current converter combined with two series-connected resistors R_P and R_N and produces bias current I_{BIAS}. The resistors consist of a low-resistive polysilicon and a high-resistive one that have opposite temperature coefficients to cancel the temperature dependence of the total resistance (see Section II-B). The voltage of one end of the resistors is fixed to a bias voltage V_{BIAS} with an operational amplifier

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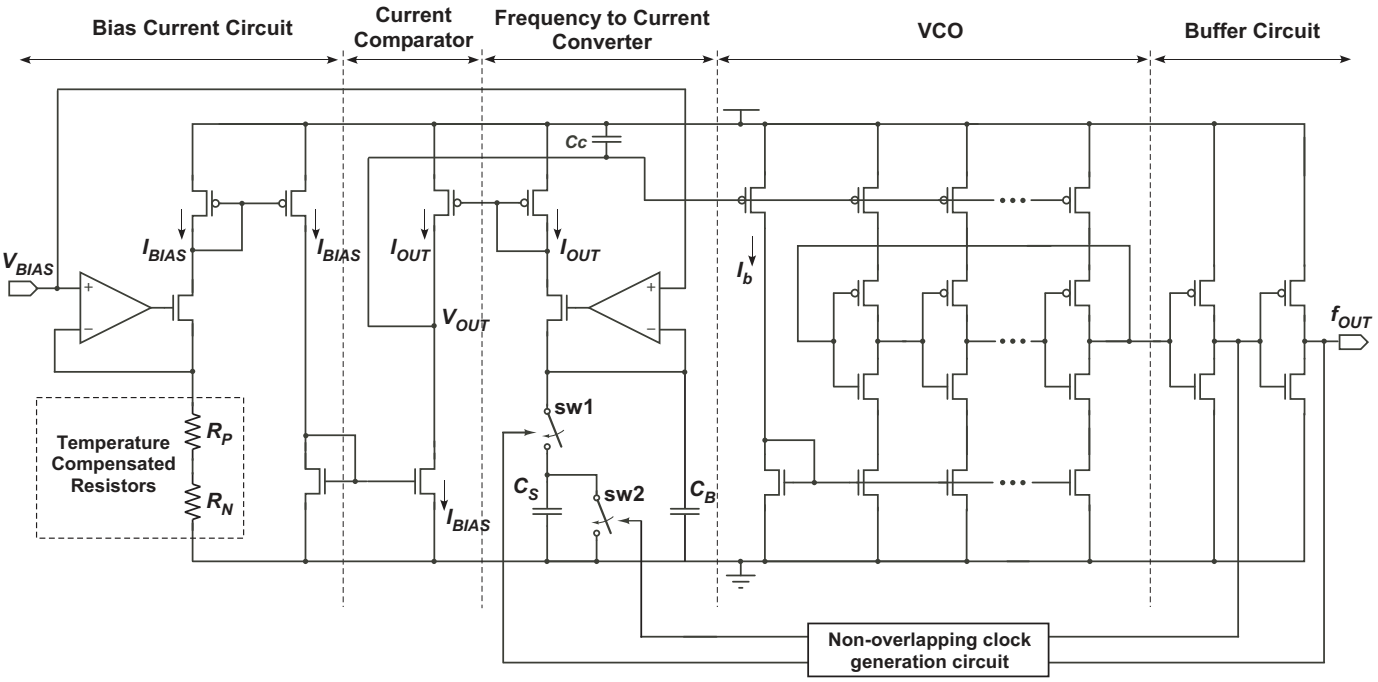

Fig. 2. Entire circuit of proposed clock reference generator.

and a MOSFET, so the variation of a bias current with supply voltage regulation can be reduced. The value of V_{BIAS} is not important for circuit operation (any value will do) as shown later. The bias current is given by

$$I_{BIAS} = \frac{V_{BIAS}}{(R_P + R_N)}. \tag{1}$$

The temperature dependence of total resistance (R_P+R_N) of resistors is canceled as described later, so we can obtain current I_{BIAS} that has little temperature dependence.

2) Current Comparator: The current comparator consists of a simple common-source circuit and is used to detect the difference between bias current I_{BIAS} and output current I_{OUT} of the frequency-to-current converter. It produces output voltage V_{OUT} proportional to the difference between the two. The capacitor C_C is for stabilizing the circuit operation.

3) Voltage Controlled Oscillator: The VCO consists of seven current-starved inverters connected in a ring. The circuit is used for producing oscillation pulses that are dependent on output voltage V_{OUT} of the current comparator. Oscillation frequency f_{OUT} depends on applied current I_b and is given by $f_{OUT} = I_b/2mAC_LV_{DD}$, where m is the number of inverters in the oscillator, C_L is the load capacitance for each inverter, and A is a delay fitting parameter [8]. Current I_b is a function of V_{OUT}, so oscillation frequency f_{OUT} depends on V_{OUT}.

4) Frequency-to-Current converter: The frequency-to-current converter is based on a voltage-to-current converter combined with a switched-capacitor resistor. The circuit is used to produce output current I_{OUT} proportional to oscillation frequency f_{OUT} of the VCO. The switched-capacitor resistor consists of capacitor C_S and two switches (sw1, sw2) driven with the oscillation pulses from the VCO, and operates as a resistor with a resistance of $(C_S \cdot f_{OUT})^{-1}$. A non-overlapping clock generator is used to prevent simultaneous shorting of the switches. Capacitor C_B removes high-frequency noise caused by switching operation. Output current I_{OUT} of the frequency-to-current converter is given by

$$I_{OUT} = f_{OUT} \cdot C_S \cdot V_{BIAS}. \tag{2}$$

This current is copied into the current comparator through a current mirror. Because of the feedback operation, the circuit settles down into a state such that I_{OUT} (Eq. (2)) is equal to I_{BIAS} (Eq. (1)). Consequently, the oscillation frequency f_{OUT} will be

$$f_{OUT} = \frac{1}{(R_P + R_N) \cdot C_S}. \tag{3}$$

The total resistance (R_P+R_N) of the resistors and the capacitor C_S have little temperature dependence, and therefore the output frequency f_{OUT} is insensitive to temperature. The output frequency is independent of bias voltage V_{BIAS} for the bias current circuit and the frequency-to-current converter.

This way, a constant-frequency clock that is independent of temperature and supply voltage can be obtained. The clock frequency can be adjusted over a wide frequency range by adjusting the total resistance of resistors R_P and R_N.

B. Temperature and Process Dependence

As resistors R_P and R_N for the bias current circuit, we used polysilicon resistors with a positive temperature coefficient and a negative one. Resistor R_P was made from polysilicon with a sheet resistance of 50Ω/ □ and a positive temperature coefficient, and resistor R_N with a sheet resistance of 1.2

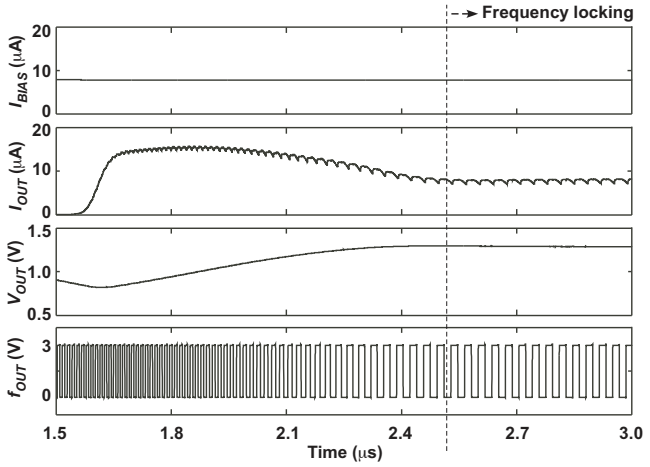

Fig. 3. Timing diagram of our circuit with supply voltage applied at time = 0.

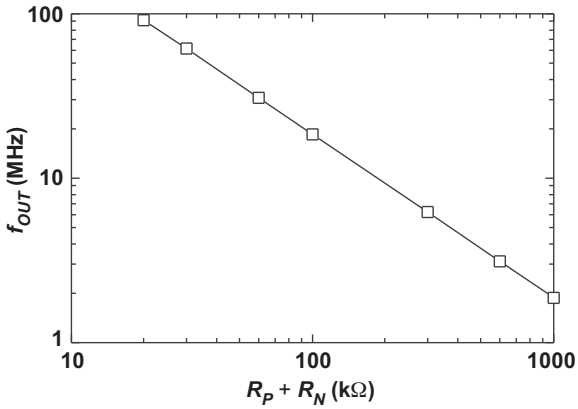

Fig. 4. Output frequency as a function of resistance $R_P + R_N$, simulated for 3-V power supply and room temperature. Tuning range of oscillation frequency was 2-100 MHz.

kΩ/ □ and a negative temperature coefficient. The temperature dependences of the resistors R_P and R_N are given by

$$R_P \approx R_{0P}(1 + \alpha_P T), \quad R_N \approx R_{0N}(1 - \alpha_N T), \quad (4)$$

where R_{0P} and R_{0N} are the 0-K resistances of resistors R_P and R_N, α_P and α_N are the temperature coefficients of the resistors, and T is the absolute temperature. Using Eqs. (3) and (4), we can express the temperature coefficient of the output frequency as

$$\frac{1}{f_{OUT}} \frac{df_{OUT}}{dT} = -\frac{R_{0P}\alpha_P - R_{0N}\alpha_N}{R_{0P} + R_{0N} + (R_{0P}\alpha_P - R_{0N}\alpha_N)T}. \quad (5)$$

Therefore, setting appropriate values of R_{0P} and R_{0N} can cancel the temperature dependence of the output frequency.

We next discuss the effect of process variation on the output frequency. The process dependence of the output frequency f_{OUT} can be given by

$$\frac{\Delta f_{OUT}}{f_{OUT}} = -\frac{\Delta(R_P + R_N)}{(R_P + R_N)} - \frac{\Delta C_S}{C_S}. \quad (6)$$

The output frequency depends on the variations of the resistances and the capacitance. However, because the temperature dependence of the output frequency can be canceled as described above, the one-point calibration such as a programmable resistor technique will enable us to compensate for process variation.

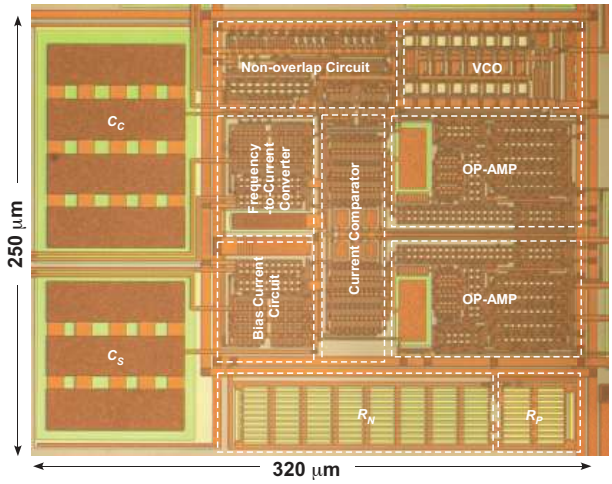

Fig. 5. Micrograph of prototype chip. Area is 0.08 mm^2.

III. Simulation Results

We confirmed the operation of the circuit by means of SPICE simulation with a set of 0.35-μm standard CMOS parameters and a supply voltage from 1.8-3 V. Bias voltage V_{BIAS} was set to 0.5 V in this simulation (other values will do).

Figure 3 shows the timing diagram of the circuit with the supply voltage applied at time = 0. The simulation results show that the current comparator produces output voltage V_{OUT} such that I_{OUT} is equal to I_{BIAS}. Consequently, the oscillation frequency f_{OUT} is locked by the feedback operation. The settling time for locking operation was about 2.5 μs. Figure 4 shows the oscillation frequency as a function of the total resistance of the resistors R_P and R_N. Resistance $R_P + R_N$ was changed from 20 kΩ to 1 MΩ. The resistors were able to adjust output frequency over a wide range of 2-100 MHz at room temperature. The supply current, with a 1.8-V supply voltage, was 7.5 μA for f_{OUT} = 2 MHz and 34 μA for f_{OUT} = 10 MHz. A low-power and wide-frequency-range operation was able to be obtained.

IV. Experimental Results

We fabricated a prototype chip with a 0.35-μm, 2-poly, 4-metal standard CMOS process. Figure 5 shows a micrograph of our prototype chip with an area of 0.08 mm^2. In this sample chip, the resistance value of resistors R_P and R_N were set to 20 kΩ and 40 kΩ. The measurement results were as described below.

Figure 6 shows the measured output frequency as a function of temperature, with supply voltage V_{DD} as a parameter. The average output frequency was 29.4 MHz at a 3-V supply voltage. The temperature variation was 310 kHz in a temperature range from –20 to 100℃. The temperature coefficient was 90

TABLE I

COMPARISON OF REPORTED CMOS CLOCK REFERENCE CIRCUITS

	This work	[1]	[2]	[3]
Process	0.35-μm, CMOS	0.25-μm, CMOS	65-nm, CMOS	0.25-μm, CMOS
Temperature range	–20 - 100℃	0 - 70℃	0 - 120℃	–40 - 125℃
V_{DD}	1.8 - 3 V	3.3 V	1.2 V	2.4 - 2.75 V
f_{OUT}	30 MHz 2 MHz - 100 MHz (freq. range)	0.5 - 480 MHz	6 MHz	7 MHz
Power	180 μW (f=30 MHz) 60 μW (f=10 MHz)	49.5 mW (f=24 MHz)	66 μW	1.5 mW
Temperature Coefficient	90 ppm/℃	N.A.	86 ppm/℃	95 ppm/℃
Temperature variation	–0.7 - 0.5%	–30 - 90 ppm	±0.8%	±0.84%
Line regulation	4%/V	N.A.	N.A.	1.8%/V
Phase noise (1 kHz offset)	–32 dBc/Hz	–65 dBc/Hz	N.A.	N.A.
(1 MHz offset)	–96 dBc/Hz	–140 dBc/Hz	N.A.	N.A.
Process sensitivity	2.7% (w/o calibration)	N.A.	0.8% (w/o calibration)	0.13% (w/ calibration)
(σ/μ)	20 samples (same wafer)		7 samples	94 samples
Chip area	0.08 mm^2	2.25 mm^2	0.03 mm^2	1.6 mm^2

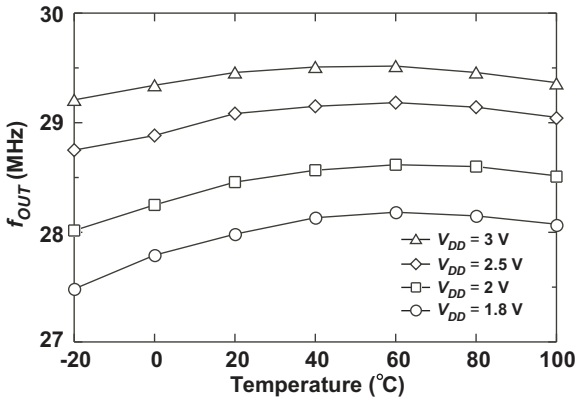

Fig. 6. Measured output frequency f_{OUT} as a function of temperature with different power supply. Temperature coefficient was 90 ppm/℃ at a 3-V supply voltage.

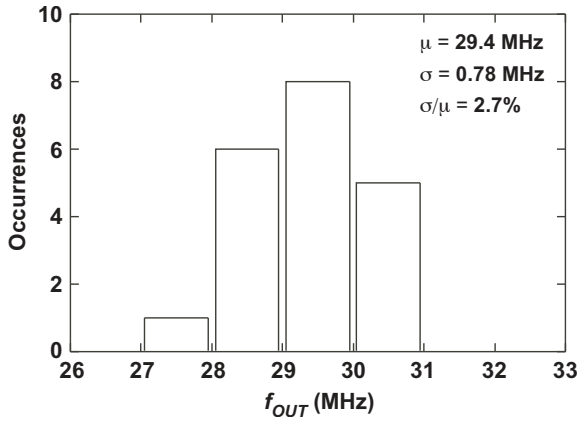

Fig. 7. Distribution of output frequency for 20 chips on the same wafer, measured at room temperature. Process sensitivity (σ/μ) was 2.7%.

ppm/℃. The circuit operated correctly for a supply voltage of 1.8-3 V, with a line regulation of 4%/V. Thus, we were able to develop a constant reference clock insensitive to temperature and supply voltage.

To examine the stability of process variation in our devices, we measured the characteristics of 20 samples, each on different chips from the same wafer. Figure 7 shows the distribution of the oscillation frequency f_{OUT} at room temperature with a 3-V power supply. The coefficient of variation (σ/μ: μ is the mean value and σ is the standard deviation of the distribution) was 2.7% without calibration and trimming techniques. This variation was smaller than expected from Monte Carlo simulation (σ/μ=12%). This is so because the sample chips were from the same wafer.

Table I summarizes the performance of our circuit in comparison with other CMOS clock reference generator [1]-[3]. The power dissipation at a 1.8-V power supply was 180 μW at 30 MHz, which is superior to other reported data. The phase noise was –32 dBc/Hz and –96 dBc/Hz at 1-kHz and 1-MHz offset frequencies. Our circuit would be useful for on-chip reference clocks of low-power and low-cost LSI applications.

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