

A 30 to 44 GHz Divide-by-2, Quadrature, Direct Injection Locked Frequency Divider for Sliding-IF 60 GHz Transceivers

Hammad M. Cheema, Reza Mahmoudi, Arthur van Roermund

Department of Electrical Engineering, Mixed-signal Microelectronics group,
Eindhoven University of Technology, 5600 MB,
Eindhoven, The Netherlands

Abstract—This paper presents a wideband 40 GHz divide-by-2 quadrature injection locked frequency divider (Q-ILFD) as an enabling component for sliding-IF 60 GHz transceivers. The design incorporates direct injection topology and input power matching using interconnect inductances to enhance injection efficiency. This results in an excellent input sensitivity and a wide locking range. Fabricated in a 65nm bulk CMOS technology, the divider operates from 30.3 to 44 GHz (37% locking range) while consuming 9mW from a 1.2V supply. The measured phase noise is -131 dBc/Hz at 1-MHz offset whereas the phase error between I-Q outputs is less than 1.44°.

Index Terms — Injection locked frequency divider, Direct injection, Frequency synthesizer, 60 GHz sliding-IF

I. INTRODUCTION

The availability of high f_T silicon IC technologies capable of operating at millimeter wave (mm-wave) frequencies and the extraordinary interest for high data rate (>1Gbps) applications has motivated research and development of 60 GHz transceivers in recent years. The 7 GHz of contiguous bandwidth available at 60 GHz, though very useful, poses circuit design challenges especially for components like VCOs, prescalers and PLLs in a direct conversion transceiver. Therefore, alternative synthesizer friendly architectures based on double-heterodyne, sliding-IF, low-IF and half-RF architectures are being investigated.

Conventionally, prescalers in frequency synthesizers were flip-flop based CML circuits [1]-[2]. However, these are difficult to design reliably for 60 GHz owing to large RC time constants of the devices which limit high frequency performance. On the other hand, injection locked frequency dividers can operate at very high frequencies but are inherently narrowband due to their LC-tanks. Fig.1 shows the system architecture of a sliding-IF 60 GHz transceiver. In this system, the RF signal is converted to baseband in two steps. The first mixing operation with the VCO transfers the RF signal from 60 GHz to 20 GHz. The second mixing using quadrature outputs from the prescaler down-converts the 20

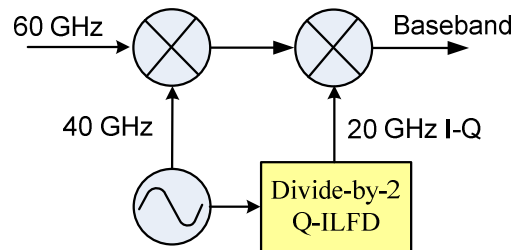


Figure 1. Quadrature ILFD usage in a sliding-IF 60 GHz receiver

GHz signal to baseband. This approach relaxes the synthesizer specifications and also avoids VCO pulling which is an issue for direct conversion architectures. In this paper, feasibility of ILFDs for 60 GHz sliding-IF transceivers is investigated by implementing a 40 GHz divide-by-2 quadrature ILFD. In addition, techniques to enhance locking range of the divider are proposed which yield good measured results.

Section II describes the circuit design of the ILFD, followed by a brief discussion, in section III, about layout and technology used. Section IV includes the measurement results and comparison with earlier published results and conclusions are drawn in section V.

II. THEORY AND CIRCUIT DESIGN

In conventional ILFD's the RF input signal is injected at the common-source node of the oscillator which is inherently running at double the fundamental frequency. However, the transistor parasitic capacitances at this node "eat-up" significant part of the high frequency injection signal. To counter this issue, shunt-peaking techniques have been utilized, albeit at the cost of extra chip area [3]. In contrast, the input signal, in this design, is directly injected across the tank which improves injection efficiency considerably, thus improving the locking range of the divider.

Majority of the published high frequency (above 30 GHz) ILFDs, either based on conventional [3] or direct-injection [4]

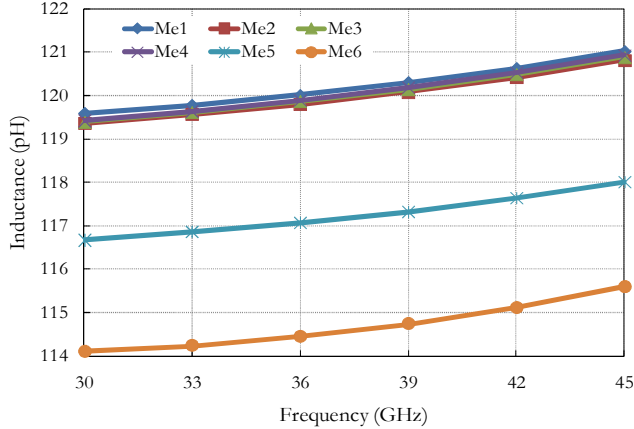


Figure 4. Inductance of a 2.5μm wide, 78μm long interconnect in different metal layers

used to determine the required inductance for maximum power matching. After optimization, EM simulations are done in ADS Momentum to determine the inductance per unit length for different metals in the technology stack as shown in Fig. 4. The metal layer Me3, which is closest to the required value is used for the interconnect layout. Due to this injection enhancement technique, input sensitivity is improved and for the same output power, the required input signal power is almost halved. This is proved by the measured low sensitivity discussed in section IV.

III. LAYOUT AND TECHNOLOGY

The layout of the divider is done carefully and compactly to reduce unnecessary parasitics. The RF signal paths between the tank and negative gm-cells are kept short and narrow lines are avoided to reduce resistive losses. The coupling transistors (M7-M10) are perfectly matched to ensure identical oscillation frequencies for both stages. In addition, ground meshing is used under the RF paths and decoupling capacitors are included for the voltage supplies. The differential input and outputs use 50Ω transmission lines (TLs) to the bondpads. These TLs are coplanar waveguide based with lateral ground plane consisting of all metal layers “sandwiched” together using large number of vias, thus providing excellent noise isolation. The width of the signal path of the TL is 5μm and spacing from the ground plane is 4.22μm.

The dividers are fabricated in TSMC bulk CMOS 65nm LP (low-power) process having six metallization layers. The process offers MIM capacitors and poly-silicon resistors. The measured f_T of NMOS and PMOS transistors is 140 GHz and 80 GHz, respectively. As shown in Fig. 5, the area of the divider is bond-pad limited and occupies 900x750μm² in which the complete core is located between the two coils and occupies 80x100 μm².

IV. MEASUREMENT RESULTS

The 40 GHz ILFD was measured on-wafer. The input 40 GHz signal from an Agilent signal generator is applied to a single-to-differential converter (180° hybrid) and then passed on the RF probe. The output differential signal is converted to

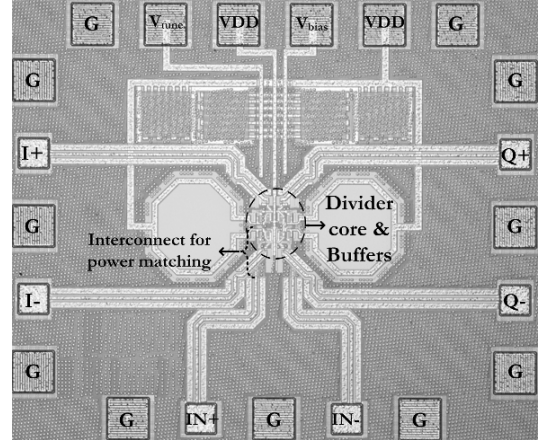


Figure 5. Die Micrograph of the 40 GHz Q-ILFD

single-ended using a similar hybrid and observed by an Agilent spectrum analyzer (E4446A). The phase noise is also measured by the spectrum analyzer.

The free-running frequency of the ILFD is first measured by switching “off” the injection signal. It starts oscillating at 1V supply whereas the maximum tuning range from 17 to 20.5 GHz is obtained with a 1.2 V supply. After fixing the tuning voltage of the varactor to a certain value, the injection signal is then switched “on” close to double the self-oscillating frequency for that particular V_{tune} . The input power is reduced to determine the minimum value for which the ILFD still locks to the input signal. Similarly, input sensitivity for different varactor tuning voltage is measured, three of which are plotted in Fig. 6. The ILFD can operate from 30.3GHz to 44 GHz (14 GHz or 37% locking range). The locking range for one tuning voltage is about 6 GHz, thus only three V_{tune} values are required to cover the complete operating range. The improved injection efficiency due to direct injection topology and input power matching technique, results in the required input power close to free-running frequency of the ILFD to be as low as -38 dBm. The simulated sensitivity curves are also plotted for reference and match closely to the measured curves. The low voltage operation of the ILFD is also verified by reducing the supply voltage. The divider can operate with a reduced supply of 1V resulting in a locking range of 8 GHz.

The phase noise of the ILFD is -131.6 dBc/Hz at 1-MHz from a 18.95 GHz output frequency (Fig. 7). The phase noise of the signal generator at double the frequency is -125 dBc/Hz which is close to the theoretical 6 dB difference due to frequency division. The phase noise variation over the complete operating range is ± 2.5 dB. The combined power consumption of the I-Q dividers is 9mW from a 1.2V supply. The output buffers used for measurement purpose consume 12mW. The locked spectrums at minimum and maximum operating frequencies are shown in Fig. 8. Due to usage of considerable number of cables (six in total), hybrids and needed connectors, considerable power loss is observed in the measured spectrum. However, after de-embedding these losses the output power of the ILFD is between -4 and -8 dBm. The I-Q phase error could not be measured reliably due to the absence of a stable trigger signal during oscilloscope measurements; however, post-layout simulations based on RC

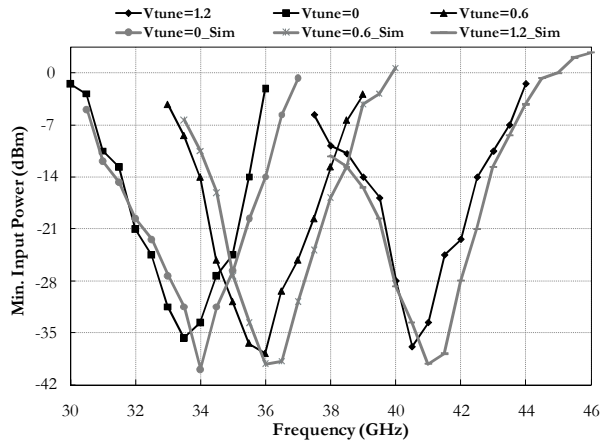


Figure 6. Input sensitivity curves of 40 GHz Q-ILFD

extraction demonstrate a phase error less than 1.44° over the complete locking range.

Table I shows a comparison of the presented frequency divider with published results. As frequency dividers with identical operating frequencies could not be found, the divide-by-2 Q-ILFD of this work is compared with ILFDs operating at higher and lower frequencies. It offers the second-highest locking range with lowest power of -2 dBm required at the locking range corners. Due to the input matching technique, the input power of -38 dBm is lower than the designs in [4-5][7]. As the only quadrature divider in the table, the power consumption is comparable to non-quadrature designs in [4]-[5]. The measured phase noise is also lower than all cited works in Table I.

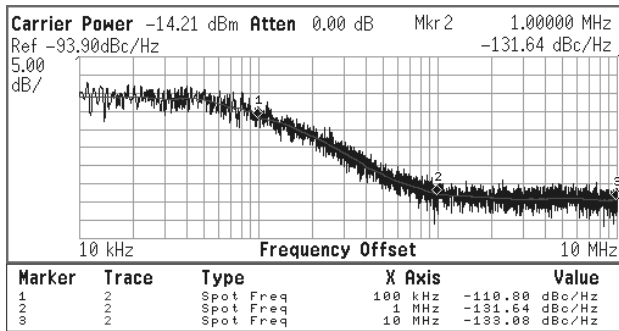


Figure 7. Phase noise for a 18.95 GHz divided output

V. CONCLUSIONS

We have presented a mm-wave quadrature injection locked frequency divider as an enabling component for a 60 GHz sliding-IF systems. The measured locking range of the ILFD is 14 GHz (37 %) while consuming 9 mW from a 1.2 V supply. The phase noise for a 18.95 GHz divided output is -131 dBc/Hz at 1 MHz offset. The minimum input injection power required is as low as -38 dBm. The low input sensitivity is achieved by employing direct injection and input power matching. The latter technique utilizes interconnect inductance to cancel the parasitic capacitance of the input injection transistor, thus no area or performance penalty is introduced.

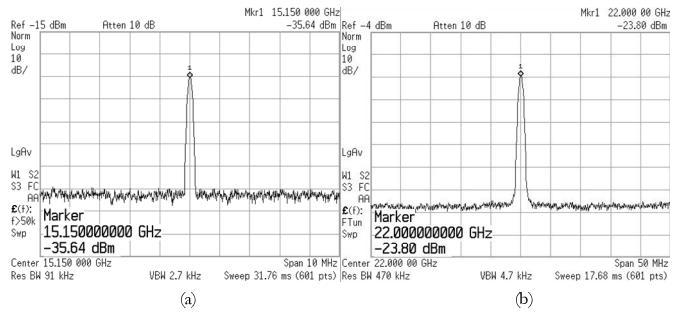


Figure 8. Output spectrum for (a) Min. input frequency (30.3 GHz) (a) Max. input frequency (44 GHz)

TABLE I. COMPARISON WITH PUBLISHED RESULTS

Ref	Process (nm)	Op. Freq (GHz)	L. R. (%)	Pin (dBm)	Power (mW)	Ph. Noise (dBc/Hz @ 1 MHz)
[4]	180	43 - 49	13	0	8	-120
[5]	130	50 - 62	21.42	0	10.8	-124.9
[6]	130	25 - 31.2	22	0	1.86	-130
[7]	90	35.7 - 54.9	42.3	5	0.8	-118.4
This work	65	30.3 - 44	36.9	-2	9*	-131.6

* Total consumption including both I-Q divider

ACKNOWLEDGMENT

The authors would like to thank Philips Research Eindhoven for technology access.

REFERENCES

- [1] H. M. Cheema, R. Mahmoudi, M. A. T. Sanduleanu, and A. van Roermund, "A Ka Band, Static, MCML Frequency Divider, in Standard 90nm-CMOS LP for 60 GHz Applications," *IEEE Radio Frequency Integrated Circuit Symposium (RFIC)*, pp. 541-544, June 2008.
- [2] Y. Mo, E. Skafidas, R. Evans, and I. Mareels, "50 GHz static frequency divider in 130 nm CMOS," *Electronics Letters*, vol. 44, no. 4, pp. 285-286, 2008.
- [3] H. Wu, A. Hajimiri, "A 19GHz 0.5mW 0.35μm CMOS Frequency Divider with Shunt-Peaking Locking-Range Enhancement," *ISSCC Dig. Tech. Papers*, pp. 412-413, Feb., 2001.
- [4] Yi-Jan Emery et al., "A Wide Operation Range CMOS Frequency Divider for 60 GHz Dual-Conversion Receiver," *IEEE Radio Frequency Integrated Circuit Symposium (RFIC)*, June 2006.
- [5] Yu-Hang Wong, Wei-Heng Lin, Jeng-Han Tsai, Tian-Wei Huang, "A 50-to-62GHz Wide-Locking-Range CMOS Injection-Locked Frequency Divider with Transformer Feedback," *IEEE Radio Frequency Integrated Circuit Symposium (RFIC)*, pp. 435-438, June 2008.
- [6] Hsien-Ku Chen, Da-Chiang Chang, Ying-Zhong Juang, Shey-Shi Lu, "A 30-GHz Wideband Low-Power CMOS Injection-Locked Frequency Divider for 60-GHz Wireless-LAN," *IEEE Microwave and Wireless Components Letters*, pp. 145-147, Feb. 2008.
- [7] Tang -Nian Luo, Yi-Jan Emery et al., "A 0.8-mW 55-GHz Dual-Injection-Locked CMOS Frequency Divider," *IEEE Transactions on Microwave Theory and Techniques*, vol. 56, no. 3, pp. 620-625, March 2008.