A 32-KB Standard CMOS Antifuse One-Time Programmable ROM Embedded in a 16-bit Microcontroller

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***Abstract*—A 32-KB standard CMOS antifuse one-time programmable (OTP) ROM embedded in a 16-bit microcontroller as its program memory is designed and implemented in 0.18-μm standard CMOS technology. The proposed 32-KB OTP ROM cell array consists of 4.2 μm^2 three-transistor (3T) OTP cells where each cell utilizes a thin gate-oxide antifuse, a high-voltage blocking transistor, and an access transistor, which are all compatible with standard CMOS process. In order for high density implementation, the size of the 3T cell has been reduced by 80% in comparison to previous work. The fabricated total chip size, including 32-KB OTP ROM, which can be programmed via external I^2C master device such as universal I^2C serial EEPROM programmer, 16-bit microcontroller with 16-KB program SRAM and 8-KB data SRAM, peripheral circuits to interface other system building blocks, and bonding pads, is 9.9 mm^2. This paper describes the cell, design, and implementation of high-density CMOS OTP ROM, and shows its promising possibilities in embedded applications.**

***Index Terms*—CMOS antifuse, CMOS OTP, embedded PROM, gate-oxide breakdown, I^2C, microcontroller, nonvolatile memory, OTP ROM.**

I. Introduction

CONVENTIONAL program memory (PM) of microcontrollers has generally been implemented by using nonvolatile memories (NVM) such as electrically programmable read-only-memory (EPROM) [1], electrically erasable programmable ROM (EEPROM) [2], flash EEPROM [3]–[5], or ferroelectric memory [6], [7]. However, these NVMs usually require additional processes which lead to a longer process turnaround time, higher complexity, lower reliability, and higher cost in manufacturing. An internal SRAM can be used for PM, but an external PROM [8] is required to store the firmware after power-off.

Additionally, there are various types of one-time programmable (OTP) ROMs based on fusing and antifusing [9], [10] such as polyfusing or utilization of oxide–nitride–oxide (ONO) [11] and metal–oxide–metal [12], [13] as the antifuse (AF) element which are candidates to be used as the PM of microcontrollers. However, polyfusing is not reliable enough for manufacturing, while metal–oxide–metal and ONO require additional processes in order to apply it to standard CMOS products. On the other hand, continuous advances and scaling in CMOS technology has enabled the use of the thin gate-oxide of CMOS as the AF for programming [14], [15]. As the channel length and the gate-oxide thickness are scaled down, the breakdown voltage of the gate-oxide is decreased. The usage of the gate-oxide of CMOS has the great advantage of its feasibility to be applied to standard CMOS circuits directly with no additional processes. Therefore, CMOS gate-oxide AF is a promising candidate to be integrated as the PM of microcontrollers as well as other embedded applications.

In order to program the AF, a high voltage (HV) is applied to the gate-oxide of CMOS to cause a permanent hard breakdown in the dielectric [16]. Using this phenomenon, a three-transistor (3T) cell OTP ROM using standard CMOS gate-oxide AF was proposed in [14]. In [14], the AF cell measurement results showed stable and reliable characteristics after breakdown, and showed promising possibilities to be applied as embedded high density nonvolatile PROM in various analog as well as digital systems.

In this paper, for the first time, we present the high density 32-KB OTP ROM embedded in a 16-bit microcontroller utilized as its PM in 1-poly 6-metal 0.18-μm standard CMOS process. In comparison to previous work, the size of the 3T cell in the OTP ROM is reduced, achieved with careful design without compromising its reliability, in order to integrate the ROM and the microcontroller in a single chip. Breakdown conditions in selected cells for programming as well as leakage disturbances in non-selected cells are carefully considered during the design of the high density OTP ROM array. The embedded OTP ROM can be programmed and read either by externally applying a high voltage and using a logic analysis system with the pattern generator or by utilizing the I^2C serial EEPROM programmer. It has a 32-byte page write mode where 32 bytes of data is programmed simultaneously in a single program cycle. In the reading mode, the 16-bit data is outputted through the sense amplifiers in the output path.

The paper is organized as follows. The design of 1-bit 3T CMOS OTP cell and its breakdown I–V characteristics are discussed in Section II. The design and structure of the 32-KB

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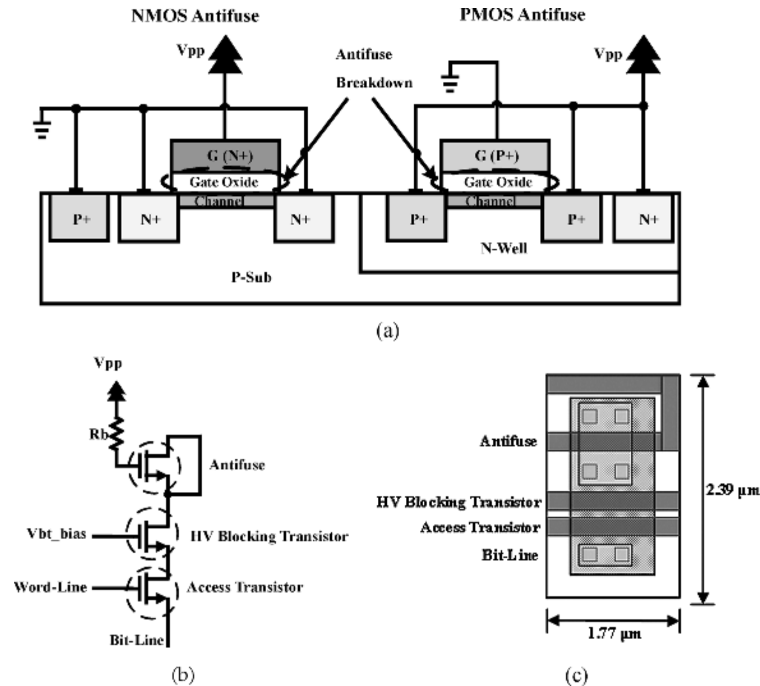

Fig. 1. (a) Cross-sectional view of nMOS and pMOS AF in standard CMOS process. (b) Schematic of 1-bit nMOS 3T OTP memory cell. (c) Layout of 1-bit 3T cell.

CMOS OTP ROM is described in Section III. Section IV deals with the 16-bit microcontroller with embedded OTP ROM as its PM. In Section V, the chip implementation and measurement results are discussed, followed by the conclusion in Section VI.

II. Three-Transistor OTP Cell

Fig. 1(a) shows the cross-sectional view of nMOS and pMOS AF [17] in the programming mode, where applied HV of $V_{\rm PP}$ whose value is approximately three times higher than those of the power supply voltage ($V_{\rm DD}$). The 3T cell is comprised of a nMOS or a pMOS AF, a HV blocking transistor (BT) to prevent other circuits from possible high voltage stress when it is applied to the AF during the programming mode, and an access transistor (AT) for addressing. In our design, as it is represented in Fig. 1(b), all three transistors were specifically designed with the nMOS since higher integration would be more feasible than the PMOS. The area of the 3T cell is 4.2 μm^2, which is an 80% size reduction in comparison to the previously reported cell in [14], with all three transistors in the OTP cell designed with equal widths and minimum lengths. The layout of the 3T cell is shown in Fig. 1(c).

To measure the breakdown I–V characteristics of nMOS AFs of various sizes, the source and drain nodes are grounded and the programming high-voltage (HV $= V_{\rm PP}$) is applied to the gate node using a semiconductor parameter analyzer. The channel is inverted and the source/drain edge regions below the gate are accumulated, which favor higher electric field in edges and channel regions. The equivalent circuit for the breakdown AF can be modeled as a resistor, parasitic MOSs and BJTs, which is shown in [18]. Before breakdown, the gate current shows tunneling characteristics with a very large resistance of $R_{\rm OFF}$ greater than 1 GΩ at $V_{\rm PP} = V_{\rm DD}$. However, the gate-oxide is permanently broken down when $V_{\rm PP}$ exceeds the

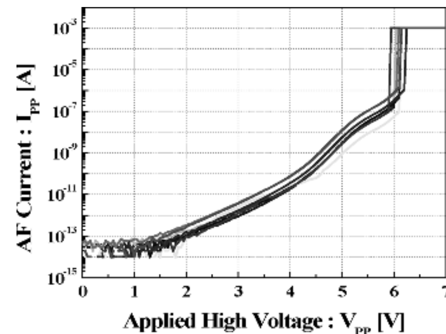

Fig. 2. NMOS antifuse breakdown voltage ($V_{\rm BD}$) measurements of various AFs.

breakdown voltage ($V_{\rm BD}$) of around 6 V for 0.18-μm standard CMOS process (gate-oxide thickness of $T_{\rm OX} = 40$ Å). Fig. 2 shows the nMOS AF $V_{\rm BD}$ measurement characteristics. The current compliance (CC) is set at 1 mA.

The measurement of time-to-breakdown ($T_{\rm BD}$) of 100 samples of nMOS AFs is shown in Fig. 3. From the distribution of $T_{\rm BD}$, the program duty cycle of the program control signal (PGM) can be estimated, and eventually the total time required to program the whole chip can be predicted. In accordance to the measurements, the average value (μ) of $T_{\rm BD}$ is 5.9 ms with the standard deviation (σ) of 3.7 ms. CC and $V_{\rm PP}$ are set at 1 mA and 6.5 V, respectively.

During the breakdown of an AF, higher current supply reduces the value of post-breakdown resistance of $R_{\rm ON}$ [19]. $R_{\rm ON}$ is one of the critical characteristics for AF OTP ROM because its programmed characteristics, such as the access time and sensing margin, are mainly dependent on the $R_{\rm ON}$ value. The value of $R_{\rm ON}$ can be varied with the breakdown position of an AF

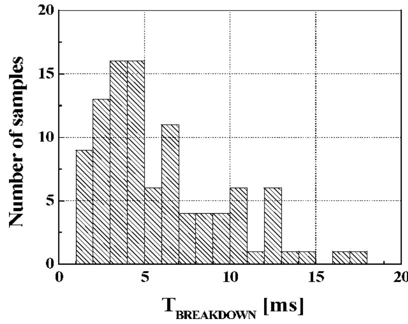

Fig. 3. NMOS antifuse time-to-breakdown ($T_{\rm BD}$) measurements.

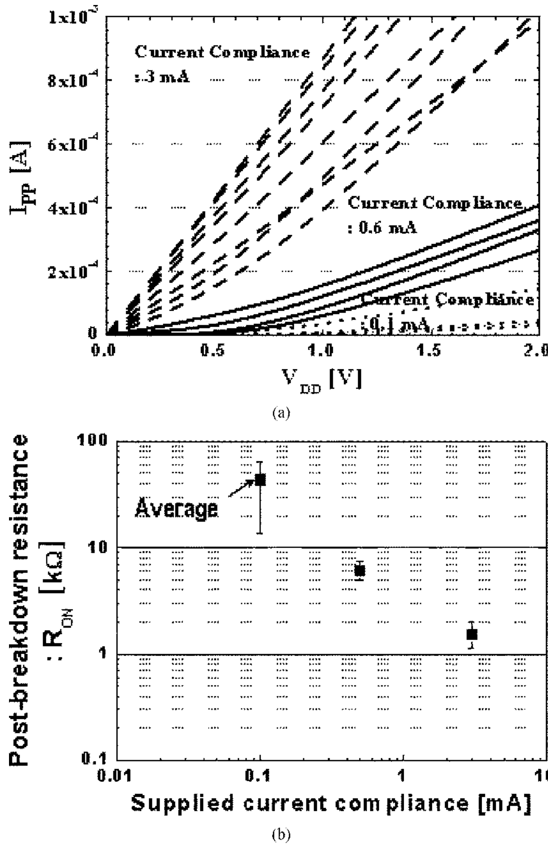

Fig. 4. NMOS antifuse post-breakdown resistance ($R_{\rm ON}$) measurements. (a) $I_{\rm PP}$–$V_{\rm PP}$ characteristics of various AFs after programmed at three different current compliances. (b) Distribution of $R_{\rm ON}$ versus current compliance.

whether the oxide breakdown spot is located near the source/drain region or far from it [18], and the radius of the breakdown spot. However, the most dominant factor the value of $R_{\rm ON}$ depends on is the supplied current when the AF breaks down. The amount of supplied current during the AF breakdown depends on the size of BT and AT. Fig. 4 shows the nMOS AF $R_{\rm ON}$ measurement characteristics. From this measurement we are able to determine the suitable size of the 3T cell considering the trade-off between the amount of integration and $R_{\rm ON}$ value.

The 3T cell is selected when the word-line (WL) is logic "high" and the bit-line (BL) is logic "low". The AF breaks down and a certain amount of programming cell current ($I_{\rm PP}$) dependent on the sizes of BT and AT flows through the BL of the cell. In this work, in order to realize high integration and obtain smaller values of $R_{\rm ON}$ with little variation at the same time, we designed the cell sizes so that approximately 600 μA of $I_{\rm PP}$ per cell would flow in the normal corner condition during the programming mode. The size of AF as well as BT and AT can be designed to be smaller, but $R_{\rm ON}$ would then have a higher probability of becoming larger with higher variation which would affect the access time as well as add more constraints in designing the sense amplifier in the reading mode. Fig. 5 shows the $R_{\rm ON}$ measurement characteristics of two different 3T cells of 100 samples each. The "3T1" cell consists of BT and AT with a larger width while smaller BT and AT form the "3T2" cell ($W_{3T1} = 6W_{3T2}$). Both cells have equal AF width and minimum lengths. It can be seen that careful sizing is required in designing the cell since BT/AT with minimized widths may result in large $R_{\rm ON}$ with much variation.

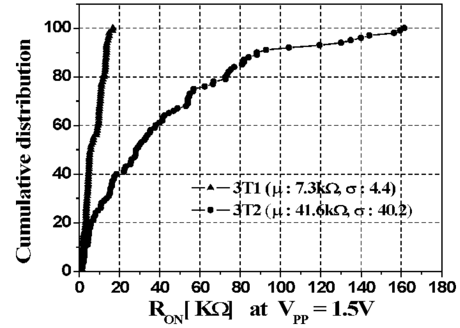

Fig. 5. $R_{\rm ON}$ measurements of 3T cells with different BT/AT sizing.

The cell is nonselected when WL is "low" while BL is "high/low" or when WL and BL are both "high". In any case, AT is "off" for the nonselected cell. In the nonselected programming mode, after power-on, both $V_{\rm PP}$ and $V_{\rm bt_bias}$ $(V_{\rm PP}/2) = 0$ V and BT is also "off" initially. In this mode, there are two different cases where the cell has an unbroken AF or it already has a broken AF. The major concern in the former case is that the AF must not breakdown when HV is applied. As long as HV is not applied between the two electrodes of AF, breakdown will not occur. This is shown in Fig. 6(a) and (b), where the voltage of tied source/drain node of AF is high enough so that the gate-oxide is not ruptured during programming. Instead, when $V_{\rm PP}$ is applied to the nonselected cell, a small amount of gate-induced drain leakage (GIDL) [20] current flows from both the BT drain and AT drain to the substrate. Fig. 6(c) shows the measured characteristics of nonselected cell with unbroken AF in the programming mode for possible disturbances. By comparing the two graphs, the GIDL current increases more rapidly than that of the other. As $V_{\rm PP}$ is increased from $V_{\rm PP_init}$ $(= 0\,{\rm V})$ while AT is turned off, the GIDL current of AT appears before that of BT. But as $V_{\rm PP}$ is further increased, $V_{\rm bt_bias}$ also increases and when it reaches the point where $V_{\rm bt_bias}$ is high enough to turn on BT, the source voltage of BT immediately follows the drain voltage of BT until it reaches $V_{\rm bt_bias} - V_{\rm TH}$ and BT turns off. When $V_{\rm PP}$ is increased above 5 V, the two current plots are overlapped because their dominant GIDL current is that of BT in the higher voltage. Therefore, the two graphs

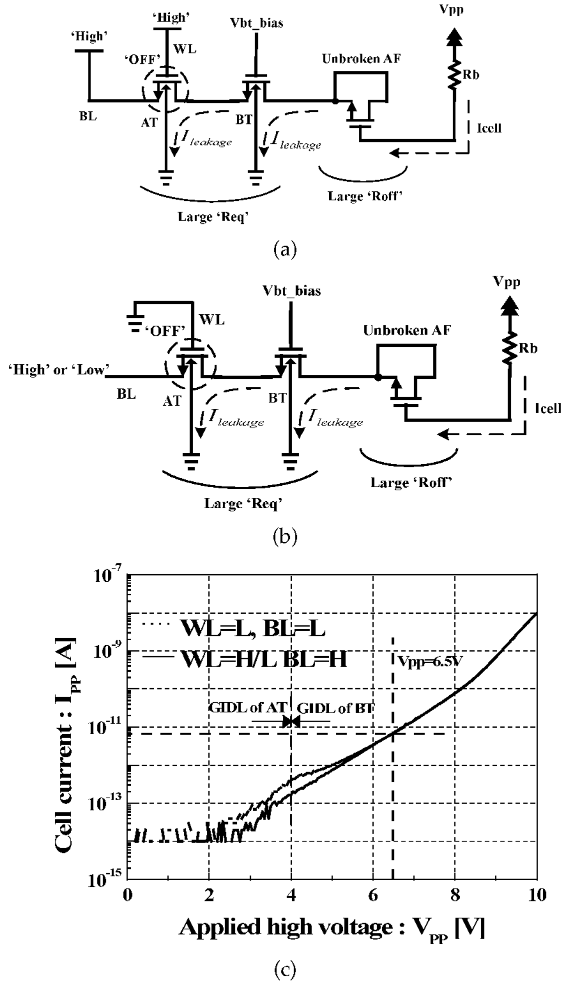

Fig. 6. Leakage characteristics of nonselected cell with unbroken AF in the programming mode. (a) WL and BL are both "high". (b) WL is "low" while BL is "high/low". (c) Measurements.

overlap above 5 V of $V_{\rm PP}$, which is the point when the drain voltage of AT reaches $V_{\rm bt_bias} - V_{\rm TH}$.

In the latter case shown in Fig. 7(a), the AF is already broken and when HV is applied, the drain node of BT will be close to HV, which induces GIDL current that may rupture the gate of BT or bring about high leakage current. The voltage between the drain and gate node of BT will be $V_{\rm DG_BT} = V_{\rm PP} - V_{\rm bt_bias}$ which can be as high as 4.7 V if $V_{\rm bt_bias} = V_{\rm DD} = 1.8$ V. Even though the area of which the drain is overlapped with the gate is very small and that the junction breakdown voltage of BT is very high, the reliability of BT can be increased by applying a higher BT gate bias voltage of $V_{\rm bt_bias} > V_{\rm DD}$ so that $V_{\rm DG_BT} = V_{\rm PP} - V_{\rm bt_bias}$ becomes lower. For the nonselected cell with broken AF, to investigate long-duration and high-voltage reliability of BT, Fig. 7(b) plots the GIDL current versus elapsed time for 1-hour at three different programming voltages of 6.5 V, 6.7 V, and 6.9 V at $V_{\rm bt_bias} = V_{\rm DD} = 1.8$ V. Even though this is nonproblematic in the operation of a single cell, in order to increase the reliability of BT in the programming mode of the ROM array, an internal BT biasing circuitry is included in order to generate a voltage higher than that of $V_{\rm DD}$. The BT bias circuit is shown in Fig. 8. With the READ_bar

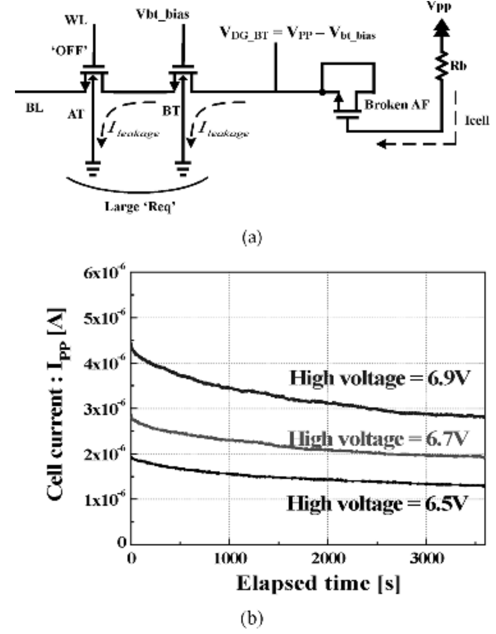

Fig. 7. (a) Schematic of 3T nonselected cell with already broken AF in the programming mode. (b) GIDL of nonselected with broken AF versus elapsed time at different programming high voltages.

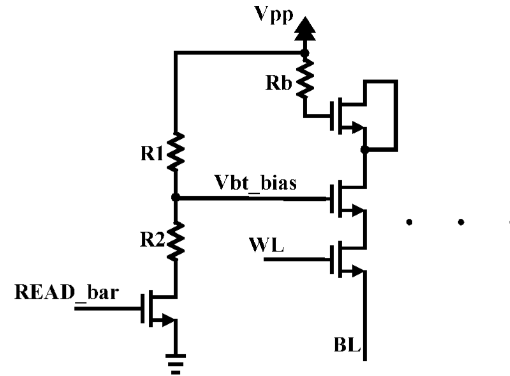

Fig. 8. Schematic of $V_{\rm bt_bias}$ circuit.

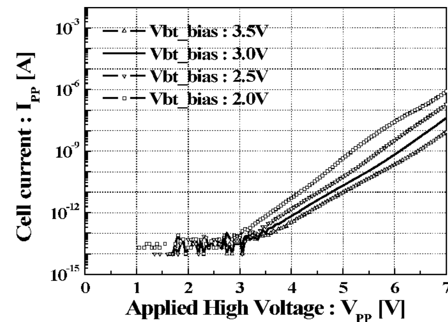

Fig. 9. Measurements showing the effect of higher $V_{\rm bt_bias}$.

signal enabled in the programming mode, the following simple equation of voltage division can be applied:

$$\left(\frac{R_2}{R_1 + R_2}\right) \times V_{\rm pp} = V_{\rm bt_bias}. \tag{1}$$

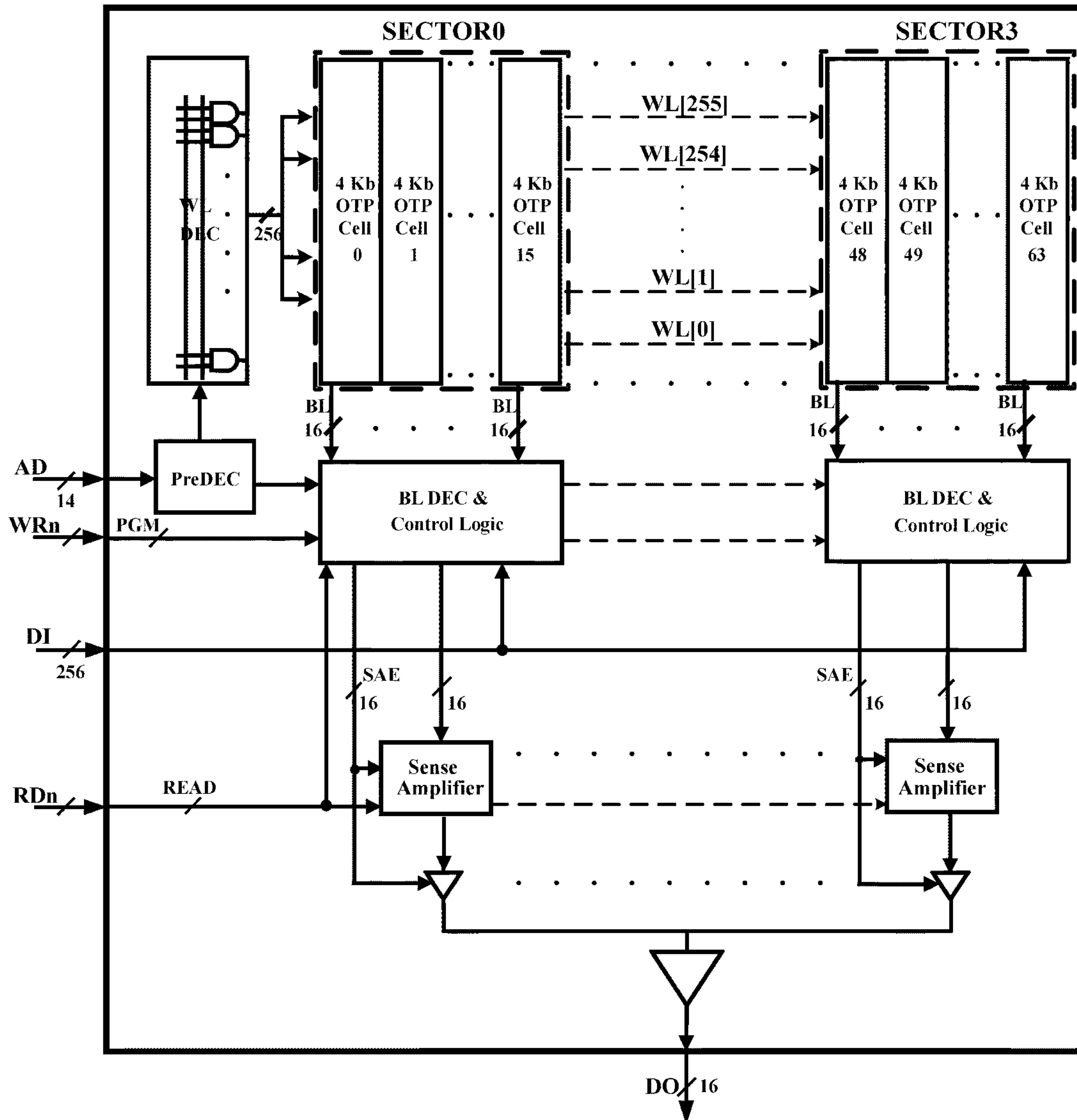

Fig. 10. Block diagram of 32-KB OTP ROM array.

As shown in Fig. 9, less GIDL current flows when higher $V_{\mathrm{bt_bias}}$ is applied to the BT, thus enabling a more reliable 3T cell.

III. 32-KB OTP ROM

To realize a high density OTP ROM array, key factors such as low area consumption and reliable operation during the programming mode are considered. The proposed 32-KB (16K $\times$16 bit organization) OTP ROM is composed of a 32-KB memory cell array and other typical peripheral blocks such as address decoders, sense amplifiers (SA), and control logic block as illustrated in Fig. 10. The reduced 3T cell provides the ability to minimize the overall area consumption because the memory cell occupies over 60% of the total area of the ROM. Also, since OTP ROM uses high voltage to program the storage cell, the architecture for high voltage and long programming duration is necessary for reliable operation. As mentioned in the previous section, the GIDL current in the nonselected cells is at most a few μA per cell in the worst case. In several thousands of OTP cell array, however, the leakage current can be more than several mA. This current and the blocking resistance R_{B} make programming voltage drop between the two electrodes of AF. In order to settle this problem, a unit block, which is composed of 4 Kb (16 b by 256 b) of OTP cells, is introduced in the design of the ROM so that the maximum amount of leakage current per BL is limited. The 32-KB memory cell is comprised of four 8-KB sectors, where each sector consists of sixteen 4-Kb OTP cell unit blocks. The static 8-bit WL (Row) decoder and the 6-bit BL (Column) decoder, which are located in the left and bottom part of the memory cell, respectively, form the 14-bit address decoder required to access the 32 KBs of memory cells. The program page width per cycle is 32 bytes and the reading width is 16 bits. 64 SAs per sector, which totals up to 256 SAs for the whole chip, is located below the BL decoders. The control logic which controls the transition between the programming and reading modes, as well as the data I/O buffers are also located in the bottom part of the ROM.

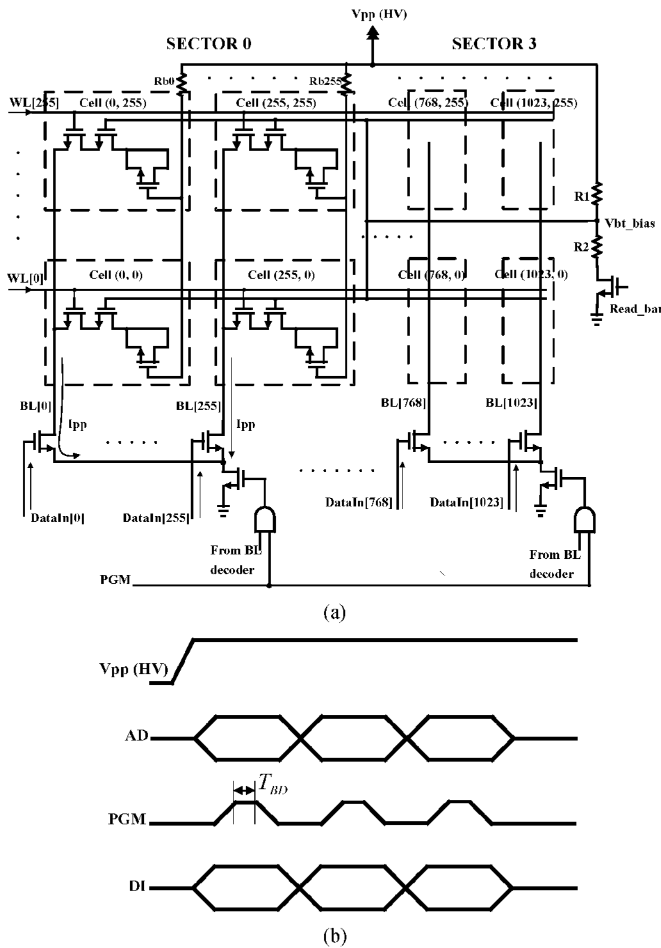

Fig. 11. (a) Schematic and (b) timing waveform in the programming mode.

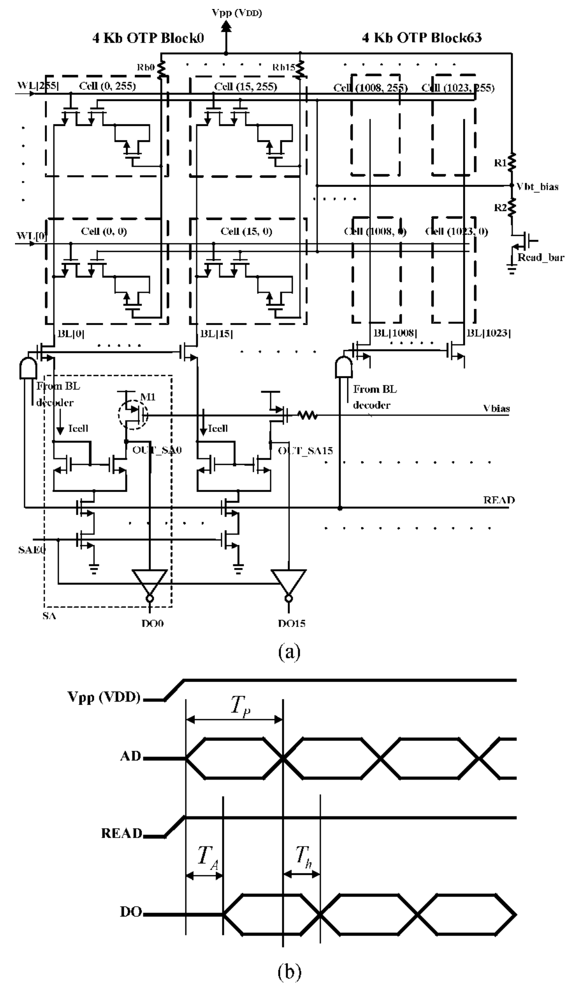

Fig. 12. (a) Schematic and (b) timing waveform in the reading mode.

The total area of the ROM, excluding the microcontroller part, is 2200 μm$\times$900 μm.

In the programming mode, an externally supplied HV is applied to the tied gates of all nMOS AFs ($V_{\rm PP}$ node) through external pins, and only the selected AFs corresponding to the WL and BL, gets ruptured. In order to reduce the programming time, 32 bytes of OTP cells are programmed simultaneously. As mentioned in the previous section, the cell is designed so that approximately 600 μA of $I_{\rm PP}$ per cell flows when AF breaks down, which totals up to a maximum value of over 150 mA in the case where the programming input data is logic "high" for all 32 bytes. In order to alleviate the effect of great amount of programming current, excessive external $V_{\rm PP}$ and ground (GND) pins are assigned. The schematic of the OTP cell array and the timing waveform for the programming mode is shown in Fig. 11(a) and (b), respectively. With the input address (AD) and PGM enabled, the value of the data input (DI) determines whether "1" or "0" will be programmed. If the DI is logic "high", then breakdown will occur in the corresponding cell and thus programmed as "1". When the DI is logic "low", then the AF in the selected cell will not rupture and thus programmed as "0". Although most of the AF gets ruptured before 15 ms at $V_{\rm PP}$ of 6.5 V, in order to be certain of reliable breakdown of all the programming cells, the duty of the PGM signal ($T_{\rm BD}$) is set to be 20 ms. The $V_{\rm PP}$, $V_{\rm bt_bias}$ and $V_{\rm DD}$ in the programming mode are 6.5 V, 3.25 V ($V_{\rm PP}/2$), and 1.8 V, respectively.

In the reading mode, $V_{\rm DD}$ is applied to the $V_{\rm PP}$ node. The reading current flows through the AF to BL at the programmed cell, which is detected by the BL SA, while a very small tunneling current (< 100 pA) flows at the nonprogrammed (with unbroken AF) cell. The cell current of a programmed cell is in the range of a few μA to several tens of μA, depending on the size of $R_{\rm ON}$. Each SA compares the cell current to that of a reference current, a current value which can be controlled by an external SA bias pin. If the cell current is larger than the reference current, the data is "1", and vice versa. The voltage of the BL node in the reading mode is in the vicinity of 1 V.

The schematic of the simple SA is shown in Fig. 12(a). In order to sense the programmed data correctly even for a cell with a large $R_{\rm ON}$, the SA is specifically designed with a high sensing margin to overcome the problems of low cell current. The sensing margin depends on the M1 transistor sizing of the SA. However, a trade-off exists between the sensitivity and the speed of the SA, thus leading to a longer read access time. The SA is designed to sense cells with high $R_{\rm ON}$ values up to 500 kΩ with a speed of 10 MHz at typical corner conditions with 1.8 V $\pm$ 5% supply voltage and 85 °C. The reading width

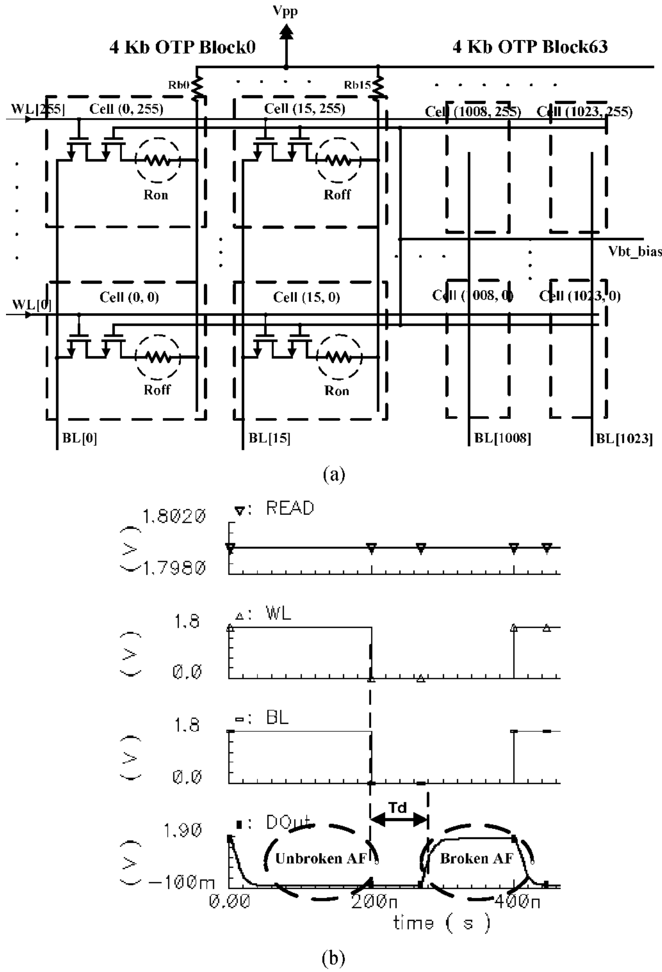

Fig. 13. Reading Simulation: (a) modeling of programmed AF; (b) simulated waveform.

is 16 bits. Every four 4-Kb cell blocks share 16 SAs to support $\times$ 16 organization of the block. With the enabled reading control signal (READ) and the input address, the word data from the corresponding address is sensed through the selected 16 SAs located below the cell array. The selection of the SAs is done by a combination of the READ and SA enable (SAE) signal. The schematic of the OTP cell array and the timing waveform for the reading mode is shown in Fig. 12(a) and (b), respectively. The V_{PP}, $V_{\mathrm{bt_bias}}$, and V_{DD} in the reading mode are 1.8 V, 1.8 V, and 1.8 V, respectively.

The simulation performed for two sensing cycles in the reading mode is shown in Fig. 13. The programmed AF can be modeled as a resistor in the reading mode as shown in Fig. 13(a). In order for the simulation, broken AFs (data "1") are modeled as resistors (R_{ON}) with values from 5 kΩ to 500 kΩ (worst case). Unbroken AFs (data "0"), on the other hand, are modeled as resistors with values of 1 GΩ (R_{OFF}). The simulated waveforms are shown in Fig. 13(b). "WL" and "BL" in the figure represent input LSB address bits of wordline and bitline predecoders. So in this particular simulation the programmed "0" cell is located in $\mathrm{WL}[7:0] = 00000001$, $\mathrm{BL}[5:0] = 000001$ while programmed "1" cell is located in $\mathrm{WL}[7:0] = 00000000$, $\mathrm{BL}[5:0] = 000000$.

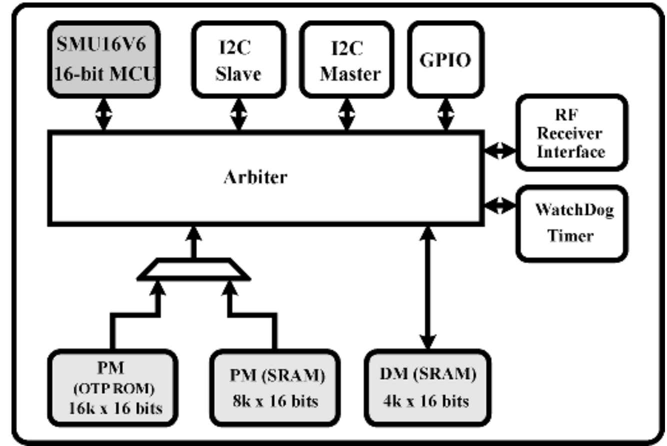

Fig. 14. The block diagram of fabricated chip.

IV. 32-KB CMOS OTP ROM Embedded in 16-bit Microcontroller

The block diagram of the 32-KB OTP ROM embedded in a 16-bit microcontroller is shown in Fig. 14. The microcontroller is a three-stage pipelined Harvard RISC architecture with 32 instructions of 16-bit wide. It contains 8 KB of internal SRAM data memory (DM) and 50-bit general purpose I/Os (GPIO), a WatchDog timer for fail-safe or power minimization purposes, and a RF interface block which can control an external RF transceiver. Besides the embedded 32-KB OTP ROM as its PM, a conventional 16-KB of internal SRAM PM (for external serial EEPROM booting) is also included for testing. The microcontroller is designed to operate at 50 MHz with a performance of 0.95 MIPS/MHz at normal core supply voltage of 1.8 V $\pm$ 5% and a temperature range of 0 °C to 85 °C. The supply voltage which is regulated to 1.8 V using built-in regulator can vary from 2.5 V to 3.3 V so that this microcontroller with the OTP ROM is adequate for lithium-ion coin type battery-powered applications.

There are three different test modes for testing in which the selection is done externally. In the first test mode, the microcontroller can choose either the OTP ROM or the built-in SRAM as its PM by monitoring memory selection pin. In the second test mode, the microcontroller is disabled and the OTP ROM can be programmed and read by the universal $\mathrm{I^2C}$ serial EEPROM programmer through the $\mathrm{I^2C}$ slave interface which is connected directly to the arbiter block. In the third test mode, only the OTP ROM is selected and the data can be programmed and read externally through the logic analysis system with a pattern generator. In this mode, all other digital blocks except PAD I/Os are disabled and all PAD I/Os change their roles as the direct control signals and data bus for the OTP ROM so that the ROM has the parallel interface. This mode is provided to test the OTP ROM even if all other digital blocks do not work properly. In addition, there are some special blocks which are the RF transceiver interface and the WatchDog timer. In case of battery-powered systems, the WatchDog timer can provide a sleep/wake-up mechanism which minimizes the power consumption of the entire system.

TABLE I
SUMMARY OF KEY FEATURES OF CHIP

Technology	1-Poly 6-Metal 0.18 μm CMOS
Oxide Thickness T_{OX}	40 Å
Cell Type	3 NMOSs
3T Cell area	4.2 μm²
32 KB ROM area (w/o microcontroller part)	2200 μm x 900 μm
Die Size (incl. bonding pads)	3300 μm x 3000 μm
ROM Configuration	16K x 16 bit
Programming Mode Current Consumption	170 mA (max.) per page at 6.5 V V_{PP}
Reading Mode Current Consumption	1.1 mA at 4 MHz,1.8 V V_{DD}
Package	100-pin LQFP
Supply Voltage	HV (V_{PP}) : 6.5V, V_{DD} : 1.8V (core), 3.3V (I/O)

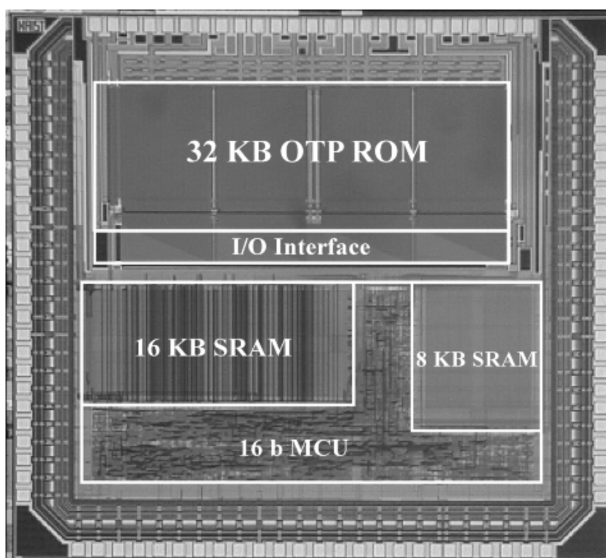

Fig. 15. The microphotograph of fabricated chip using 0.18-μm standard CMOS technology.

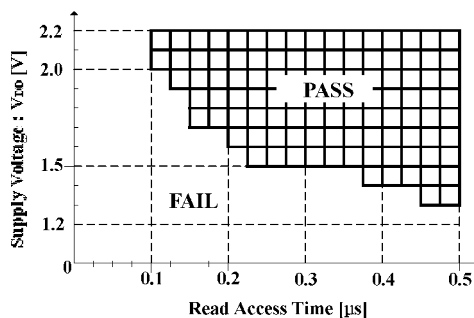

Fig. 16. The Shmoo plot in the reading mode.

V. IMPLEMENTATION AND MEASUREMENTS

The chip microphotograph of the implemented chip is shown in Fig. 15. The chip consists of 32-KB OTP ROM, 16-bit microcontroller, 8-KB SRAM, 16-KB SRAM, and peripheral circuits, using 1-poly 6-metal 0.18-μm standard CMOS process. The 32-KB CMOS OTP ROM is located in the top part of the chip with the I/O interface in the middle. The 16-bit microcontroller with 16-KB SRAM, 8-KB SRAM, and peripheral circuits are located in the bottom part of the chip. The total area of the chip including the bonding pads is 3.3 mm $\times$3 mm. The chip is assembled in a standard 100-pin LQFP.

First, we confirmed the operation of the OTP ROM in the third test selection mode by externally applying the test signals using a logic analysis system with the pattern generator. Various data input patterns were applied in the programming mode to measure the range of programming current per program cycle. Second, in the second test mode, the universal serial EEPROM programmer was used to program and read the ROM through the I^2C slave interface. We finally confirmed the successful operation of the microcontroller adopting the OTP ROM as its PM under typical conditions on an evaluation board. The key features of the chip are summarized in Table I. The cell size is 4.2 μm^2 using three nMOS transistors. The maximum current consumption (when all 32-byte data input is logic "high") per program cycle in the programming mode is in the range from 160 to 180 mA per page at 6.5 V V_{PP}. In the reading mode, the current consumption is 1.1 mA at 4 MHz at 1.8 V V_{DD}. Fig. 16 shows the measured Shmoo plot of the ROM in the reading mode.

VI. CONCLUSION

A 32-KB standard CMOS antifuse one-time programmable ROM embedded in a 16-bit microcontroller as its program memory was designed and implemented in 1-poly 6-metal 0.18-μm standard CMOS technology. To minimize the size of the ROM for feasible integration without compromising the breakdown characteristics in a nonideal way, a 3T cell, with 80% in size reduction, was designed. The 3T OTP cell has an area of 4.2 μm^2, while the total area of the whole chip including the 32-KB OTP ROM, 16-bit microcontroller with 8-KB/16-KB SRAM, peripheral circuits, and bonding pads is 9.9 mm^2. The total current consumption of the 32-KB OTP ROM is as low as 1.1 mA at 4MHz so that this microcontroller can be used in the lithium-ion coin type battery-powered applications. The CMOS OTP ROM, having the advantage of its compatibility with standard CMOS technology and thus lowering the cost and adding versatility, guaranteeing high density and high yield, shows promising capabilities to be applicable to many embedded analog and digital systems.

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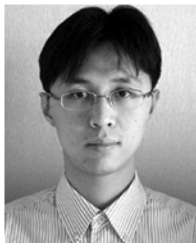

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