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21.7 A 32kb 10T Subthreshold SRAM Array with Bit-Interleaving and Differential Read Scheme in 90nm CMOS

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For robust subthreshold SRAMs, 8T or 10T subthreshold SRAMs based on single-ended read sensing have been proposed [1-3]. While the schemes in [1-3] improve the read stability and writability significantly, their single-ended sensing methods still suffer from reduced bitline swing due to bitline noise. In addition, the previous schemes do not have efficient bit-interleaving in the column structure, which is critical to cope with multiple-bit soft errors [4]. In this paper, we present a 10T subthreshold SRAM with efficient bit-interleaving for soft-error immunity and fully differential read for better stability.

Figure 21.7.1 shows the 10T SRAM cell. In read mode, WL is enabled and VGND is forced to ground while W_WL remains disabled as shown in the timing diagram. Since the disabled W_WL makes the nodes 'Q' and 'QB' isolated from the bitlines during the read mode, the read static noise margin (SNM) of this 10T SRAM is almost same as the hold SNM of conventional 6T SRAM. During the write mode, both WL and W_WL are enabled to transfer the write data to cell node from the bitline. To compensate weak writability, V_{WL} and V_{W_WL} are boosted by 33% of 0.3V V_{DD}. Since the gate input boosting overwhelms the sizing effect in the subthreshold region, we obtain strong writability without incurring a large area penalty in spite of having series transistors. Figure 21.7.1 shows 100mV boosting gives good writability even in the worst-case process corner. To reduce the area overhead, four columns share a common VGND node (Fig. 21.7.2). The pull-down strength of VGND driver is degraded due to process variation, so the dynamic-threshold MOS (DTMOS) technique is employed to mitigate this effect. The pull-down NMOS of the VGND driver is forward-biased during read, increasing the pull-down drive current.

As shown in the array structure in Fig. 21.7.2, WL is shared by the cells in a row and W_WL is shared by the cells in a column. Since both WL and W_WL must be enabled to write a cell, each column is selected individually depending on the value of W_WL. This unique feature can be used for bit-interleaving to reduce the multiple-bit soft errors. Soft-error rate is expected to be significantly higher in subthreshold SRAM than that in super-threshold SRAM due to the lower V_{DD} and the smaller gate capacitance in subthreshold region. Previous subthreshold SRAMs [1,2] do not allow bit-interleaving because the cells that are in the unselected columns but share the wordline with the selected cells experience significant stability degradation during write mode. Therefore, a logic word is composed of all cells sharing a wordline so that the design is exposed to multiple bit soft errors. (Fig. 21.7.3) On the other hand, in our technique, writing a cell does not affect hold stability of other cells along the same wordline since W_WL is shared by the cells in a column. When the W_WL of a column is raised for writing a cell, W_WLs of other columns still stay at 0V. Hence, the rise of WL does not affect hold stability of unwritten cells sharing the WL. Monte-Carlo simulation results, shown in Fig. 21.7.3, show that the hold stability of unwritten cells sharing W_WL does not degrade during write. Despite the influence of enabled W_WL and VGND, the worst hold SNM shows improvement of 25% compared to conventional 6T SRAM since the pull-up of NMOS transistors (NL or NR) complements weak PMOS at FS process corner, which is the worst case corner for hold stability. Since the hold stability in adjacent cells is not affected during write, bit-interleaving is efficiently implemented in our design, achieving soft-error tolerance with conventional ECC [4].

Another characteristic of our cell is the fully differential read, which improves the bitline noise immunity significantly during read. The column structure in Fig. 21.7.4 explains the read mechanism. When read begins, the wordline of the accessed SRAM cells is raised and precharge signal (PRE_CH) is disabled. Depending on the data value of the accessed cell, one of the precharged bitlines (BL or BLB) starts discharging. The unfolded circuit diagram, which is equivalent to a column with the worst,case leakage condition, is also shown in Fig. 21.7.4. During the read, the leakage current through unselected cells (storing complementary value to the accessed cell) impedes a successful read. In single-ended READ structure, leakage makes it difficult to distinguish a logic high and low from the developed bitline voltage [3]. Since a differential read does not solely depend on the trip voltage of an inverter, it is more tolerant to bitline leakage noise. We employ the dynamic DCVSL technique to further increase leakage tolerance. In Fig. 21.7.4, the discharge of BL turns on keeper M2 and bitline leakage current in BLB is compensated by the drive current of M2. The graph in Fig. 21.7.4 shows the effectiveness of the DCVSL differential read. The simulation results show that $0.7V_{DD}$ bitline differential develops for 1024 cells per bitline at 25°C.

In order to achieve larger bitline swing, read circuitry using cross-coupled inverters is included per each column. The footer transistor M0 of Fig. 21.7.4 prevents malfunction induced by intra-die variation inside the read circuitry. Drive current flowing through M0 is almost negligible before there is significant discharging from a bitline, excluding the influence of intra-die variation inside the read circuitry. Leakage current through a write driver reduces bitline swing, so to reduce this leakage, stacking transistors are employed (Fig. 21.7.4). Since a boosted signal is used for W_WL and W_EN, degradation of write stability resulting from IR-drop of the stacked NMOS structure in the write driver is almost negligible.

An alternative 10T cell with differential bitlines can also be implemented by simply adding two read transistors and the complementary bitline to the single-ended-read 8T cell [2]. That implementation, however, does not allow bit-interleaving. The unique characteristic of our cell is to allow both bit-interleaving and differential read with the same number of devices (10T) in a cell.

The SRAM test-chip is fabricated in a 90nm CMOS technology (Fig. 21.7.7). For leakage comparison, 49kb arrays are implemented for both the conventional 6T cell and our 10T cell. Fig. 21.7.5 shows that the leakage power consumption of our SRAM is close to that of the 6T cell (between 0.96× and 1.1×) even though it has extra transistors in a cell. This is because the subthreshold leakage from the bitline to the cell node is drastically reduced by the stacking of devices in the leakage path. For performance and power measurement, a 32kb (256×128) SRAM array is implemented using the cell. As shown in Fig. 21.7.6, the design operates at 31.25kHz with a 0.18V supply and 33% boosted WL and W_WL. With more aggressive wordline boosting of 80mV, the V_{DD} scales down to 0.16V. At 0.16V V_{DD}, the operating frequency is 500Hz and power consumption is 0.123μW.

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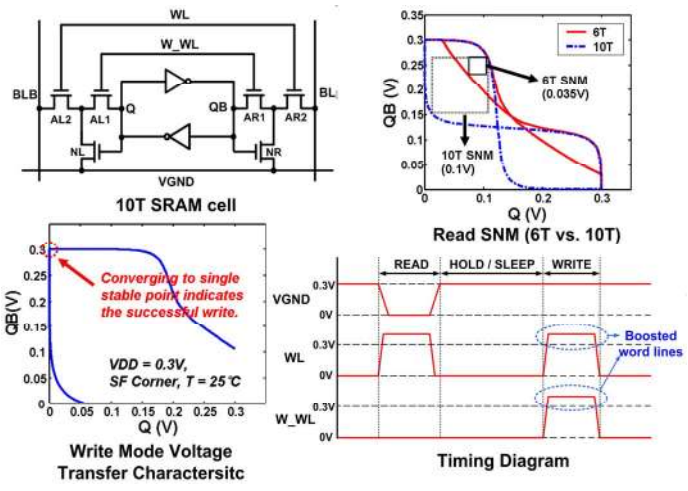
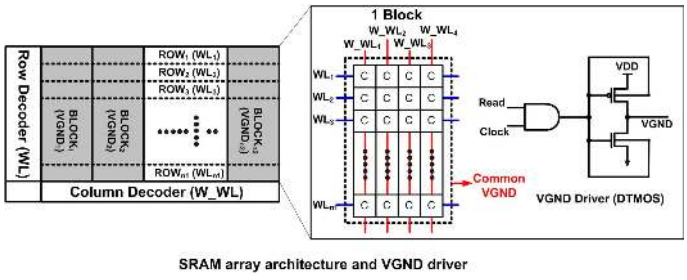


Figure 21.7.1: Our 10T SRAM has almost same read SNM as the hold SNM of conventional 6T SRAM. Boosted W_WL overcomes weak writability of conventional 6T in subthreshold.



SRAM array architecture and VGND driver

Figure 21.7.2: In our architecture, 4 columns have one common VGND node. W_WL is shared by cells in a column. For VGND driver, DTMOS technique is used.

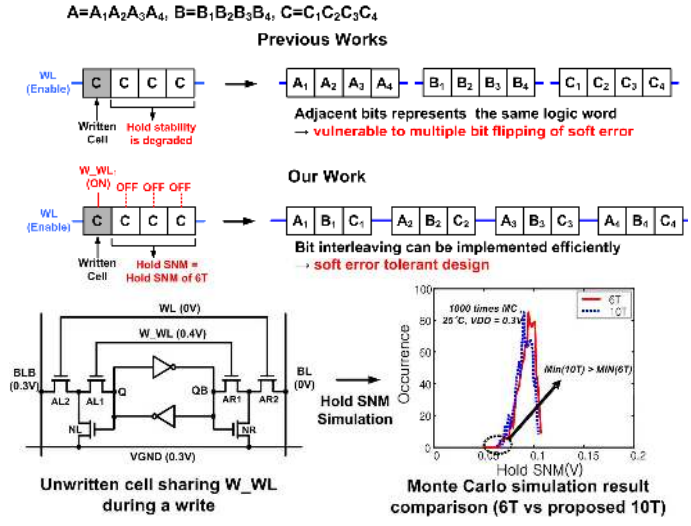


Figure 21.7.3: Writing a cell does not affect the hold stability of other cells in our design. Therefore, we can implement bit-interleaving structure.

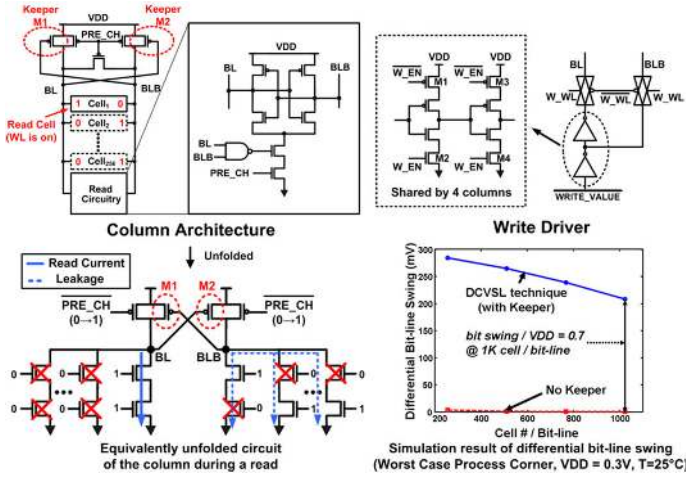


Figure 21.7.4: Differential structure and dynamic DCVSL technique improves bitline swing significantly.

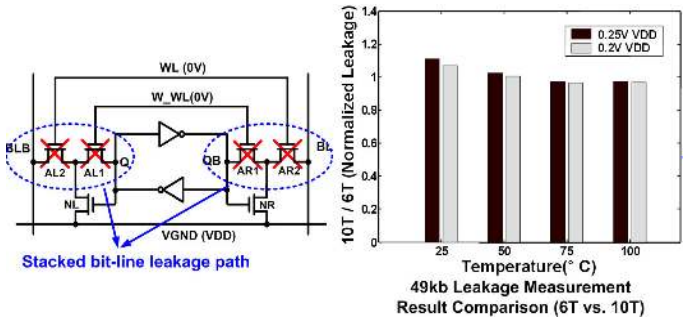


Figure 21.7.5: Leakage measurement result in 49kb 10T SRAM and 49kb conventional 6T.

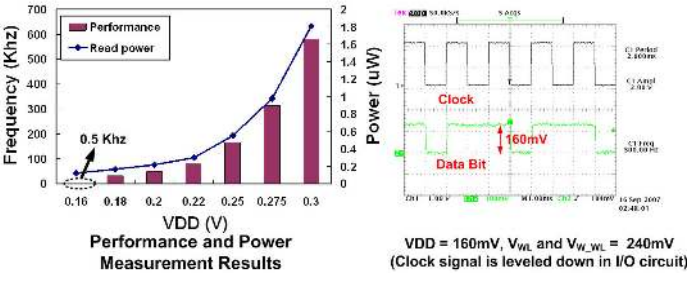


Figure 21.7.6: Test-chip measurement results. Minimum V_{DD} is 160mV.

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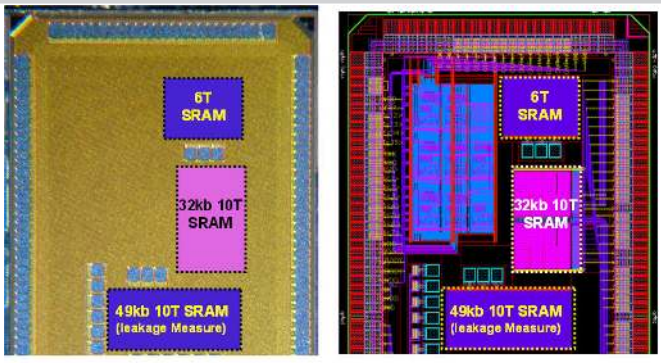

Technology	90nm 8-metal CMOS technology
Chip size	4 x 2 mm^2
VCC min	0.16V, 500hz @ 256 cells/bit-line
Performance	166Khz @ 0.25V VDD, 25°C
Leakage Current (49kb)	1.4µA @ 0.25V, 25°C

Figure 21.7.7: Die micrograph and layout.

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