A 33-Megapixel 120-Frames-Per-Second 2.5-Watt CMOS Image Sensor With Column-Parallel Two-Stage Cyclic Analog-to-Digital Converters

Kazuya Kitamura, *Member, IEEE*, Toshihisa Watabe, Takehide Sawamoto, Tomohiko Kosugi, Tomoyuki Akahori, Tetsuya Iida, Keigo Isobe, Takashi Watanabe, *Member, IEEE*, Hiroshi Shimamoto, *Member, IEEE*, Hiroshi Ohtake, Satoshi Aoyama, *Member, IEEE*, Shoji Kawahito, *Fellow, IEEE*, and Norifumi Egami

***Abstract*—A 33-megapixel 120-frames/s (fps) CMOS image sensor has been developed. The 7808 × 4336 pixel 2.8-μm pixel pitch CMOS image sensor with 12-bit, column-parallel, two-stage, cyclic analog-to-digital converters (ADCs) and 96 parallel low-voltage differential signaling output ports operates at a data rate of 51.2 Gb/s. The pipelined operation of the two cyclic ADCs reduces the conversion time. This ADC architecture also effectively lowers the power consumption by exploiting the amplifier function of the cyclic ADC. The CMOS image sensor implemented with 0.18-μm technology exhibits a sensitivity of 0.76 V/lx · s without a microlens and a random noise of 5.1 $e^-_{\rm rms}$ with no column amplifier gain and 3.0 $e^-_{\rm rms}$ with a gain of 7.5 at 120 fps while dissipating only 2.45 and 2.67 W, respectively.**

***Index Terms*—Analog–digital conversion, CMOS image sensors, high-definition video, high-resolution imaging.**

I. Introduction

THE RECENT growth in demand for high-reality video systems has stimulated research and development efforts to create systems for ultrahigh-definition televisions (UDTVs), sometimes referred to as "Super Hi-Vision" (SHV), as the next generation of television broadcasting systems [1], with the aim of improving the viewing experience by conveying a greater sense of realism through higher resolution pictures.

The full specifications for SHV video signals require images with 4320 lines of 7680 pixels at 120 frames/s (fps) with a 12-bit resolution [2]. To meet this specification, the image sensor will require a readout capability for very high-speed data transfer. The total pixel data output rate of a full-specification SHV sensor will be 47 Gb/s or more.

The column-parallel analog-to-digital converter (ADC) is a key technology for achieving a high pixel rate from a CMOS image sensor. Several image sensors have been developed for UDTVs or digital-cinema applications that use a column-parallel ADC architecture [3]–[6]; however, these do not meet the full specifications for SHV. A 33-megapixel 60-fps CMOS image sensor with a successive-approximation column-parallel ADC [5] has half the pixel rate required by the full SHV specifications and also shows a high power consumption value of 3.7 W. A 17.7-megapixel 120-fps CMOS image sensor with a single-slope column-parallel ADC [6] similarly produces half the pixel rate required to meet the SHV specifications and uses a very high clock frequency to achieve high-speed analog-to-digital (A/D) conversion and a high bit resolution.

A cyclic ADC [7], [8] and a delta–sigma ADC [9] have been also used as column-parallel ADCs but only in image sensors of several megapixels. Cyclic ADCs have a short A/D conversion time and are suitable for use in high-speed image sensors. However, because they contain amplifiers, cyclic ADCs consume more power than other ADCs. The delta–sigma ADC has the advantage of simultaneously producing a low temporal noise and a high bit resolution through an oversampling technique. However, the ADC requires more samplings (e.g., more than 90 samplings for 12 bits) than are required by other cyclic ADCs.

Here, we describe our 33-megapixel 120-fps CMOS image sensor that uses column-parallel two-stage cyclic 12-bit ADCs. To meet the full SHV specifications, we split the cyclic ADC into two stages [10], [11]. The pipelined and parallel operation of the first- and second-stage cyclic ADCs reduces the conversion time effectively. Furthermore, this architecture also helps in reducing the power consumption of the ADC. A prototype image sensor with the ADC architecture and 96 parallel low-voltage differential signaling (LVDS) output ports achieved a frame rate of 120 fps with 33-megapixel resolution while dissipating less than 2.5 W.

We describe the architecture of the sensor and its overall operation in Section II below. In Section III, we discuss the detailed design and operation of the two-stage cyclic ADC, and in Section IV, we describe the implementation of the image sensor and our experimental results.

Manuscript received May 30, 2012; revised August 22, 2012; accepted September 12, 2012. Date of publication October 26, 2012; date of current version November 16, 2012. The review of this paper was arranged by Editor J. R. Tower.

K. Kitamura and T. Watabe are with the NHK Science & Technology Research Laboratories, Tokyo 157-8510, Japan, and also with the Research Institute of Electronics, Shizuoka University, Hamamatsu 432-8011, Japan (e-mail: kitamura.k-hi@nhk.or.jp).

T. Sawamoto was with the Research Institute of Electronics, Shizuoka University, Hamamatsu 432-8011, Japan. He is now with Brookman Technology, Inc., Hamamatsu 430-0936, Japan.

T. Kosugi, T. Akahori, T. Iida, K. Isobe, and S. Aoyama are with Brookman Technology, Inc., Hamamatsu 430-0936, Japan.

T. Watanabe and S. Kawahito are with Brookman Technology, Inc., Hamamatsu 430-0936, Japan, and also with the Research Institute of Electronics, Shizuoka University, Hamamatsu 432-8011, Japan.

H. Shimamoto, H. Ohtake, and N. Egami are with the NHK Science & Technology Research Laboratories, Tokyo 157-8510, Japan.

Digital Object Identifier 10.1109/TED.2012.2220364

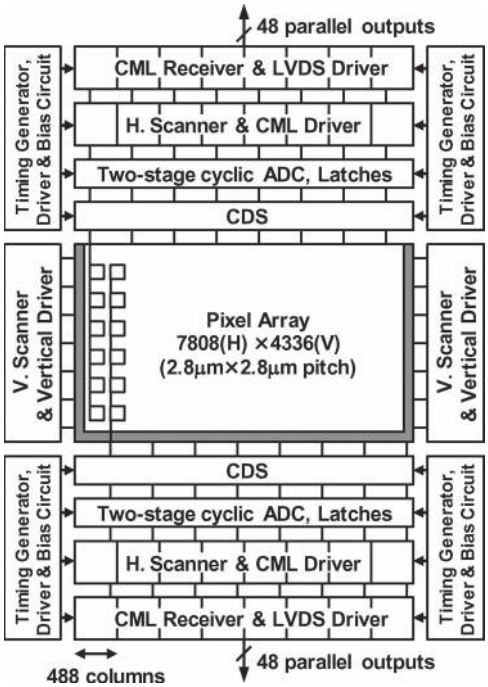

Fig. 1. Block diagram of the 33-megapixel CMOS image sensor.

II. Sensor Architecture

A block diagram of the sensor is shown in Fig. 1. The pixel size of the sensor is 2.8 μm $\times$ 2.8 μm, and the pixel array consists of 7808 pixels $\times$ 4336 pixels. The vertical scanners and drivers are positioned to the left and right of the pixel array. Located above and below the pixel array are the correlated double-sampling (CDS) circuits, column-parallel two-stage cyclic ADCs, latches, horizontal scanners, current mode logic (CML) circuits, and LVDS drivers; to the left and right of these, located are the timing generators, drivers, and bias circuits. A 2.5-transistor two-shared-pixel architecture with pinned photodiodes is used for the pixels. The layout pitch of the column-parallel circuits is 5.6 μm. To decrease the scanning speed, the horizontal scanners are divided into 16 parallel blocks, with each block scanning 488 columns. CML, which permits low-voltage differential signal transfer, is used for horizontal data scanning during the A/D conversion. The sensor has 96 parallel LVDS output ports on its upper and lower faces.

III. Column-Parallel Two-Stage Cyclic ADC

A. Design of the ADC

Fig. 2 shows a simplified schematic of the two-stage cyclic ADC. A single-ended cyclic ADC with internal reference and return-to-zero (RTZ) digital signal feedback [8] is used in each stage of the ADC. An internal reference with a divided capacitor helps to generate a highly accurate three-level reference voltage using two reference wires. The RTZ digital signal feedback technique is effective in reducing the coupling noise from the digital feedback line to the capacitor. Each cyclic ADC generates three-state redundant binary codes expressed in two decision levels (2-bit) for each cycle to relax the demand for precision placed on the comparator [12].

Each stage of the ADC consists of a single-ended amplifier, two capacitors (C_1 and C_2 for the first ADC; C_3 and C_4 for the second ADC), a sub-ADC with two comparators, switch transistors, and a digital-to-analog converter with a decoder. To generate an internal reference, the sampling capacitor C_1 is subdivided into C_{1a} and C_{1b}, whereas capacitor C_3 is divided into C_{3a} and C_{3b}. The output of the first-stage cyclic ADC is connected to the input of the second-stage cyclic ADC by a switching pulse $\phi_{\rm SB}$. As will be described later, the size of the capacitance of the second-stage cyclic ADC is designed to be smaller than that of the first-stage cyclic ADC. In our design, the first-stage cyclic ADC operates for four cycles, and the second-stage cyclic ADC operates for eight cycles so that an overall 12-bit resolution is obtained from the ADC.

B. Timing Diagram and Operation

The operating sequence for the row cycles is illustrated in Fig. 3. The sensor has four pipeline operations, including analog CDS, first-stage cyclic ADC, second-stage cyclic ADC, and horizontal readout.

A timing diagram of the two horizontal periods is shown in Fig. 4. The horizontal scanning time is 1.92 μs at a frame rate of 120 fps with 4336 vertical lines. Labels RT and TX represent control signals for the reset transistor and for the transfer gate in the pixel, respectively. Analog CDS cancels reset noise in the pixel output signal. The analog output signal of the CDS circuit is sampled and converted into 12-bit digital data in the two-stage cyclic ADC. Each cyclic ADC has four operating phases: 1) reset; 2) signal sampling; 3) amplification; and 4) feedback.

The two-stage cyclic ADC operates as follows. First, all the capacitors in the first-stage cyclic ADC are initialized during the reset phase to remove any residual charge [see Fig. 5(a)]. The output signal from the CDS is then sampled in the first-stage cyclic ADC during the signal-sampling phase, and the sub-ADC generates a three-state digital code for the most significant digit [see Fig. 5(b)]. During the amplification phase, the sampled signal is multiplied by a gain of two, and the reference voltage, as determined by the sub-ADC in the signal-sampling phase, is subtracted [see Fig. 5(c)]. At the end of the amplification phase, the sub-ADC generates a three-state digital code. Subsequently, the amplified output signal is returned to the input terminal of the ADC in a feedback phase [see Fig. 5(d)]. The amplification and feedback phases are repeated for three cycles to obtain the first 4-bit resolution. During the amplification phase of the final cycle, the output of the first-stage cyclic ADC is connected to the second-stage cyclic ADC by turning on the switch controlled by $\phi_{\rm SB}$ (see Fig. 2). Fig. 5(e) shows the moment that the output of the first-stage cyclic ADC is sampled to the second-stage cyclic ADC. In the subsequent signal-sampling phase, the switch controlled by $\phi_{\rm SB}$ (see Fig. 2) is turned off and the second-stage cyclic ADC is disconnected from the first-stage cyclic ADC. As a result of this architecture, while the second-stage cyclic ADC performs the 8-bit conversion in eight cycles of the amplification and feedback phases, the first-stage cyclic ADC can sample and

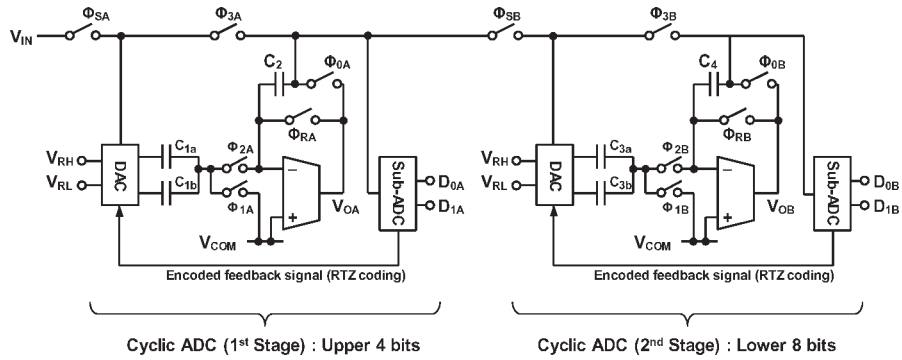

Fig. 2. Simplified diagram of the column-parallel two-stage cyclic ADC.

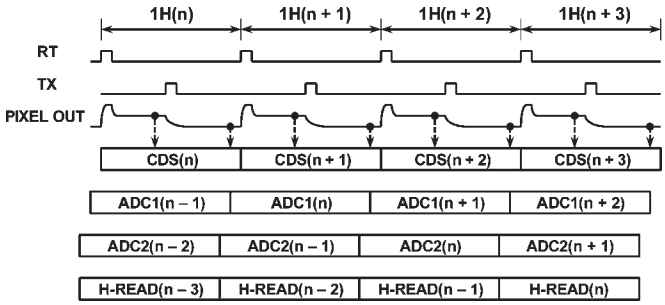

Fig. 3. Pipeline operation sequence for row cycles.

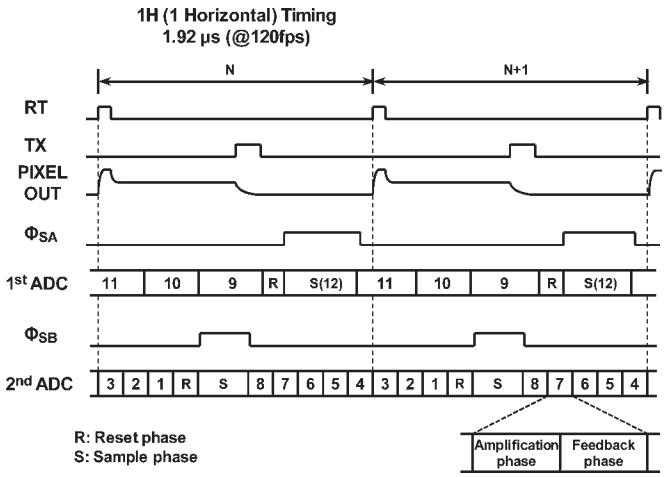

Fig. 4. Timing diagram of the two-stage cyclic ADC.

convert the next pixel signal, which means that the two ADCs work in a pipelined fashion.

C. Power Consumption-Reduction Effect

By exploiting the amplifier function of the cyclic ADC, we designed the two-stage cyclic ADC to have low power consumption. In the two-stage cyclic ADC, the analog signal output from the first-stage cyclic ADC is multiplied by the $(N_1 - 1)$th power of 2 when it is subject to N_1-bit processing. As a result, the second-stage cyclic ADC can tolerate more noise and mismatch error. This property can be effectively used to reduce the total power dissipation of the two-stage cyclic ADC by reducing the size of the sampling capacitor of the second-stage cyclic ADC. However, if the capacitor scaling is extreme, the sampled thermal noise (kT/C noise) generated

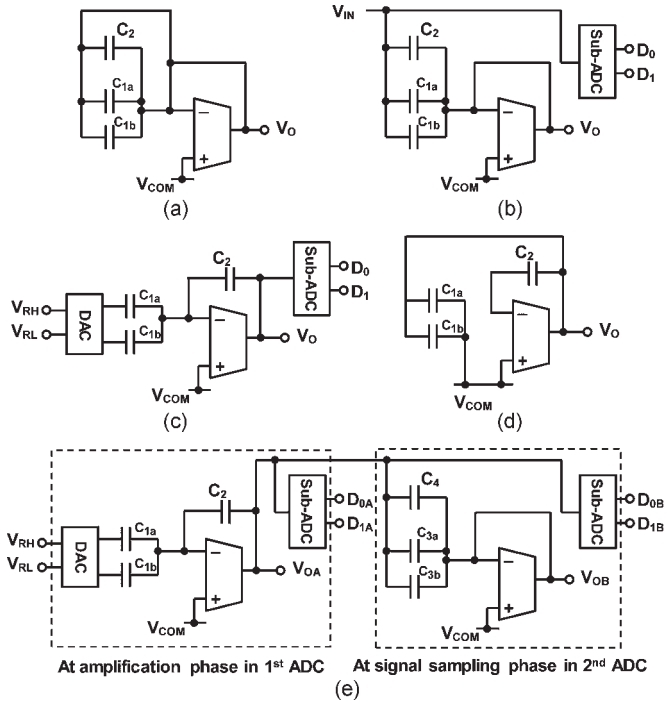

Fig. 5. Phase diagram showing detailed circuit connections: (a) reset; (b) signal sampling; (c) amplification; (d) feedback; and (e) signal transfer from the first-stage cyclic ADC to the second-stage cyclic ADC.

in the second-stage cyclic ADC makes a major contribution to the total noise. The thermal noise is therefore an important factor in optimizing the power of the two-stage cyclic ADC. The bit separation of the two-stage cyclic ADC is also an important factor in optimizing the power consumption because the processing bit number of the first-stage cyclic ADC (N_1) determines the magnification of the analog signal output and the required settling time for each cyclic ADC. Below, we introduce a model for the noise generated in a two-stage cyclic ADC in relation to the scaling factor of the capacitor. We then introduce a model of the current in the cyclic ADC, which uses the settling time of the amplifier. Finally, by using the noise model and the current model of the ADC, we describe power optimization by bit separation.

In a simplified model, it can be assumed that the noise of a cyclic ADC is inversely proportional to the size of the sampling capacitors that are used, provided that the kT/C noise is dominant. With this assumption, the total input-referred noise

power of the first- and second-stage cyclic ADCs can be expressed by

$$\overline{v_{n1}^2} = A\frac{k_BT}{C_s}\left(1+2^{-2}+2^{-4}+\cdots+2^{-2(N_1-1)}\right) \quad (1)$$

$$\overline{v_{n2}^2} = A\frac{k_BT}{C_s\gamma}\left(2^{-2N_1}+2^{-2(N_1+1)}+\cdots+2^{-2(N_F-1)}\right) \quad (2)$$

where A is a constant, C_s is the sampling capacitance of the first-stage cyclic ADC, γ is the capacitor scaling factor expressed as C_3/C_1 in Fig. 2, and N_F is the total process bit number of the two-stage cyclic ADC. The total input-referred noise power of the two-stage cyclic ADC is expressed as

$$\begin{aligned}\overline{v_n^2} &= \overline{v_{n1}^2} + \overline{v_{n2}^2} \\ &= A\frac{k_BT}{C_s}\left\{\frac{1-2^{-2N_1}}{1-2^{-2}} + \frac{2^{-2N_1}}{\gamma}\frac{1-2^{-2(N_F-N_1)}}{1-2^{-2}}\right\} \\ &= A\frac{k_BT}{C_s}F(\gamma, N_1, N_F). \end{aligned} \quad (3)$$

The current in the cyclic ADC is estimated by using the settling time of the amplifier. A large proportion of the power in each cyclic ADC is consumed in the amplifier. The response of the amplifier is operated in a slew-rate-limited mode at the beginning. Later, the amplifier operates in the linear range of the transconductance, where the output signal increases or decreases exponentially with a time constant that is governed by the circuitry of the amplifier. The total settling time is therefore described by using the slewing time and the time of the linear range. If the time for the linear range is n times the time constant, where n is a constant, the settling time is expressed by

$$t_{\rm st} = t_{\rm sl} + n\tau \quad (4)$$

where $t_{\rm sl}$ is the slewing time, and τ is the time constant of the amplifier. In a simplified model where the parasitic capacitance in the amplifier is ignored, the slewing time and the time constant are assumed to be given by

$$t_{\rm sl} \cong \frac{C_s}{I_{SS}}V_s \quad (5)$$

$$\tau \cong \frac{C_s}{g_m} = \frac{C_s}{I_{SS}}V_{\rm od} \quad (6)$$

where I_{SS} is the bias current of the operation amplifier, V_s is the maximum output voltage range, g_m is the transconductance of the input transistor, and $V_{\rm od}$ is the overdriving voltage of the input transistor. Therefore, (4) can be rewritten as

$$t_{\rm st} \cong \left(1+n\frac{V_{\rm od}}{V_s}\right)\frac{C_s}{I_{SS}}V_s = m\frac{C_s}{I_{SS}}V_s. \quad (7)$$

For the first- and second-stage cyclic ADCs, we assume that the values of n and $V_{\rm od}$ in the amplifier are the same. The value of m is therefore constant and is the same as the value in both the first- and second-stage cyclic ADCs. For the settling time specified, the bias current required to satisfy (7) can be written as

$$I_{SS} = m\frac{C_s}{t_{\rm st}}V_s. \quad (8)$$

The required settling time of each stage of the cyclic ADC depends on the processing bit number of each stage. A larger value of the processing bit number gives a smaller settling time and a larger current in the amplifier. The required settling time is decided by the total A/D conversion time and by the number of settlements that occur in each ADC. The total A/D conversion time is a horizontal time slice t_{1H}. A cyclic ADC needs to have two phases, i.e., an amplifier phase and a feedback phase, to generate 1 bit, as shown in Fig. 4, and each phase requires sufficient settling time. We therefore assume that the required settling time is t_{1H} divided by twice the process bit number of each cyclic ADC. The required settling times for the first- and second-stage cyclic ADCs (i.e., $t_{\rm st1}$ and $t_{\rm st2}$, respectively) are then given by

$$t_{\rm st1} = \frac{t_{1H}}{2N_1} \quad (9)$$

$$t_{\rm st2} = \frac{t_{1H}}{2(N_F-N_1)}. \quad (10)$$

From (8)–(10) and by taking into consideration the scaling factor for the sampling capacitance in the second stage, the total bias current required per column is given by

$$\begin{aligned} I_{\rm total} &= m\frac{C_s}{t_{\rm st1}}V_s + m\frac{\gamma C_s}{t_{\rm st2}}V_s \\ &= \frac{2mC_sV_s}{t_{1H}}\left\{N_1+\gamma(N_F-N_1)\right\}. \end{aligned} \quad (11)$$

For a given signal-to-noise ratio SNR, where $SNR = V_s/\overline{v_n}$, and by using (3), the total bias current can be expressed as

$$I_{\rm total} = A\frac{2mSNR^2k_BT}{t_{1H}V_s}\left\{N_1+\gamma(N_F-N_1)\right\}F(\gamma, N_1, N_F). \quad (12)$$

The optimal scaling factor γ, which minimizes the total current, can be calculated by the derivative of (12) by the scaling factor as

$$\gamma = \sqrt{\frac{2^{-2N_1}N_1\left(1-2^{-2(N_F-N_1)}\right)}{(N_F-N_1)\left(1-2^{-2N_1}\right)}}. \quad (13)$$

The total current of the two-stage cyclic ADC can be estimated from (12) and (13). Fig. 6 shows the estimated total current, normalized by the total current of N_1 equal to 12, as a function of the processed bit number in the first-stage cyclic ADC when N_F is 12. The total current of the two-stage cyclic ADC is less than that for the case where N_1 is 12, i.e., the case in which a single cyclic ADC performs 12-bit processing. When the value of N_1 is about 3, the total current is minimized. Fig. 7 shows the estimated total current of the two-stage cyclic ADC and the single cyclic ADC as a function of the total number of process bits N_F. The current from the two-stage cyclic ADC is the minimum value estimated by using (12) and (13) for each value of N_F. Whereas the total current of the single cyclic ADC increases with increasing total process bits, that of the two-stage cyclic ADC is flat. When N_F is 12, the total current of the two-stage cyclic ADC is about one-third that of the single cyclic ADC.

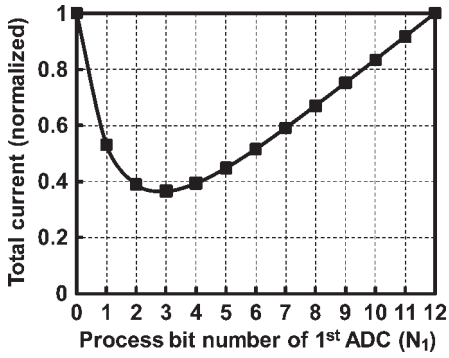

Fig. 6. Simulated total current of the two-stage cyclic ADC relative to the process bit number of the first-stage ADC.

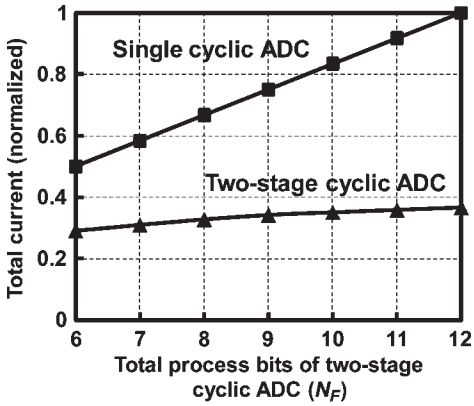

Fig. 7. Simulated total current of a two-stage cyclic ADC and of a single cyclic ADC for various values of the total process bits.

We also performed a SPICE simulation for the designed circuit to estimate its power consumption and to compare it with that of a previously reported cyclic ADC [8]. The size of capacitor C_s was decided by considering thermal noise and capacitor matching to achieve 12-bit precision. The total current is minimal when N_1 is 3 (see Fig. 6). In our 12-bit ADC design, we set N_1 to 4 to take into consideration the layout area. The simulation showed that, although the processing speed of the ADC with the two-stage architecture with 12-bit precision is 1.56 times greater than that of a conventional cyclic ADC, it consumes one-third of the power of a conventional cyclic ADC. The use of a telescopic amplifier in each stage also contributes to the low power consumption of the ADC because previously reported cyclic ADCs have used two-stage amplifiers.

IV. Implementation and Experimental Results

The image sensor was fabricated by a 0.18-μm one-polysilicon four-metal CMOS image sensor process. A micrograph of the die for the fabricated sensor is shown in Fig. 8. The size of the chip die was 26.5 mm (horizontal) by 21.6 mm (vertical). The area of the two-stage cyclic ADC was 5.6 μm $\times$ 1770 μm. In general, horizontal readout routing for these large-format high-speed image sensors is challenging. In our image sensor, the parallel LVDS driver blocks are placed near the horizontal scanners to reduce the length of wiring in the data-transfer path, thereby minimizing degradation of the horizontal

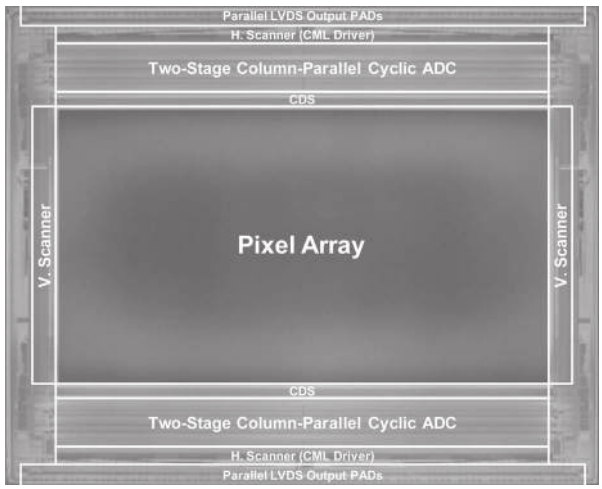

Fig. 8. Micrograph of the die for the prototype image sensor.

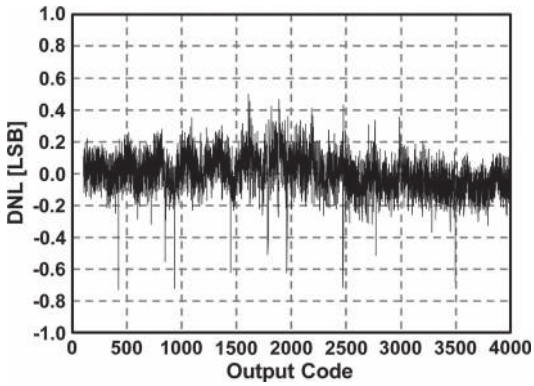

Fig. 9. Measured DNL of the two-stage cyclic ADC.

readout signals from the CML, which are obtained with a 66-MHz double-data-rate clock.

We fabricated two initial prototypes of the image sensor. The first was produced for the purposes of evaluation and had a test element group of pixels with 40 different layout patterns [11]. From an evaluation of these pixels, we selected the layout that gave a low noise level coupled with a high conversion gain, and we used this layout in our second prototype. The characteristics of the second prototype image sensor are those described in this paper.

The measured differential nonlinearity (DNL) plots of the ADC are shown in Fig. 9. The maximum DNL is in the range -0.7 to $+0.5$ least significant bits (LSBs) for the entire output range at 12-bit resolution and 120 fps, without missing codes.

We were unable to measure the integral nonlinearity (INL) because of a failure of our evaluation circuit. Our image sensor has about 8000 ADCs. A thin test input wire was connected to the inputs of all the ADCs to permit measurements of the nonlinearity. This increased the impedance of the test input line and induced an error in the test input signal. The measured INL under these conditions was +86/0 LSB, which was markedly larger than that of a previously reported cyclic ADC [8]. It will be necessary to fit a low-impedance test input line to measure the correct value of the INL.

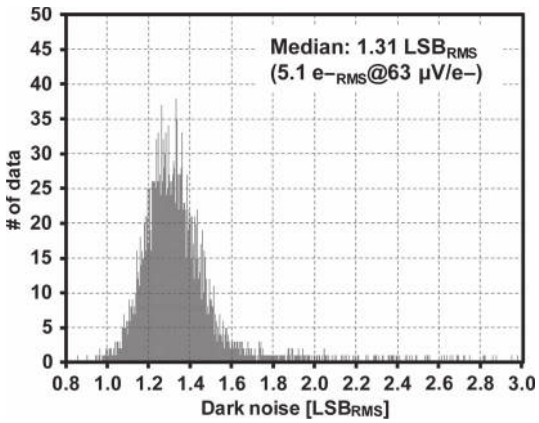

Fig. 10. Noise histogram for 10 000 pixels in darkness.

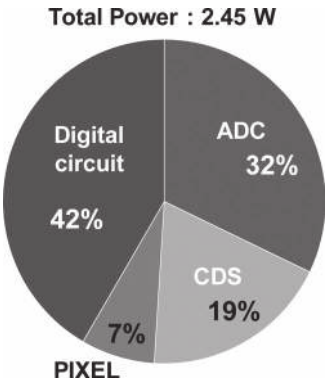

Fig. 11. Breakdown of power consumption.

The noise histogram for 10 000 pixels for the case when the analog gain was set to 1 is shown in Fig. 10. Here, 1 LSB corresponds to 244 μV with a 1-V reference at 12-bit resolution. The measurements were performed at room temperature. The median dark random noise obtained from 10 000 pixels was 1.31 $\mathrm{LSB_{rms}}$, which corresponds to 320 $\mu\mathrm{V_{rms}}$.

We designed this image sensor on the assumption that the fixed-pattern noise (FPN) will be canceled outside the image sensor. The measured amounts of vertical and pixel-level FPNs from the image sensor were 12.57 $\mathrm{LSB_{rms}}$ and 1.60 $\mathrm{LSB_{rms}}$, respectively. These FPNs are subtracted from the signal data by the FPN-reduction system that we developed. As a result, vertical and pixel-level FPN levels were reduced to 0.14 $\mathrm{LSB_{rms}}$ and 0.54 $\mathrm{LSB_{rms}}$, respectively. This type of ADC architecture can be used for digital CDS, which is effective in reducing vertical FPN (VFPN) [8]; the architecture is therefore likely to reduce VFPN in the image sensor if we adopt digital CDS. However, digital CDS requires twice the A/D conversion time; hence, we did not adopt it in this image sensor.

The total power consumption of the image sensor was 2.45 W at 120 fps for a column analog gain of unity. This includes the power consumption of the I/O pad. A breakdown of the total power consumption is shown in Fig. 11. The total power consumption of the two-stage cyclic ADC is about 0.79 W, and therefore, the power consumption of each two-stage cyclic ADC is 101 μW, which is about one-third that of a previously reported cyclic ADC [8] and agrees well with the value calculated by the simulation described in Section III. The power consumption in the digital circuitry, which includes the LVDS driver and the CML circuits, is about 40% of the total power consumption.

Fig. 12. Full-frame image captured at 120 fps.

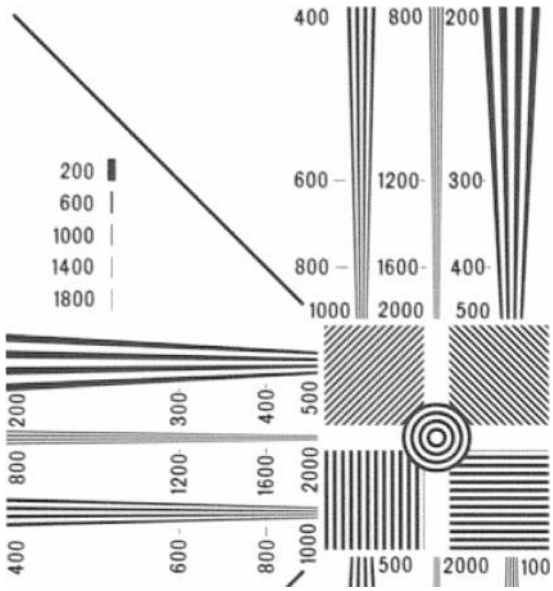

Fig. 13. Magnified image from the central portion of a resolution chart with zoom out.

A full-resolution image taken at 120 fps by the image sensor is shown in Fig. 12. The resolution characteristics of the image sensor were also measured by using a Hi-Vision resolution chart. The resolution chart was captured in one-sixteenth of the area of the full resolution, which corresponds to Hi-Vision resolution. The "1000" TV lines shown on the chart therefore correspond to an actual resolution of 4000 TV lines. Fig. 13 shows the magnified image from the central portion of the resolution chart. This demonstrates that a line spacing of 1000 TV lines (4000 TV lines by this conversion) is resolved.

Examples of images of a moving object are shown in Fig. 14. When the object was moving to the right, there was significant motion blur in the 60-fps image but little blurring in the 120-fps image. The image lag of the image sensor was below the measurement threshold at 120 fps.

The specifications and characteristics of the sensor are summarized in Table I. An RMS random temporal noise of 5.1 e^-_{rms} was achieved at a frame rate of 120 fps when the analog gain was set to 1. When the analog gain was set to 7.5, the input-referred random noise was 3.0 e^-_{rms} while a low power

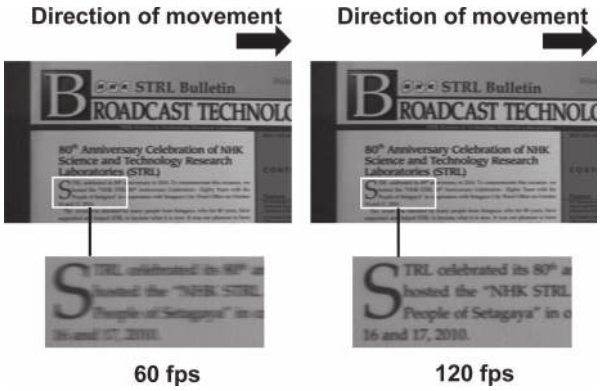

Fig. 14. Reproduced images of a moving object at two frame rates.

TABLE I
PERFORMANCE SUMMARY

Process	0.18 μm 1P4M CIS
Chip size	26.5 mm (H) × 21.6 mm (V)
Power supplies	1.8 V (Digital), 3.3 V (Analog)
Number of active pixels	7680 (H) × 4320 (V)
Number of total pixels	7808 (H) × 4336 (V)
Pixel size	2.8 μm × 2.8 μm
Pixel type	2.5-Tr two-shared pixel (Pinned PD)
Farme rate	120 fps (maximum)
Optical format	3/2 inch
ADC resolution	12 bit
ADC DNL	+0.5/-0.7 LSB
ADC noise	148.5 μV_{rms}
Conversion gain	63 μV/e-
Dynamic range	62.9 dB
Sensitivity	0.76 V/lx•s (w/o microlens)
Random noise	5.1 e^-_{rms} (Gain=1) at 120 fps
	3.0 e^-_{rms} (Gain=7.5) at 120 fps
Power consumption	2.45 W (Gain < 7.5) at 120fps
	2.67 W (Gain = 7.5) at 120fps

consumption value of 2.67 W was maintained. The data rate for each LVDS output port was 533 Mb/s, and the sensor had an aggregate data rate of 51.2 Gb/s.

Table II shows a comparison of the primary characteristics of our imager with those of some recent imagers. A figure-of-merit (FoM) of 2.0 $e^- \cdot$ nJ, where FoM $=$ (power $\times$ noise)/(number of pixels $\times$ fps), was achieved. In comparison with large-format image sensors [4], [6], the FoM of our new sensor is smaller and it is about half that of the sensor developed by Toyama *et al.* [6]. In comparison with the sensor developed by Chae *et al.* [9], the pixel rate of our sensor is 16 times faster and its FoM is comparable. Owing to the nature of the two-stage cyclic ADCs, our sensor showed a low power consumption value in conjunction with a high frame rate of 120 fps and a high resolution of 33 megapixels.

V. CONCLUSION

We have described a 33-megapixel 120-fps CMOS image sensor that incorporates a column-parallel two-stage cyclic ADC. The two-stage architecture, with appropriate bit separation, provides not only an increase in the operating speed but also a decrease in the power consumption of the cyclic ADC. A low power consumption value of 2.45 W, coupled with a very high data output of 51.2 Gb/s, was achieved by the suitable design of the ADC architecture and by the use of 96 parallel LVDS output ports. Images recorded at 120 fps have sufficient resolution for use in a 4000-line television, and the quality of images of moving objects is superior to those recorded at 60 fps. The image sensor is therefore suitable for use in an ultrahigh-definition color imaging system and for delivering an enhanced visual experience in SHV.

TABLE II
COMPARISONS WITH RECENT HIGH-RESOLUTION IMAGE SENSORS

Ref.	[4]	[6]	[9]	[8]	[13]	This work
Resolution [bits]	12	12	12.5	13	12	12
Technique used	SAR	SS	ΔΣ	Cyclic	2-Stage cyclic	2-Stage cyclic
Frame rate [fps]	60	120	120	360	1700	120
# of V. pixels	2168	2160	1212	428	1024	4320
# of H. pixels	4122	8192	1696	640	1280	7680
Noise [e-]	2.8	2.75	2.4	4.5	7	3.0
Colum Amp. gain	8	11.2	1	1	2	7.5
Conv. gain [μV/e-]	45	48	80	61	40	63
Power [mW]	1085	3000	180	297	908	2670
FoM [e-•nJ]	5.7	3.9	1.8	13.6	2.9	2.0

REFERENCES

[1] M. Sugawara, M. Kanazawa, K. Mitani, H. Shimamoto, T. Yamashita, and F. Okano, "Ultrahigh-definition video system with 4000 scanning lines," *SMPTE Motion Imag. J.*, vol. 112, no. 10/11, pp. 339–346, Oct./Nov. 2003.

[2] T. Yamashita, K. Masaoka, K. Ohmura, M. Emoto, Y. Nishida, and M. Sugawara, "Super Hi-Vision video parameters for next-generation television," presented at the SMPTE—Annu. Technical Conf. Exhibition, Hollywood, CA, Oct. 25–27, 2011.

[3] I. Takayanagi, M. Shirakawa, K. Mitani, M. Sugawara, S. Iversen, J. Moholt, J. Nakamura, and E. R. Fossum, "A 1-1/4 inch 8.3 M-pixel digital output CMOS APS for UDTV application," in *Proc. ISSCC Dig. Tech. Papers*, Feb. 2003, pp. 216–217.

[4] S. Matsuo, T. Bales, M. Shoda, S. Osawa, B. Almond, Y. Mo, J. Gleason, T. Chow, and I. Takayanagi, "A very low column FPN and row temporal noise 8.9 M-pixel, 60 fps CMOS image sensor with 14 bit column parallel SA-ADC," in *Proc. IEEE Symp. VLSI Circuits, Dig. Tech. Papers*, 2008, pp. 138–139.

[5] S. Huang, T. Yamashita, Y. Wang, K. L. Ong, K. Mitani, R. Funatsu, H. Shimamoto, L. P. Ang, L. Truong, and B. Mansoorian, "A 2.5 inch, 33 Mpixel, 60 fps CMOS image sensor for UHDTV application," in *Proc. Int. Image Sens. Workshop*, Jun. 2009, pp. 308–311.

[6] T. Toyama, K. Mishina, H. Tsuchiya, T. Ichikawa, H. Iwaki, Y. Gendai, H. Murakami, K. Takamiya, H. Shiroshita, Y. Muramatsu, and T. Furusawa, "A 17.7 Mpixel 120 fps CMOS image sensor with 34.8 Gb/s readout," in *Proc. ISSCC Dig. Tech. Papers*, Feb. 2011, pp. 420–422.

[7] M. Furuta, Y. Nishikawa, T. Inoue, and S. Kawahito, "A high-speed, high-sensitivity digital CMOS image sensor with a global shutter and 12-bit column-parallel cyclic A/D converters," *IEEE J. Solid-State Circuits*, vol. 42, no. 4, pp. 766–774, Apr. 2007.

[8] J. H. Park, S. Aoyama, T. Watanabe, K. Isobe, and S. Kawahito, "A high-speed low noise CMOS image sensor with 13-b column-parallel single-ended cyclic ADCs," *IEEE Trans. Electron. Devices*, vol. 56, no. 11, pp. 2414–2422, Nov. 2009.

[9] Y. C. Chae, J. Cheon, S. Lim, M. Kwon, K. Yoo, W. Jung, D.-H. Lee, S. Ham, and G. Han, "A 2.1 M pixels, 120 frame/s CMOS image sensor with column-parallel $\Delta\Sigma$ ADC architecture," *IEEE J. Solid-State Circuits*, vol. 46, no. 1, pp. 236–247, Jan. 2011.

[10] K. Kitamura, T. Watabe, Y. Sadanaga, T. Sawamoto, T. Kosugi, T. Akahori, T. Iida, K. Isobe, T. Watanabe, H. Shimamoto, H. Ohtake, S. Aoyama, S. Kawahito, and N. Egami, "A 33 Mpixel, 120 fps CMOS image sensor for UDTV application with two-stage column-parallel cyclic ADCs," in *Proc. Int. Image Sens. Workshop*, Jun. 2011, pp. 343–346.

[11] T. Watabe, K. Kitamura, T. Sawamoto, T. Kosugi, T. Akahori, T. Iida, K. Isobe, T. Watanabe, H. Shimamoto, H. Ohtake, S. Aoyama, S. Kawahito, and N. Egami, "A 33 Mpixel 120 fps CMOS image sensor using 12b column-parallel pipelined cyclic ADCs," in *Proc. ISSCC Dig. Tech. Papers*, Feb. 2012, pp. 388–390.

[12] S. H. Lewis, H. S. Fetterman, G. F. Gross, Jr., R. Ramachandran, and T. R. Viswanathan, "A 10-b 20-Msample/s analog-to-digital converter," *IEEE J. Solid-State Circuits*, vol. 27, no. 3, pp. 351–358, Mar. 1992.

[13] J. H. Park, S. Aoyama, T. Watanabe, T. Kosugi, Z. Liu, T. Akahori, M. Sasaki, K. Isobe, Y. Kaneko, K. Muramatsu, T. Iida, and S. Kawahito, "A high-speed low-noise CIS with 12b 2-stage pipelined cyclic ADCs," in *Proc. Int. Image Sens. Workshop*, Jun. 2011, pp. 339–342.

Authors' photographs and biographies not available at the time of publication.