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# A 4-Element Phased-Array System with Simultaneous Spatial- and Frequency-Domain Filtering at the Antenna Inputs

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*Abstract* **—** To reject strong interference in excess of 0 dBm, a 4-element LO-phase shifting phased-array receiver with 8-phase passive mixers terminated by baseband capacitors is presented. The passive mixers up-convert both the spatial and frequency domain filtering from baseband to RF, hence realizing blocker suppression directly at the antenna inputs. A comprehensive mathematical model provides a set of closed-form equations describing the spatial and frequency domain filtering including imperfections. A prototype is realized in 28 nm CMOS. It exploits 3$^{rd}$ harmonic reception to achieve a wide RF-frequency range from 0.6-4.5 GHz at 34-119 mW power dissipation, while also providing impedance matching. Out of the band/beam, a 1 dB-compression point as high as +12/+10 dBm has been measured. The 1-element NF over the RF-frequency range is 4-6.3 dB, while in-beam/band IIP3 values of 0..+2.6 dBm are measured. This proposed technique can be instrumental to make RF receivers more robust for interference, while still being flexibly tunable in frequency.

*Index Terms* — Phased-array receiver, spatial filtering, N-path filter, tunable filter, high linearity, high compression point, linear periodically time variant circuit, LPTV, commutated capacitors, frequency translated filter, high-Q, CMOS, cognitive radio, software-defined radio, coexistence, blocking, blocker suppression, Passive Mixer.

## I. INTRODUCTION

The abundance of wireless communication devices in the low GHz frequency bands results in potentially strong mutual interference between devices, often referred to as "blocking". Blocking signals can exist both in-band and out-of-band, where especially the requirements

1

on the latter tend to be strong. The GSM and Bluetooth standards for instance specify 0 dBm out-of-band blockers. Note that 0 dBm received power in a 50 $\Omega$ impedance corresponds to a voltage swing of 0.6 $V_{pp}$, which is difficult to handle by CMOS circuits with a supply voltage of around 1Volt! When mobile devices are in close proximity, blockers even stronger than 0 dBm may occur, not only out-of-band but also in-band. Such in-band interference scenarios are also an important bottleneck for future dynamic spectrum access via a cognitive radio, where unused spectrum may exist in close spectral proximity to strong signals[1]. In order to reduce the out-of-band blockers, RF bandpass pre-filtering is commonly used. However, such frequency-domain filtering does not help for in-band or near in-band blocking. In contrast, *spatial filtering* through multiple antennas in a beamforming phased-array can reduce blockers, both out-of-band and in-band. In a phased-array, in-beam phase shifted signals from multiple antennas add constructively, while out-of-beam signals add destructively.

To align in-beam phase-shifted signals, different approaches have been presented in literature. Among them, passive RF phase-shifting in the signal path is attractive from a linearity point of view. However, passive RF components tend to take a large die area and their loss results in signal attenuation and noise figure degradation [1, 2]. Beamforming based on LO-phase shifting can be more compact, but usually still exploits inductors [3]. In the low GHz frequency range, inductorless LO-phase shifting combined with vector modulation gained interest in recent years [4-7]. Digital techniques leveraging Moore's law are exploited to realize programmable phase shifts. Array size considerations often dictate a limited number of antenna elements, so that all phase shifted signals can be summed, usually after amplification and sometimes after frequency downconversion. Thus interfering signals are amplified before they are canceled at the summation point. This requires a high dynamic range for the blocks preceding the summing node to handle full strength blocking signals. To improve blocking behavior, a fully passive switched-capacitor vector modulator was presented in [7], achieving a compression point $P_{1dB}$=+2 dBm, but at a high noise penalty (NF=18 dB).

In this paper we discuss a mixer-first phased-array receiver that merges beamforming and N-path filtering techniques in one circuit. In essence it exploits LO-phase shifting to realize simultaneous frequency- and spatial-domain filtering. We will show that this renders superior blocker handling, at the cost of some flexibility in control of the beam pattern. In [8] we

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[1] Actually the difference between in-band and out-of-band is blurred for cognitive radio scenarios exploiting white spaces (there is no clear dedicated band but just used/unused spectrum).

presented a 4-element phased-array receiver in 65 nm CMOS technology which achieves up to +10 dBm out-of-band/beam[2] compression point and 3-6 dB single-element noise figure in a frequency range of 0.6-3.6GHz. This paper elaborates on the phased-array system and includes a comprehensive mathematical analysis of the spatial- and frequency-domain filtering at the antenna inputs and also at the baseband. Moreover measurement results of a new prototype IC realized in 28 nm CMOS will be provided. The new prototype demonstrates similar performance compared to 65 nm version at wider frequency range and lower power consumption demonstrating the scalability of the design. Finally the theoretical analysis results and their implications are verified by Spectre-RF simulations and measurements.

In section II a brief summary of a phased-array system is presented. The mixer-first phased-array system is discussed intuitively in section III. The mathematical analysis of the proposed system is presented in section IV. The implemented prototype will be discussed in section V. Section VI discusses some implications of the analysis on the implemented architecture and finally the measurement results and comparison are presented in section VII, while conclusions are drawn in VIII.

## II.    MULTI-ANTENNA PHASED-ARRAY SYSTEM

A general block diagram of an M-element linear phased-array antenna system is shown in Fig. 1. We analyze it briefly here as we need to introduce a mathematical notation. The desired planar wave signal (Sde) is incident on the antennas at an angle θ to broadside, while an undesired signal (Sud) also hits the receiver antennas with a different spatial angle from the desired signal. Depending on the spatial angle θ, these signals experience different travel times to reach different antennas. This causes a time delay on the signals reaching two neighbor antennas which can be calculated as [9]:

$$\Delta \tau = d.\sin(\theta)/c,$$

(1)

where "c" is the speed of light and "d" is the physical distance between antennas. The time delay in the desired signals should be compensated via true time delay blocks or phase shifters in the receiver before the summation point (see Fig. 1). Assuming a narrow band system, the delay time in (1) can be approximated by a phase shift. As the mth antenna (m=1, 2 **,...**) signal experiences a delay of $(m-1)\Delta \tau$, the received signal after phase shifting can be written as:

$$s_{in,m}(t) \approx \left| A(t) \right| \cos(\omega_c t - \omega_c (m-1)\Delta \tau + \varphi(t)).$$

(2)

---

[2] Two blocker scenarios were considered: (1) In-beam and out-of-band (2) In-band and out-of-beam.

Hence, a phase shift of $\omega_c(m-1)\Delta\tau$ is needed, which can be realized as a phase-shift in the LO path of a frequency down conversion mixer. The phase shifter in Fig. 1 is then replaced by a mixer and the summation is realized in the baseband. If the time delay is compensated for a certain desired angle of reception (index "de") the beams add-up constructively in-beam, while for undesired (index "ud") out-of-beam signals (partially) destructive addition occurs. This provides spatial filtering [10]. Phase shifting instead of true time delay causes so called beam squinting (i.e. frequency dependent beam direction), but for narrow-band applications this effect can be neglected [11]. Apart from spatial filtering a phased-array system has a benefit of signal to noise ratio (SNR) improvement, compared to a single antenna receiver. In fact for every doubling of the number of receivers and antenna aperture, the sensitivity is improved by 3 dB theoretically at the cost of doubled total receiver power consumption and doubled antenna aperture. Note that this assumes uncorrelated noise in different receive paths, so that noise signals add up in power while the desired signals are correlated and add up in voltage gaining a factor of two in SNR, i.e. 3 dB improvement. We will revisit this assumption later in this paper.

### III. MIXER-FIRST PHASED-ARRAY ARCHITECTURE

#### A. Spatial- and Frequency-Domain Filtering

We will now first introduce the concept of simultaneous spatial- and frequency-domain filtering at the antenna inputs in an intuitive way. A simplified block diagram of a mixer-first 4-element phased-array receiver is illustrated in Fig. 2. The received signal at the antenna inputs is directly downconverted on the baseband capacitors via multiphase passive mixers, driven by non-overlapping clocks.

The phase shift of the RF signals is compensated by LO phase shifting in the mixers. If the RC time-constant composed of the real impedance of the antennas and the baseband capacitors is very large compared to the on-time of the mixer switches, the downconverted signals for the desired incident angle are summed on the baseband capacitors constructively.

For out-of-beam signals the summation would be partly or fully destructive, thus resulting a spatial filtering on the baseband capacitors (see beam pattern at baseband in Fig. 2). This spatial filtering is up-converted to the RF node via passive mixers, so that it occurs directly at the antenna inputs. Moreover RC low-pass filtering also occurs on the capacitors, which is also up-converted, rendering high-Q N-path frequency-domain filtering at RF [12-20].

In order to understand the spatial filtering intuitively a 4-element phased-array system with 8-phase passive mixers is depicted in Fig. 3 for two illustrative different incident angles. The

passive mixers are driven by 8 non-overlapping 1/8 duty-cycle clocks ($\varphi_1$-$\varphi_8$). For simplicity we assumed in the architecture of Fig. 3 all switches connected to the same capacitors are driven with the same clock phases thus realizing zero angle reception. By selecting other clock phases for the mixer switches, beam steering can be achieved for 8 discrete possible angles. In Fig. 3 the desired signal ($S_{de}$) with the frequency of the switching frequency ($f_s$) is impinging the receiver antennas with a zero spatial angle ($\theta=0°$) while the undesired signal ($S_{ud}$) is arriving at the antennas with $\theta=90°$. The resulting time domain signals are shown in Fig. 3b for the two incident angles. Note that for the desired signal there is no time delay among received signals while for the incident angle of $\theta=90°$, assuming d= $\lambda_c/2$ the phase shift can be calculated from (1), (2) as:

$$\Delta\varphi_m = -\omega_c(m-1)\Delta\tau = -(m-1)\pi\sin(\theta). \tag{3}$$

As a result for $\theta=90°$, the phase shift for the m$^{\text{th}}$ antenna will be $\Delta\varphi_m = -(m-1)\times180°$ (m=1, 2 ,3 ,4). This phase shift is applied to the undesired signal ($S_{ud}$) in Fig. 3b. In Fig. 3b, the parts of the signals which are "seen" by the capacitor $C_1$ are shown as shaded areas. Please note that for the desired angle of reception capacitor $C_1$ sees the same parts of the signal periodically which will be integrated on the capacitor. However; for the undesired signal, capacitor $C_1$ is exposed to the anti-phase signals successively which will be canceled out if the RC time-constant is large enough. This illustrates spatial filtering on the baseband capacitors. As each passive mixer periodically acts as a transparent switch, this spatial filtering is also "seen" at the antenna node before the switches. In fact for the undesired direction of the incident wave, the receiver input roughly acts as a short circuit to each antenna, reflecting the undesired signal. Note that this would not be the case for an active mixer, which ideally acts uni-lateral from input to output and has reverse isolation.

Considering a single antenna element in Fig. 3, N-path RC frequency-domain filtering also occurs on the baseband capacitors, which is up-converted to the switching frequency and its harmonics [14, 16, 18, 21]. The periodically time-variant nature of N-path filters introduces frequency shifts by multiples of the clock frequency. Thus the spatial- and frequency-domain filtering happens not only around the fundamental harmonic of the clock, but also around its harmonics. In this work we will aim at 3$^{\text{rd}}$ harmonic reception, as it allows for an increase in frequency range, whereas the power efficiency is also better compared to fundamental reception.

### B. Spatial Angular Resolution

As mentioned in the previous section the phases of the LO controls beam direction. Thus the spatial angle resolution is defined by the number of different mixer clock phases. In our design we use 8-phase passive mixers so that the possible uniformly spaced electrical phase shifts are $\Delta\varphi = 0°, \pm 45°, \pm 90°, \pm 135°, 180°$. By applying (3), we can find the following corresponding spatial angles: $\theta = 0°, \pm 14.5°, \pm 30°, \pm 48.6°, 90°$. Non-uniform phase shifting to increase the spatial angular resolution will be discussed in section VII with an illustrative example.

## IV.    ANALYSIS

In this section we will provide a set of closed form equations to describe the spatial- and frequency domain filtering of the mixer-first phased-array system discussed in previous section. The spatial- and frequency domain filtering both on the baseband capacitors and at the antenna terminal will be illustrated. The network of Fig. 3 is a switched-RC Linear Periodically Time Variant (LPTV) network. RS mimics the real part of the antenna impedance (50 Ω). With the assumption of non-overlapping clocks the analysis of the circuit in Fig. 3 can be performed by a state-space analysis carried out on a single state switched-RC network as shown in Fig. 4a, where only one path of every mixer is shown. The transfer for the other capacitors can be found as phase-shifted versions of the analyzed one. The timing diagram which is applied for the state-space analysis is shown in Fig. 4b. The time interval of $nT_S < t < (n+1)T_S$ is divided into N portions, where N is the number of the paths in the passive mixer (in our case N=8). During each time interval which can be identified by "k" as $nT_S + \sigma_k < t < nT_S + \sigma_{k+1}$, with $\sigma_0 = 0$, only one of N switches in the passive mixers is conducting. From the LPTV network analysis, extensively discussed in [16, 22], the output spectrum on the baseband capacitors in state "k" can be shown have a general form:

$$V_{BB,k}(f,\theta) = \sum_{n=-\infty}^{\infty} H_{n,k}(f,\theta)V_{S1}(f - nf_S). \tag{4}$$

In (4) frequency shifted versions of the input spectrum are summed after weighting them by a frequency and incident-angle dependent factor $H_{n,k}(f,\theta)$. Factor $H_{n,k}(f,\theta)$ is defined by a periodic integration mode, during which the switches are conducting and the input signals are integrated on the capacitors, followed by a hold mode in which the switches are open and the voltage on the capacitor is kept unchanged. Please note that depending on different phase settings in the phased-array system of Fig. 3, at each period (Ts) of the switching frequency there might be more than one track or hold mode on different states

illustrated in Fig. 4b. These two modes do not have overlap in the time domain and as a result the spectrum generated by each one can be derived separately and then added up. The state equation for the baseband capacitor can be written as $\dot{v}_{BB,k}(t) = A_k v_{BB,k} + B_k v_S(t)$ where Ak and Bk in general form are (m×m) matrixes (m is the number of states, in our case m=1). The transfer function $H_{n,k}(f,\theta)$ for the baseband capacitor which is connected to the input voltage of $V_S(f)$ at time interval "k", can be found similarly to [16, 22] as:

$$H_{n,k}(f,\theta) = \left(j2\pi fI - A_k\right)^{-1} \times \left( \begin{array}{l} B_k \dfrac{1-e^{-j2\pi nf_s\tau_k}}{j2\pi n}e^{-j2\pi nf_s\sigma_k} + f_sG_k(f-nf_s,\theta)e^{-j2\pi nf_s\sigma_k} \\ - f_sG_{k+1}(f-nf_s,\theta)e^{-j2\pi nf_s\sigma_{k+1}} \end{array} \right), \qquad (5)$$

where the first term in the brackets is presenting the spectrum generated by the input signal when connected to the capacitor, while $G_k(f,\theta)$ and $G_{k+1}(f,\theta)$ in the second and third terms inside the brackets are illustrating the contribution of the initial and end conditions on the capacitors in the output spectrum, which are added and subtracted at the beginning and end time of each time interval. In (5) "I" is a unit matrix with the same dimension as $A_k$. The transfer function of $H_{n,k}(f,\theta)$ should encompass both the integration and hold modes.

Since the analysis procedure to derive $G_k(f,\theta)$ in (5) for different phase settings is very much similar to the approach in [16, 22], to avoid tedious mathematical derivations we will just mention the assumptions and provide the final results of the mathematical modeling. The LPTV analysis can be carried out for all "N" possible LO phase settings in the phased-array system; however, here the analysis will cover two cases: 0 degrees and -30 degrees reception angle of the main beam. The analysis for other angles can be derived similarly. All of the results in the following sections have been cross-checked with simulation results from Spectre-RF with ideal switches (abrupt switching with zero "ON" resistance and infinite "OFF" resistance). Since the simulation results fall exactly on top of the analyzed ones we have omitted the simulation results. However, in section VII the analysis results will be compared with transistor level simulation and measurement results.

### A. Baseband Analysis at Zero Incident Angle
In order to receive the zero incident angle, all switches in Fig. 4a should be in phase. As a result the signal sources are simply in parallel and superposition can be applied. The circuit of Fig. 4a can be simplified to the one in Fig. 4c and it can be analyzed with the LPTV approach presented in [16, 22], with two changes: 1) $R_S$ is 4 times lower (more bandwidth); 2) the

source signal contains a weighted sum of 4 antenna signals components with time shifts $(m-1)\Delta\tau$. The state-space equations for integration and hold modes are as following: $\dot{v}_{BB,k}(t) = A_k v_{BB,k} + B_k v_s(t)$ in which for the integration mode $A_{k,i} = -1/(RC)$, $B_{k,i} = 1/(RC)$, $R = R_S/4$ (index "i" stands for integration). For the hold mode the differential equation becomes as: $\dot{v}_{BB,k,h}(t) = 0$ and $A_{k,h} = B_{k,h} = 0$. For the circuit in Fig. 4a the transfer function in (5) can be derived as: $H_{n,k}(f,\theta) = H_{n,k,i}(f,\theta) + H_{n,k,h}(f,\theta)$.

$$H_{n,k,i}(f,\theta) = \frac{e^{-j2\pi n f_s \sigma_k}}{1+j\dfrac{f}{f_{rc}}} \times \Psi \times \left( \frac{1-e^{-j2\pi n f_s \tau_k}}{j2\pi n} + \frac{1-e^{j2\pi((f-nf_s)(T_s-\tau_k)-nf_s\tau_k)}}{2\pi\dfrac{f_{rc}}{f_s}} G_k(f) \right),$$

$$H_{n,k,h}(f,\theta) = e^{-j2\pi n f_s \sigma_k} \times \Psi \times \left( \frac{1-e^{-j2\pi f(T_s-\tau_k)}}{j2\pi\dfrac{f}{f_s}} \times e^{j2\pi((f-nf_s)(T_s-\tau_k)-nf_s\tau_k)} G_k(f) \right),$$

$$\Psi = 0.25 \times \left( 1 + e^{-j2\pi(f-nf_s)\Delta\tau} + e^{-j2\pi(f-nf_s)2\Delta\tau} + e^{-j2\pi(f-nf_s)3\Delta\tau} \right),$$

$$G_k(f) = \frac{e^{j2\pi(f-nf_s)\tau_k} - e^{-2\pi f_{rc}\tau_k}}{e^{j2\pi\dfrac{f-nf_s}{f_s}} - e^{-2\pi f_{rc}\tau_k}} \times \frac{1}{1+j\dfrac{f-nf_s}{f_{rc}}}, \tag{6}$$

where $f_{rc} = (2\pi RC)^{-1}$ is defined as the 3 dB bandwidth of a single RC low-pass filter with resistor $R = R_S/4$ and capacitor C (see Fig. 4c). In (6) "$\Delta\tau$" is the time delay at different antennas defined in (1). "$\Psi$" presents the summation of the phase shifted input signals at the antenna inputs. $D_k$ is the duty-cycle of the clock driving the switches and ideally is 1/8 for the 8 phase mixer. Fig. 5 shows a 3D plot of $H_{-3,k}(f,\theta)$ which is presenting the 3rd harmonic reception transfer, aiming at zero angle reception. The plot clearly demonstrates both the spatial- and frequency-domain filtering on the baseband capacitors around a maximum transfer at 0 Hz and 0 degree. In Fig. 6 the cross section of the 3D plot of Fig. 5 for θ=0° is shown which in fact is the typical RC frequency N-path filtering of the switched-RC passive mixer transfer also discussed in [22]. To demonstrate the filtering and beamforming on the baseband capacitors, Fig. 7 provides cross sections of Fig 5 for different offset frequencies compared to $3f_s$. Fig. 7a does this for negative frequency offset down to $-f_s$ and in Fig. 7b for positive offsets up to $+f_s$ For easy reading of achieved rejections, the -2.1 dB maximum transfer (Fig. 6) is normalized to 0 dB in Fig. 7.

As expected from beamforming theory [9] positive offset frequencies (RF input frequencies higher than the 3$^{rd}$ harmonic) correspond to narrower beams while negative offset frequencies (RF input frequencies lower than the 3$^{rd}$ harmonic) correspond to wider beams. The attenuation at offset frequencies presents the frequency filtering which is also shown in Fig. 6.

### B. Analysis at the Antenna Inputs for Zero Incident Angle

In this section the mathematical derivations for the spectral and spatial transfer to the RF node at the antenna inputs are presented for the zero degree of physical angle reception. The RF node before switches in Fig. 4 is connected to the baseband capacitors periodically. Since there is no overlap nor gap between ideal switching intervals, the frequency spectrum at the RF node can now be derived by simply summing the spectrum contributions of all capacitors *during their respective integration modes* (only then a capacitor is connected to the RF node). As a result the integration mode equations derived for the voltage on the baseband capacitors in (6) can be applied:

$$V_{RF}(f) = \sum_{n=-\infty}^{\infty} H_{n,RF}(f,\theta)V_{S1}(f-nf_S),$$

$$H_{n,RF}(f,\theta) = \sum_{k=0}^{N-1} H_{n,k,i}(f,\theta), \tag{7}$$

where $H_{n,k,i}(f,\theta)$ is derived in (6). $H_{0,RF}(f,\theta)$ is defining the main transfer at the antenna inputs which is shown in Fig. 8. The spatial- and frequency-domain filtering is illustrated around the 3$^{rd}$ harmonic of the switching frequency which is desired in our case and also around other (undesired) harmonics as well. The cross section of the 3D plot in Fig. 8 for $\theta=0°$ is shown in Fig. 9 which is consistent with the N-path frequency domain filtering property [16].

### C. Baseband Analysis for θ=-30° of Incident Angle

Analysis of the received angle other than zero degree, requires applying a phase shift in the LO path for different antennas. As a result the switches which are connected to the same baseband capacitor will be driven with phase shifted clock signals. This is in contrast with the zero degree reception angle in which all of the switches connected to the same capacitor were in phase. Please note that 90° of electrical phase shift in the LO path will result in 270° of phase shift of the antenna signal (3$^{rd}$ harmonic reception) and according to (3) this corresponds to the spatial angle of θ=-30°. As it is shown in Fig. 10 the incident planar wave with a spatial angle of θ=-30° at first is impinging the 4$^{th}$ antenna and delayed versions of it

will hit the other antennas. Fig. 10 also illustrates the clocking diagram to compensate the phase shift in the LO path. Multi-phase clocks with 90° phase shifts are driving 4 switches that are connecting 4 antennas to the same capacitor. The signal which has the maximum time delay in the spatial domain, experiences minimum phase shift in the electrical domain. The LPTV analysis can be carried out again for this case to find the parameters in (5). The initial and end transfer functions $G(f)$ in (6) for each time interval can be found as follows:

$$
G_0 = \frac{L}{e^{\left(j2\pi\frac{f-nf_s}{f_s}\right)} - e^{\left(-8\pi D\frac{f_{rc}}{f_s}\right)}} \left\{ e^{\left(-6\pi D\frac{f_{rc}}{f_s} + j2\pi(f-nf_s)(3\Delta\tau)\right)} + \right.
$$
$$
\left. e^{\left(-4\pi D\frac{f_{rc}}{f_s} + j2\pi(f-nf_s)(\sigma_2+2\Delta\tau)\right)} + e^{\left(-2\pi D\frac{f_{rc}}{f_s} + j2\pi(f-nf_s)(\sigma_4+\Delta\tau)\right)} + e^{j2\pi(f-nf_s)(\sigma_6)} \right\},
$$

$$
G_1 = e^{\left(-2\pi D\frac{f_{rc}}{f_s}\right)}.G_0 + L.e^{\left(j2\pi(f-nf_s)(3\Delta\tau)\right)},
$$

$$
G_3 = e^{\left(-2\pi D\frac{f_{rc}}{f_s}\right)}.G_1 + L.e^{\left(j2\pi(f-nf_s)(\sigma_2+2\Delta\tau)\right)},
$$

$$
G_5 = e^{\left(-2\pi D\frac{f_{rc}}{f_s}\right)}.G_3 + L.e^{\left(j2\pi(f-nf_s)(\sigma_4+\Delta\tau)\right)},
$$

$$
G_7 = e^{\left(-2\pi D\frac{f_{rc}}{f_s}\right)}.G_5 + L.e^{\left(j2\pi(f-nf_s)(\sigma_6)\right)},
$$

$$
L = \frac{e^{\left(j2\pi D\frac{(f-nf_s)}{f_s}\right)} - e^{\left(-2\pi D\frac{f_{rc}}{f_s}\right)}}{1 + j\frac{f-nf_s}{f_{rc}}}. \tag{8}
$$

For the hold mode the initial transfer functions will be the end condition of the previous state. Thus: $G_2 = G_1, G_4 = G_3, G_6 = G_5, G_8 = G_7$. With the application of (8) and (5) the voltage transfer on the baseband capacitors for the incident angle of θ=-30° can be found. The 3D plot of the result is illustrated in Fig. 11 in which the reception at θ=-30° for the 3rd side band and the spatial- and frequency-domain filtering is visible.

### D. Analysis at the Antenna Inputs for θ=-30° of Incident Angle

Similar to the analysis in section IV-B superposition of the frequency spectrum on the baseband capacitors in the integration mode as in (7) was done for θ=-30°. The 3D plot for this case is shown in Fig. 12. Again, as expected, the main beam around the 3rd harmonic of the switching frequency experiences both frequency- and spatial-domain filtering. The cross section of this 3D plot at θ=-30° is shown in Fig. 13.

Comparing to Fig. 9 the harmonics other than the 3rd harmonic experience extra attenuation. The amount of harmonic suppression will affect the folding back from undesired

harmonics with the same amount. To evaluate the amount of suppression, contour plots derived for the 3D plot of Fig. 12 are shown in Fig. 14. Beam squinting at the offset frequencies from the 3$^{rd}$ harmonic is also observed.

## V. IMPLEMENTED ARCHITECTURE

The complete block diagram of the implemented prototype in 28 nm CMOS technology is shown in Fig. 15 (see chip micrograph in Fig. 16). The phased-array system is composed of 4-element mixer-first architecture with 8-phase passive mixers. The mixer switches are realized with NMOS transistors (64 um/28 nm) driven by 1/8 duty-cycle non-overlapped clock signals. As discussed earlier the aim is to receive the RF signals around the 3rd harmonic of the switching frequency of the passive mixers. The 8 multiphase baseband voltage signals on the capacitors are converted to the current signals via V-to-I converters (Gm blocks). The V-to-I converters are realized with self-biased inverters designed to tolerate high input swings and have a capacitive input impedance. The unit gm block in Fig. 15 has the size of PMOS:135 um/0.9 um, NMOS:58 um/0.9 um. By proper weighting of the Gm blocks the first harmonic is rejected and the third one is received. The procedure of the baseband vector weighting and summation for four phases (BB$_1$, BB$_4$, BB$_6$, BB$_7$) is illustrated in Fig. 17 (note that a delay of 1/8 clock-period renders a phase shift of α at $f_s$ , but 3α at $3f_s$ ). In a similar way, the baseband phase summation is repeated for all other phases to generate differential IQ current signals at two Trans-Impedance Amplifiers (TIA's). The TIA's are off-chip for experimental freedom to make sure we characterize the RF front-end limitations. The vector summation at the output of the G$_m$ blocks is in the current domain. As the TIAs provide a virtual ground, the output voltage swing of the G$_m$ blocks is limited, which improves linearity.

The clock divider architecture is illustrated in Fig. 18 in which a 4-stage Johnson Counter is applied. Since we have applied single-ended mixers, the flicker noise of the clock divider core might easily leak to the baseband outputs. In order to avoid this we have applied a re-clocking scheme. The output phases of the divider are combined by 4-input NAND gates (two pairs of complementary inputs) to generate ¼ duty-cycle clocks enable signals. Depending on the output, either master clock CB or CA do the re-clocking, generating a 1/8 duty-cycle at the output (see Fig. 18). In the clock divider core, the Johnson divider and the phase combining part are now allowed to have high noise. Only the re-clocking path at the output of transmission gates requires clean clock edges of the master clock. The phase selector in Fig. 15 with a digital control unit which is controlled externally via a serial bus provides full

programmability of clock phases driving the mixer switches. This is required to rotate the beam to different angles.

## VI. ANALYSIS IMPLICATIONS

In this section the analysis results in section IV are applied for the architecture described in section V, to discuss the conversion-gain, input power matching and noise behavior of the receiver architecture illustrated in Fig. 15. As we assumed in the analysis section for simplicity purposes the switches are assumed to be ideal (zero "ON" resistance and infinite "OFF" resistance).

### A. Conversion Gain

The mixer conversion gain on the baseband capacitors for the $3^{rd}$ harmonic reception in a single-element can be found from $H_{n,k}(f,\theta)$ defined in the general form in (4). $H_{n,k}(f,\theta)$ is derived for the desired angle of $\theta=0°$ in (6). Substituting $n=\pm3$, $\theta=0°$, f=0 for the 3rd harmonic reception, we find mixer conversion-gain as: $CG_{M3} = H_{n=\pm3,k}(f=0,\theta=0°) \approx -2.1\,dB$ or 0.78 V/V in linear scale which is also shown in Fig. 6. This is compared to the first harmonic reception which again can be found from (6) as $CG_{M1} = H_{n=\pm1,k}(f=0,\theta=0°) \approx -0.2dB$. As we will see in section VI-C this difference in the conversion gain of the first and the 3rd harmonic reception translates to about 2 dB degradation in the noise figure for 3rd harmonic reception compared to the $1^{st}$ harmonic.

In order to find the total conversion-gain to the I/Q output in Fig. 15, considering the phase diagram in Fig. 17, we find the differential output voltage transfer $H_{n,I}(f,\theta)$ for the I output as:

$$H_{n,I}(f,\theta) = 2Z_F g_m \left\{ (1+\sqrt{2})\left(H_{n,1}(f,\theta)+H_{n,4}(f,\theta)\right)+\left(H_{n,6}(f,\theta)+H_{n,7}(f,\theta)\right) \right\}, \qquad (9)$$

where $H_{n,k}(f,\theta)$ for k=1,4,6,7 is defined in (4). As an example for zero angle reception, the receiver conversion-gain for $3^{rd}$ harmonic reception (voltage transfer from TIA-output I to the single-ended input) is found as:

$$CG_{R3} = \frac{V_{out,I}}{V_s} = H_{n=\pm3,I}(f=0,\theta=0°) \approx 8.2 \times Z_F g_m. \qquad (10)$$

Please note that, in case of receiving the frequency band around the first harmonic of the switching frequency instead of the $3^{rd}$ harmonic, the voltage conversion-gain will be about 2 dB larger than the value in (10).

### B. Input Power Matching

In order to find the conditions to provide input power matching around the third harmonic of the switching frequency, the transfers for the RF node before switches in Fig. 15 should be applied. For this purpose (7) is approximated around the harmonics of the switching frequency with the assumption of: $f_s \gg f_{rc}$, $f \approx nf_s$ and "n" an integer number. This approximation for the zero angle reception becomes as follows:

$$H_{0,RF}(nf_S, \theta = 0) \approx \frac{2N(1 - \cos(2\pi nD))}{4D(n\pi)^2} + (1 - ND) \qquad 0 < D \le 1/N. \tag{11}$$

Assuming N=8, n=3, D=1/8 we find $H_{0,RF}(3f_s, \theta = 0) \approx 0.62 V/V$ which translates to the input impedance of $Z_{in}(3f_s, \theta = 0) \approx 1.6R_S$. This value for input impedance does not exactly provide power matching for the source impedance of $R_S$, but is not very far off. As the parasitic capacitance of the switches at the antenna side and the bondpad give a charge sharing effect reducing the real input impedance, we find in simulation that the achieved value which is close enough to 50 Ω for reasonable matching.

### C. Noise Analysis

We will now aim to provide some insight in the noise behavior of the phased-array receiver architecture in Fig. 15. We will first assume that the noise is dominated with the mixer at the input. This means the noise of the $G_m$ blocks and TIAs is negligible. In order to find the total noise power at the output, the transfer function derived in (9) can be applied. As a result the total noise transfer at the I output can be derived as:

$$N_{out,I} = \left( \sum_{n=-\infty}^{\infty} |H_{n,I}(f, \theta)|^2 \right) N_{in} |_{f=0, \theta=0°} \approx 218.4 \times (Z_F g_m)^2 N_{in}, \tag{12}$$

in which $H_{n,I}(f, \theta)$ is defined in (9) and finally the Single-Side-Band (SSB) noise figure for the single-element receiver and $3^{rd}$ harmonic reception, can be found as:

$$NF_{SSB,3} = 10 \log \left( \frac{N_{out,I}}{CG_{R3}^2 \times N_{in}} \right), \tag{13}$$

in which $CG_{R3}$ is defined in (10). Evaluating (13) gives $NF_I \approx 5dB$. Considering image rejection, the double side band noise figure is 3 dB lower than this value. In a practical implementation the switch resistance will add noise to the circuit. Moreover, the non-ideal clocking will reduce the conversion gain resulting in increased noise. Finally, noise from the $G_m$ blocks will add to the noise calculated above.

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In case we applied $1^{st}$ harmonic reception the output noise calculated in (12) will not change, while the conversion gain will be increased by about 2 dB, which will translate to the NF improvement with the same amount.

## VII. MEASUREMENTS

An external clock with a frequency range of 0.8-6 GHz is divided by 4 on-chip, providing the $3^{rd}$ harmonic reception of 0.6-4.5 GHz (ratio 3/4). In order to measure beam patterns, 4 RF signal generators with a variable well-controlled phase difference are applied to emulate the incident signals impinging the receiver antennas from different spatial directions. Please note that all measurements in this section are carried out with 1 V supply voltage with the assumption that the antenna spacing is $\lambda/2$ ($\lambda$ is the wave length of the received center frequency). If the phased-array system is applied in a wide frequency range, reconfigurable antenna spacing may be required, but this is outside the scope of this paper.

The measured beam pattern for broadside reception at 2.4 GHz ($f_s=800\ MHz$) is shown in Fig. 19 (equal phase settings). It largely follows the ideally switched 4-element phased-array (gray line). In order to illustrate the spatial filtering at the antenna inputs, the compression point ($P_{1dB}$) of 4-elements is measured versus the incident angle of the blocking signal. The output power level of the 4 RF signal generators (with proper phase difference) are swept and the compression point was measured, observing the IF signals (see Fig. 19). While the measured results show a $P_{1dB}=-5$ dBm for zero incident angle, it increases to up to +10 dBm at null points, i.e. up to 15 dB spatial rejection. The maximum improvement is limited due to the effect of the switch resistance.

In Fig. 20 also the constructed beam patterns for 8 uniformly spaced electrical phase shifts are presented as polar plots. As discussed in section III-B, a maximum gain is achieved for the spatial angles 0, ±14.5, ±30, ±48.6 and 90 degrees, corresponding to electrical LO phase shifts of (0, ±45, ±90, ±135, 180 degrees) and antenna physical distance of d=$\lambda/2$ where $\lambda$ is the wavelength of the incident RF signal. The beam patterns are superimposed in a single figure in Fig. 21(a), showing a maximum gain variation of 0.8 dB over different directions. The beam patterns in Fig. 21(a) correspond to 8 possible uniformly increasing LO phase shifts for the 4 paths, i.e. for θ=0° desired angle this can be represented as a matrix of [0 0 0 0] (no phase shift), and for θ≈14.5° degree as [0 45 90 135]. The measured beam patterns are repeated in Fig. 21(b). An angle in between can be realized using non-uniform phase shifts, e.g. [0 0 45 45] renders θ ≈ 6° as shown in Fig. 21(b). Notice that the left side-lobe is now larger than the right one [9]; moreover, the main beam experience about 0.1dB attenuation

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which might be tolerable. This phase shift scheme can be extended to other beams to increase resolution at the cost of side-lobe suppression and possible small losses in the desired angle reception.

In order to verify the analysis results in section IV we have measured the beam patterns at different offset frequencies from the carrier frequency of 600 MHz ( $f_s$=$200MHz$) for zero angle reception. The measured results are compared with the theoretical and also Spectre-RF transistor-level simulation of the design (see Fig. 22). As it is illustrated the measured beam patterns are closely following the theoretical and simulated results. These cures are in fact the cross sections of the 3D plot of Fig. 5.

The measured and simulated results of IF transfer curves for 1-element and 4-element reception are shown in Fig. 23. The measured 3 dB bandwidth for the single element is 3.3 MHz (6.6 MHz @ RF). In this measurement the external TIAs were replaced by 10 Ω differential resistors in order to eliminate TIA bandwidth limitations. When all 4 elements are activated, the effective resistance seen by the capacitors "looking to the antennas" is reduced by a factor of 4 resulting in 4 times larger bandwidth. As shown in Fig. 23 $P_{1dB}$ increases to up to +12 dBm for out-of-band blockers with 4-elements. Moreover in/out-of-band single-element IIP3 measurement and simulation results are presented in Fig. 23. In the out-of-band 2-tone IIP3 measurements, the offset frequency of two tones is chosen in such a way that one of the 3rd order intermodulation terms, always falls in-band. The IIP3 is changing from 0 dBm in-band to > +20 dBm for large offset frequencies from the carrier frequency thanks to the frequency-domain N-path filtering occurring directly at the antenna input.

Fig. 24 shows the single element DSB NF of 4-6.3 dB. Please note that the calculated noise figure of a simplified model in section VI resulted in 2 dB DSB NF. Neglecting the noise of the blocks after the summation point (Gm cells in our case) in a 4 paths phased-array system, 6 dB improvement in SNR is expected when 4 paths are combined. However, noise floor measurements at the output show 4 dB improvement instead of 6 dB, due to the noise of Gm blocks. Simulations show 4.5 dB improvement in NF. Please note that in the traditional phased-array systems, the blocks after the summation point are usually after some gain stages, so that the noise of these blocks might have less effect on the SNR improvement of the overall system. In our case the summation point is already at the antenna input without any gain stage upfront. As a result the noise from Gm blocks limits the SNR improvement to 4 dB instead of 6 dB.

All analog Gm blocks consume 17 mW together providing 100 mS in each of the I and Q paths. Overall power consumption with 4 elements activated is 34-119 mW for the received frequency range of 0.6-4.5 GHz (see Fig. 24). The maximum ripple in the gain is about 3 dB.

In this design the linearity is limited by the nonlinear switch resistance and also nonlinearity from the Gm blocks. To illustrate the effect of CMOS switch nonlinearity, the in-band IIP3 measurement for the whole RF-frequency range is shown in Fig. 25 for two cases. In case 1 two tones are applied to all of elements set to zero angle reception and the measured intercept point is referred to a single-element input (+6 ..+11 dBm is measured). Case 2 presents a single-element excitation measurement of IIP3 rendering 0 ..+2.6dBm. These results differ for this special case of zero angle reception, as the 4 switches from 4 receivers are "ON" during the same LO-phase and as a result linearity improves compared to the single-element measurement. For other reception angles without clock-overlap this is not the case.

The blocker noise figure simulation results are illustrated in Fig. 26. The simulations are carried out for a blocker at 100 MHz offset frequency from the wanted frequency of 2.4 GHz for out-of-band cases. Here the single-element SNR at the input is taken with respect to 4-element output (neglecting increased aperture) which leads to negative noise figure when 4-elements are activated. Simulation results show with 0 dBm blocker out-of-band/beam, the noise figure degrades with 5 dB.

The measured S11 is shown for three switching frequencies in Fig. 27, consistently giving better than -10 dB of S11 in the received band. S11 is measured with just one element and also with 2 elements activated, where the latter (common mode) S11 shows a broader dip in Fig. 26, consistent with doubled bandwidth as discussed earlier. In the measurement of 2-element S11, two paths are activated with two ports of a network analyzer and then the common mode S11 results are collected. This measurement has the purpose of proving experimentally that indeed filtering takes place at the antenna inputs. The narrow band matching at the chip input results in wave reflections of out-of-band/beam signals. As the chip implements a low-ohmic out-of-band/beam impedance, input voltage swing remains low which is beneficial for linearity. In a practical application, off-chip components must be taken into account along with the impedance created by the chip input.

The LO leakage to RF nodes at the antenna inputs is measured while all 4 elements were activated and at the 3rd harmonic of the switching frequency the leaked power is <-70 dBm for the whole band. The undesired folded band around the first LO-harmonic is rejected between 25-38 dB.

The measurement results are compared to three previously reported 4-element phased-array systems. Clearly remarkable $P_{1dB}$ and NF are achieved, and the dynamic range at the antenna inputs is substantially improved compared to previous work. Comparing to [7] in which the 4-phase LO phase shifting in combination with vector modulation is adopted, here we use just 8-phase LO phase shifting (no amplitude control). This renders superior input referred P1dB and NF compared to [7] because we move the summation point to the antenna input. However, with uniform phase shifting, less spatial angle resolution is achieved (3 bits compared to 5 bits in [7]), while the lack of amplitude control allows for less control in the beam pattern and sidelobe level.

Moreover compared to the 65 nm version of the same design [8] the frequency range is improved while power consumption is reduced roughly by a factor 2 for the same frequency, clearly showing the benefit of downscaling digital circuitry. Considering the out-of-band/beam compression point results in table I, there is not much difference between the 28 nm and 65 nm version. This is mainly because P1dB has a direct relation with the maximum rejection of blockers at the mixer input, which is limited by switch resistance. As the switch resistance for both versions is in the same order (4-5 Ω) similar out-of-band/beam P1dB results. On the other hand faster digital clocking in 28 nm may improve mixer linearity, while a lower supply, limits the full swing to 1 V in 28nm versus 1.2 V in 65 nm. Considering these competing factors, IIP3 is still improved by 3 dB in 28 nm.

## VIII.  CONCLUSIONS

To improve interference robustness, simultaneous spatial- and frequency-domain filtering directly at the antenna input of a 4-element phased-array receiver is proposed. By applying 8-phase passive switch-R-C mixers directly at the antenna and summing the resulting multiphase signals directly at the baseband capacitors, an angle dependent $P_{1dB}$ is achieved with an improvement of up to +15 dB for out-of-beam/band signals. Hard-driven switches implementing passive mixers provide high linearity of up to +2.6 dBm in-band and +11 dBm out-of-band. By exploiting 3rd harmonic down-mixing, high RF frequencies up to 4.5 GHz are covered at relatively low power consumption. A large tuning range of 0.6-4.5 GHz with simultaneous spatial- and frequency domain filtering can be useful for in- and out-of-band blocker rejection and for future dynamic spectrum access applications exploiting software-defined or cognitive radio.

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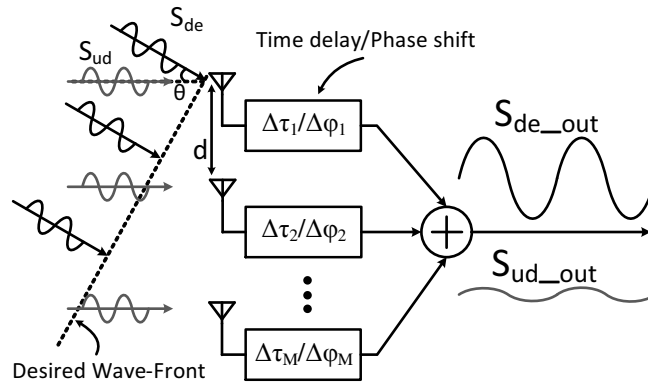
**Figure 1. Block diagram of an M-element phased-array antenna system with incident desired (de) and undesired (ud) signals. θ is the angle between the incident signal and the normal line to the antenna axis.**
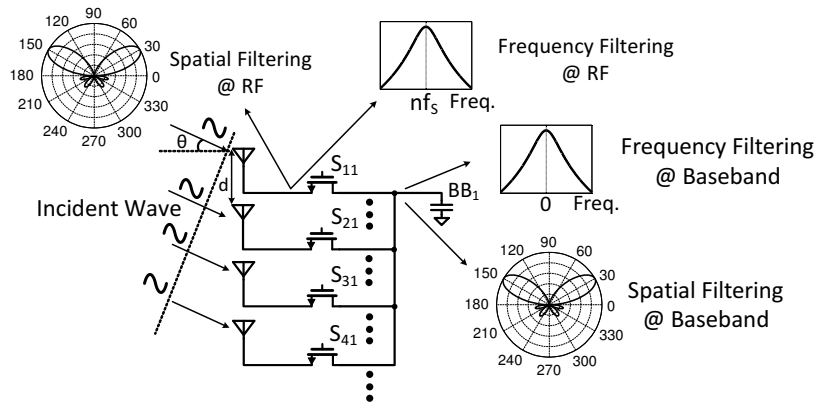


**Figure 2. Spatial- and frequency-domain filtering effect of baseband (BB) capacitor in a mixer-first phased-array system for θ=30°.**
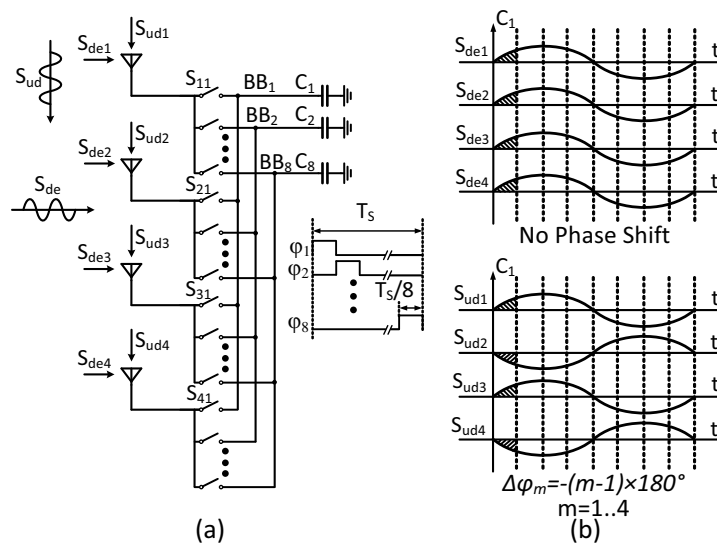


**Figure 3. (a) Mixer first 4-element phased-array system (b) Timing diagram for the desired signal ($S_{de}$) and undesired signal ($S_{ud}$) direction at 0 and 90 degrees respectively.**
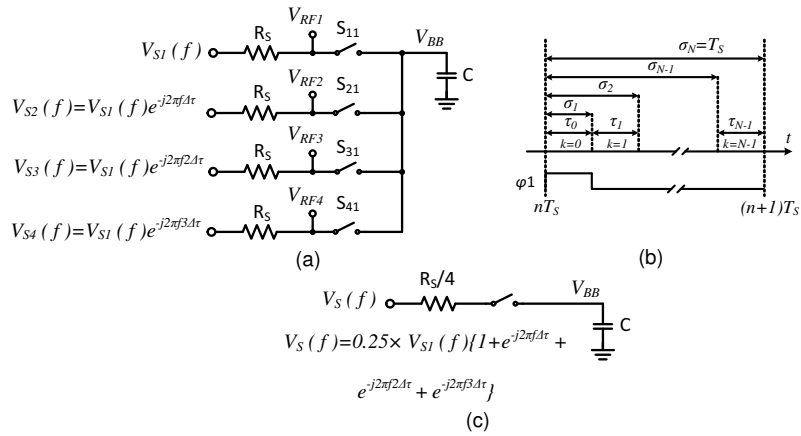
Figure 4. (a) Single-path of a 4-element phased-array receiver (b) Time intervals for the state-space analysis. (c) Simplified diagram for zero angle reception.
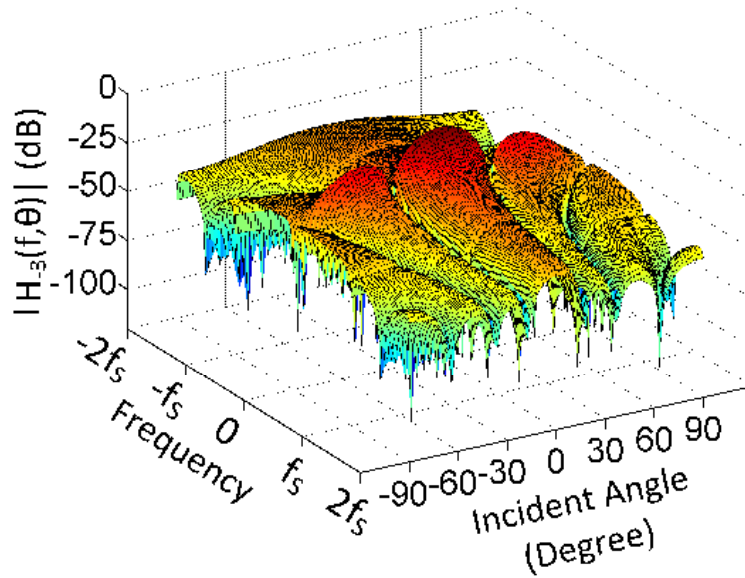


Figure 5. Spatial- and frequency-domain filtering on the baseband capacitors for a switching frequency $f_s$ and $3^{rd}$ harmonic down-conversion ($H_{-3}$)
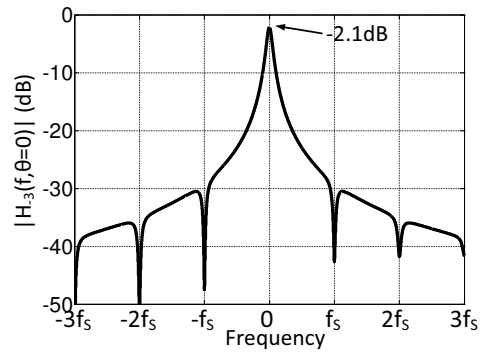


Figure 6. Cross section of the 3D plot in Figure 5 at $\theta=0°$.

(a)



(b)
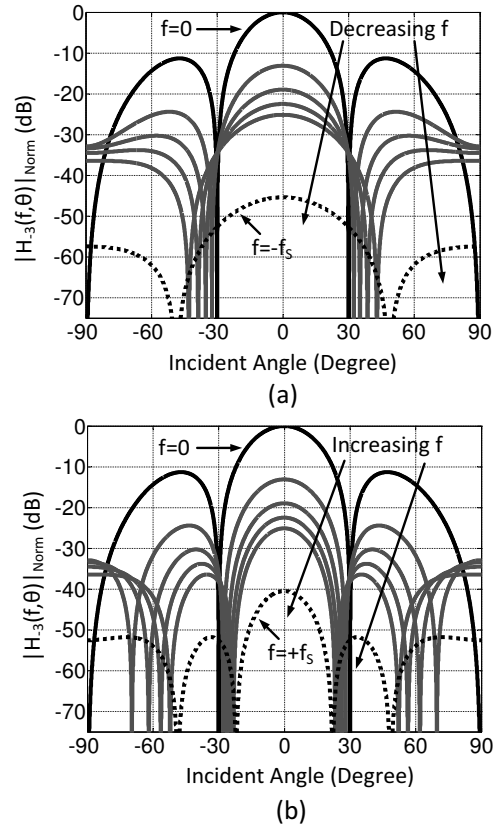
**Figure 7. Cross section of the 3D plot in Figure 5 at different offset frequencies.**
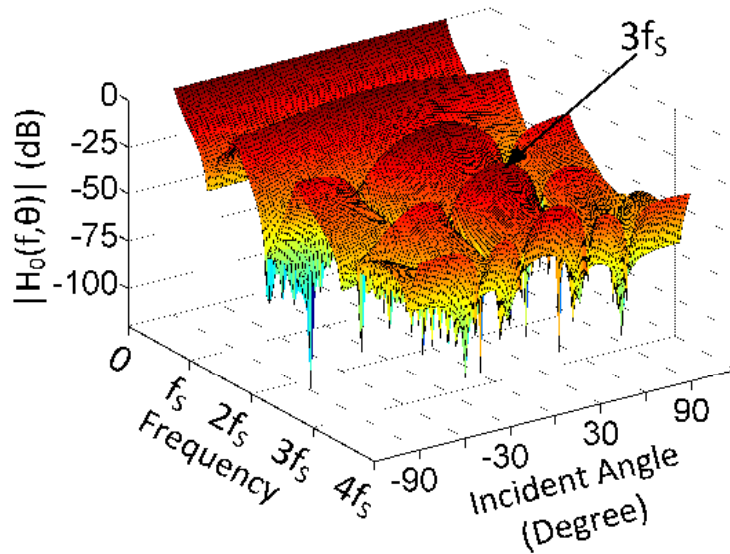


**Figure 8. Spatial- and frequency-domain filtering at the antenna inputs ($H_0$)**

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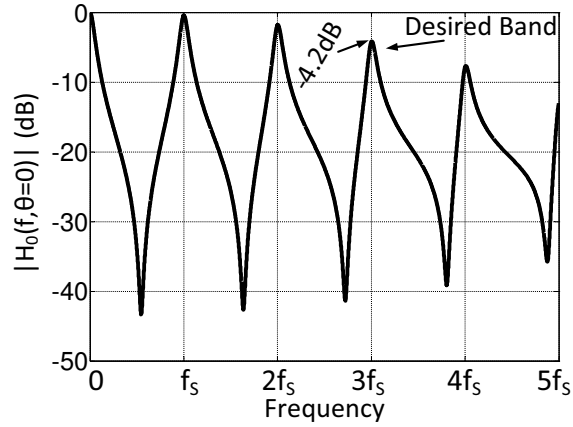
**Figure 9. Cross section of the 3D plot in Figure 8 at θ=0° illustrating N-path frequency domain filtering at the antenna.**
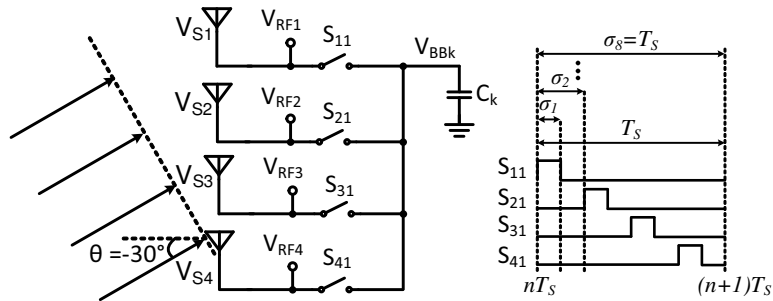


**Figure 10. Circuit and timing diagram of reception at desired angle θ=-30°.**
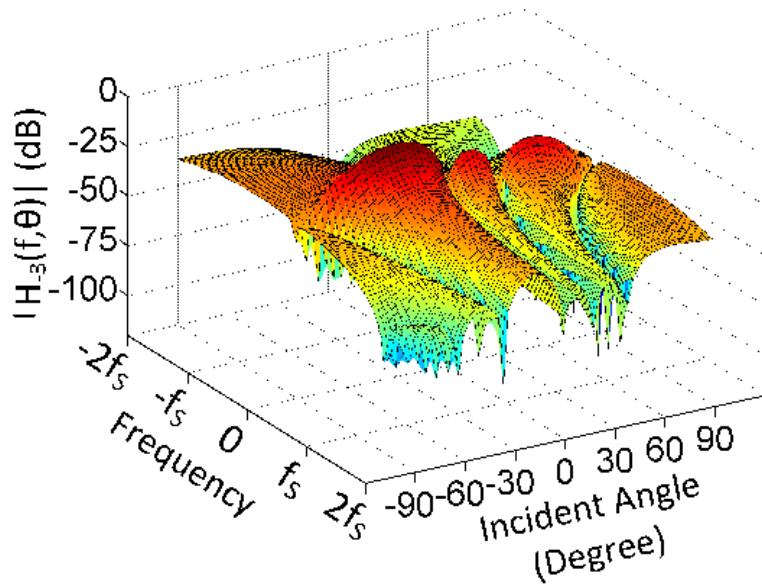


**Figure 11. Baseband transfer of 3$^{rd}$ harmonic reception (H$_{-3}$) for a desired main beam at θ=-30°.**

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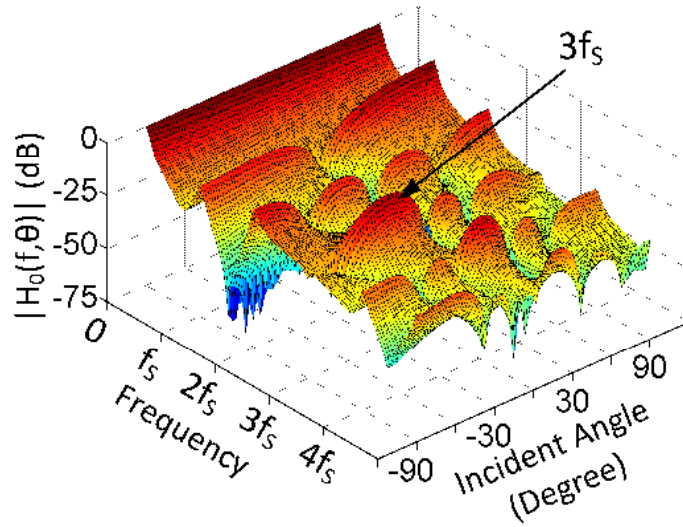
**Figure 12. Spatial- and frequency-domain filtering at the antenna inputs ($H_0$) for a desired main beam at $\theta=-30°$.**
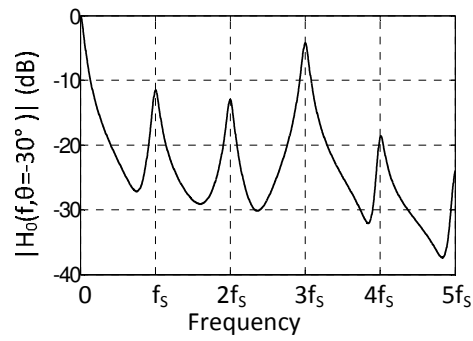


**Figure 13. Cross section of the 3D plot of Fig. 12 ($\theta=-30°$).**
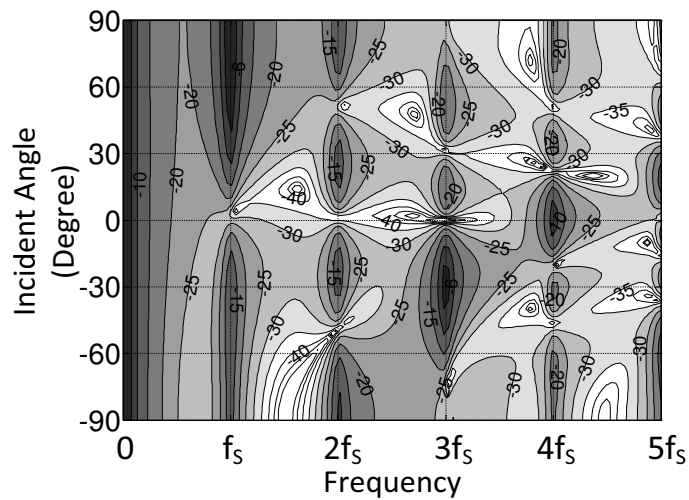


**Figure 14. Contour plots derived from the 3D plot of Fig. 12 (lighter color indicates more rejection).**
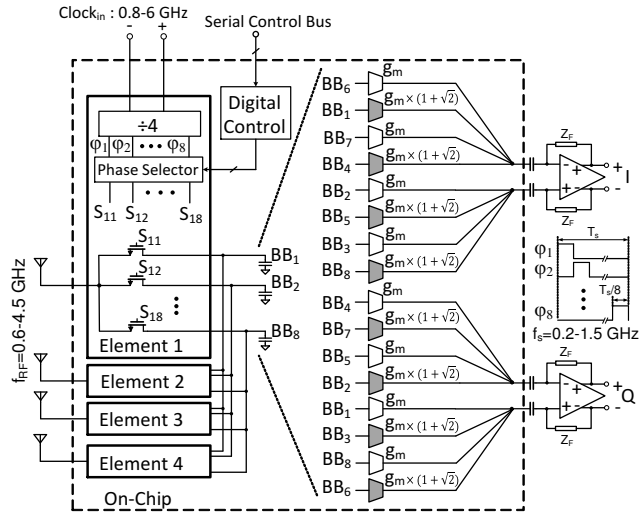
**Figure 15. Block Diagram of the 4-element phased-array system.**
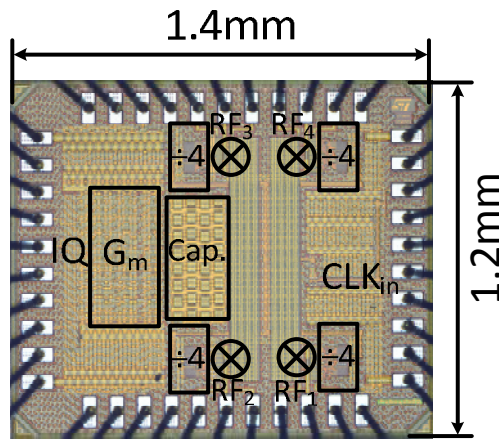


**Figure 16. Chip micrograph in 28 nm CMOS technology.**



$$\vec{A} = \left(1 + \sqrt{2}\right)\left(\overrightarrow{BB_1} + \overrightarrow{BB_4}\right)$$
$$\vec{B} = \left(\overrightarrow{BB_6} + \overrightarrow{BB_7}\right)$$

1st Harmonic   $\vec{A} + \vec{B} = 0$      3rd Harmonic   $\vec{A} + \vec{B} \neq 0$
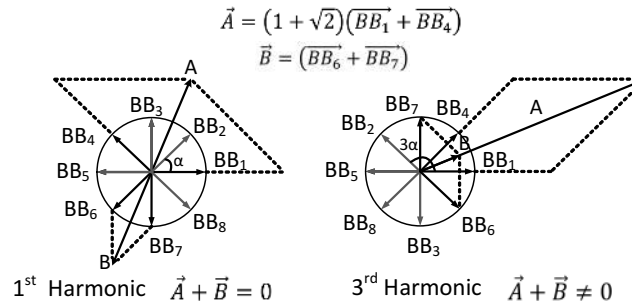
**Figure 17. Phase summation for receiving the 3rd harmonic at $f_{RF}=3f_s$ and rejecting the 1st harmonic.**
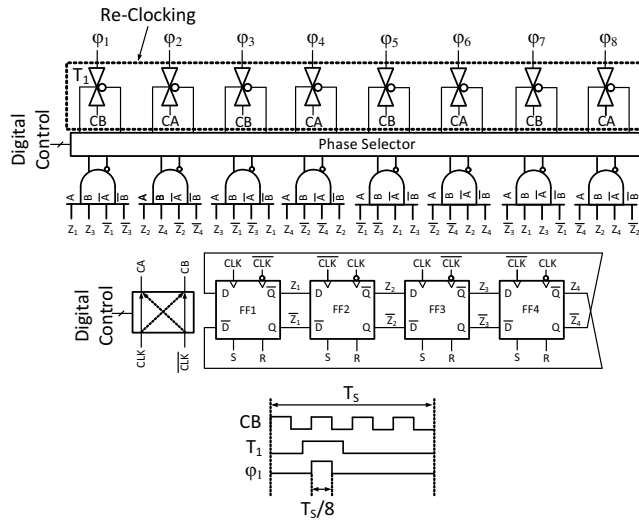
**Figure 18. Block diagram of the clock divider.**
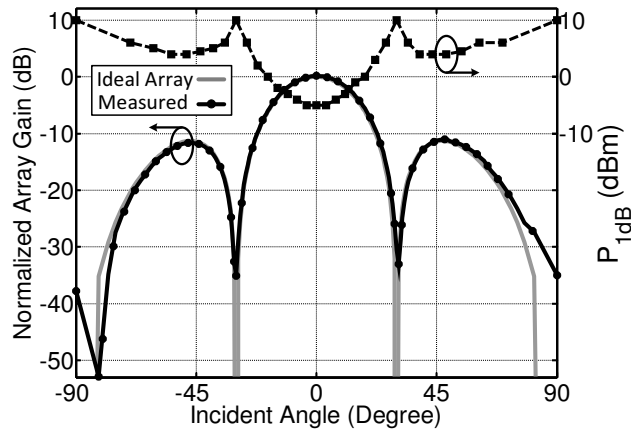


**Figure 19. Beam pattern at zero incident angle and P$_{1dB}$ measurements at f=2.4 GHz received band.**
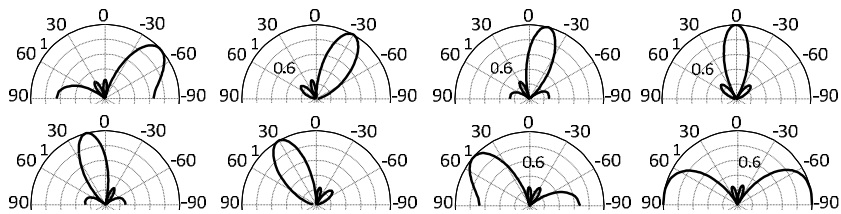


**Figure 20. Constructed (measured) beam patterns at f=2.4 GHz received band.**
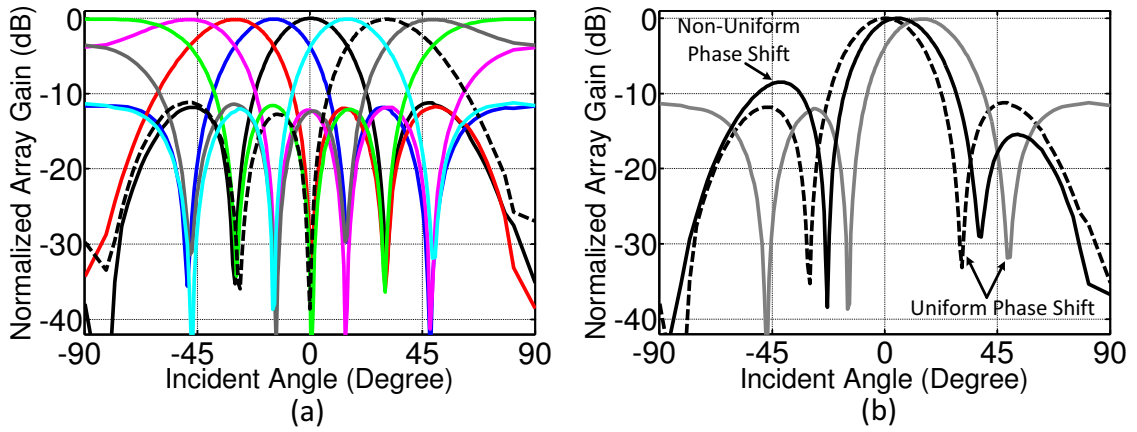
**Figure 21. (a) Constructed (measured) beam patterns at f=2.4 GHz received band. (b) Increasing spatial angle resolution via non-uniform phase shifting (Measurements).**
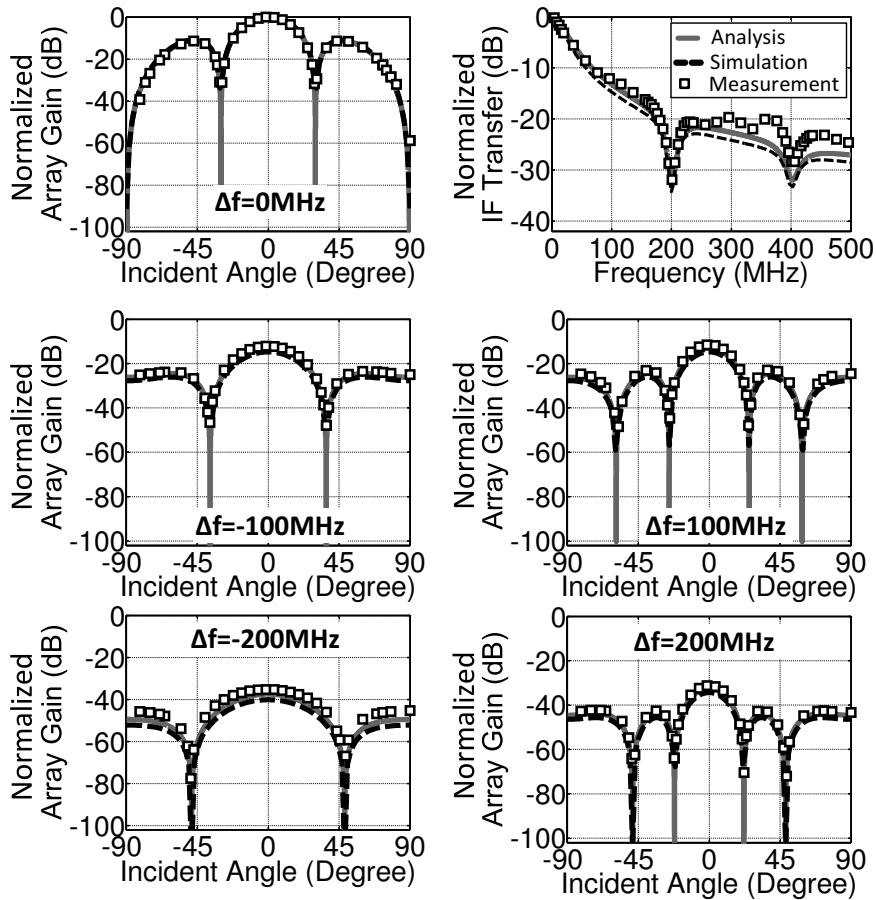


**Figure 22. Comparison of the beam pattern and IF transfer at different offset frequencies from the carrier frequency of f=600 MHz.**
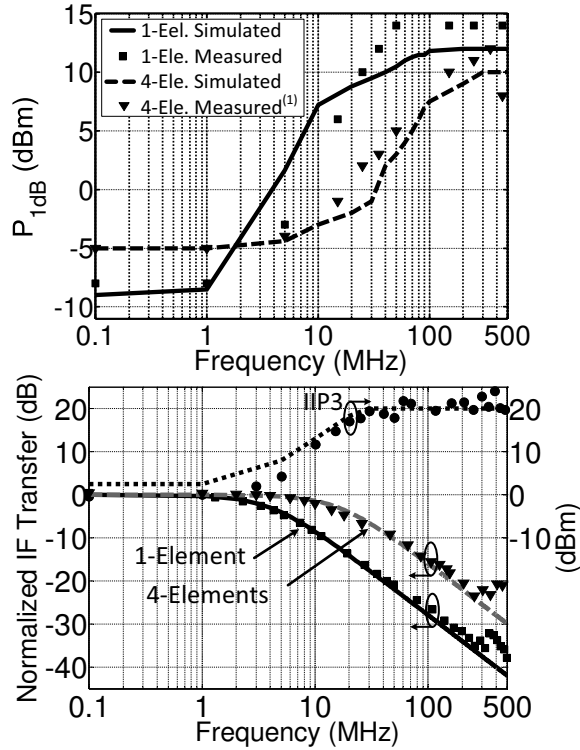
**Figure 23. Measured (lines) and simulated (markers) results for the IF transfer, IIP3 and $P_{1dB}$ at $f_{RF}$=2.4 GHz. IIP3 is measured for single-element; $P_{1dB}$ is measured with 4-elements, but power is referred to the single-element input.**
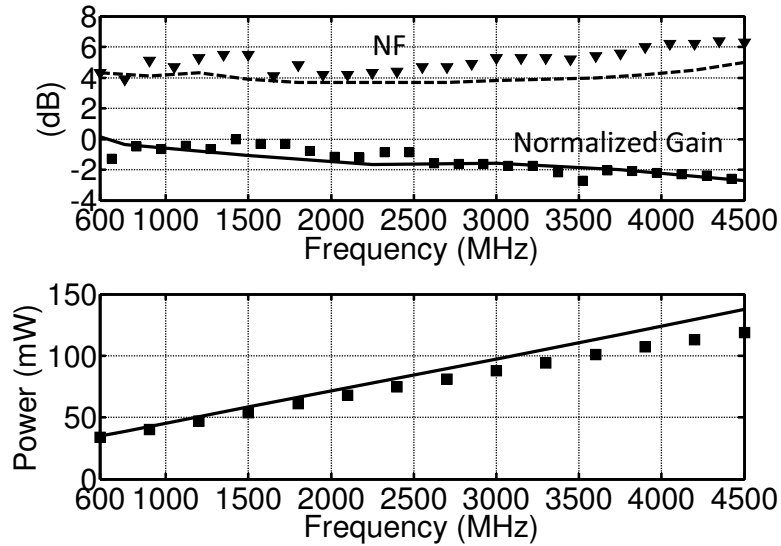


**Figure 24. Measured (markers) and simulated (lines) results of NF, normalized gain and in-beam/band IIP3 of single-element, and power consumption of 4 elements versus received frequency.**
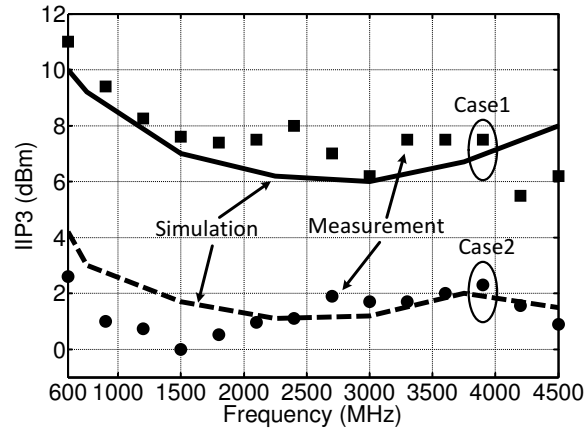
**Figure 25. In-band IIP3 simulation and measurement results for: Case 1) 4-element measurement at zero degree spatial angle where power is referred to the single-element input. Case 2) Single-element measurement.**
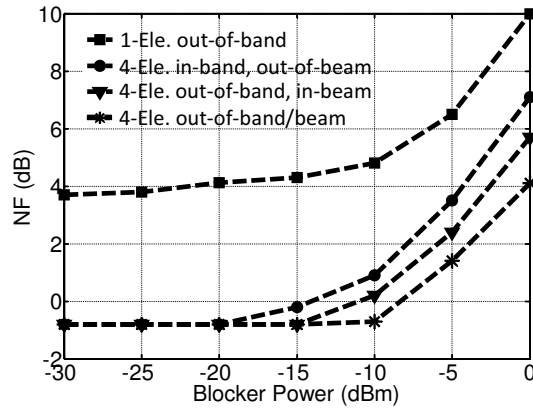


**Figure 26. Blocker noise figure simulation results (received band is 2.4 GHz). The blocker is applied at 100 MHz offset from the wanted frequency of 2.4 GHz for out-of-band cases.**
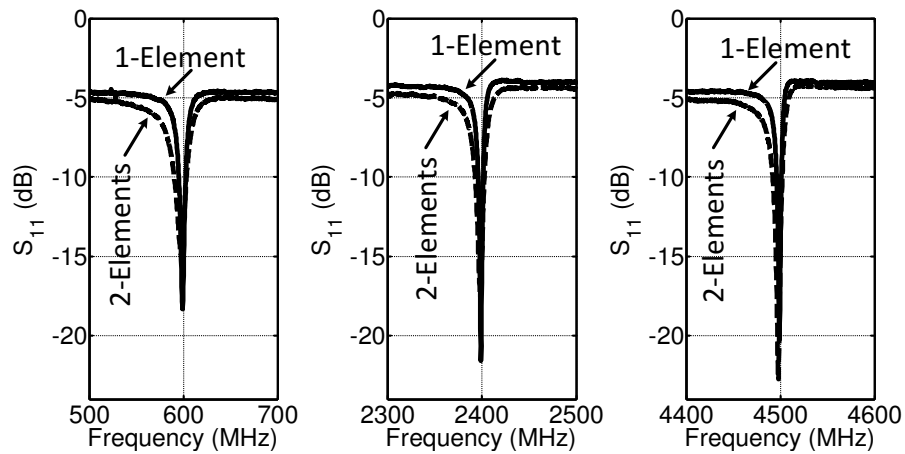


**Figure 27. Measured $S_{11}$ for 1-element and for 2 simultaneously activated elements at three received frequency bands.**

**Table I. Comparison of CMOS 4-element phased-array systems.**

| | [5] | [6] | [7] | This Work (65 nm) [8] | This Work (28 nm) |
|---|---|---|---|---|---|
| **Technology** | CMOS 90 nm | CMOS 65 nm | CMOS 65 nm | CMOS 65 nm | CMOS 28 nm |
| **Active Die Area (mm$^2$)** | 1.4 | 0.44 | 0.18 | 0.97 | 0.65 |
| **RF Frequency (GHz)** | 4 | 1-4 | 1.5-5 | 0.6-3.6 | 0.6-4.5 |
| **Phase/Amplitude Resolution (bits)** | 5 / 3 | 5 / 3 | 5 / - | 3 / - | 3 / - |
| **4-Elements Power (mW)** | 166 | 308 | 65-168 | 68-195 | 34-119 |
| **1-Element IF Bandwidth (MHz)** | NA | 65 | 300 | 5[1] | 3.3[1] |
| **1-Element Noise Figure (dB)** | 13 | 10 | 18 | 3-6 | 4-6.3 |
| **4-Elements SNR Improvement (dB)** | 6[2] | 6[2] | 6[2] | 4 | 4 |
| **1-Element Input Referred P$_{1dB}$ (dBm)** | NA | -14 | 2 | -5.5 (In-Beam/Band)[3] +10 (Out-of-Beam)[3] +11 (Out-of-Band)[3] | -5 (In-Beam/Band)[3] +10 (Out-of-Beam)[3] +12 (Out-of-Band)[3] |
| **1-Element IIP3 (dBm)** | 2 | -1 | 13 | +2 .. +9 [3] -1 ..+3.6 [4] | +5.5..+11[3] 0..+2.6[4] |

(1) IF$_{BW}$ is 4 times larger when 4 elements are activated (see Fig. 23).

(2) 6 dB improvement in SNR is expected but not measured.

(3) Measured with 4-elements, while power is referred to the single-element input.

(4) Single-element measurement.