A 400μW Hz-Range Lock-In A/D Frontend Channel for Infrared Spectroscopic Gas Recognition

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***Abstract*—This paper presents a low-power and fully integrated frontend channel for long-wave infrared spectroscopic gas recognition. The proposed channel circuitry includes: input sensor biasing, sub-Hz high-pass filtering and pre-amplification, differential blind cancellation, and lock-in A/D conversion. The proposed CMOS circuits make extensive use of transistor sub-threshold operation and digital programmability. Experimental results are presented for a 0.3mm^2 400μW channel prototype integrated in 0.35μm CMOS technology.**

***Index Terms*—CMOS, low-power, sensor frontend, ADC, lock-in, LWIR, gas recognition.**

I. Introduction

FAST and high-accuracy gas recognition systems are becoming a desired product in key application fields like environmental monitoring, food quality control, toxic gas warning and medical analysis, which demand not only detection but also quantification of the chemical compounds present in the air on a real-time basis.

Classically, this type of sensory systems are based on a single device which has been specifically functionalized as a chemical sensor to match the main compound of the targeted gas. Integration technology examples of these chemical sensors can be found in the form of ion selective field effect transistors (ISFET) [1], hot plates [2], chemresistors [1], xerogel films [3] or more recently carbon nanotubes (CNT) [4]. However, the main bottleneck of these gas sensors is the lack of selectivity due to the difficulty of finding an exact chemical match between the sensor and the target gas. For this reason, several sensors are usually combined in critical gas detection applications in order to avoid excessive false positive alarms. Anyway, this type of sensory systems are clearly not suitable when recognition of several gas targets is needed by the application, like in toxic gas detection.

In this sense, a promising strategy for optical gas recognition is the spectroscopic study of the long-wave infrared (LWIR) light absorption when traveling through these chemical compounds using silicon microbolometer arrays as LWIR sensors [5]. The resulting system is illustrated in Fig. 1, where lock-in reading is mandatory in order to cope with background noise, while a matched microbolometer not being IR illuminated (i.e. blind sensor) is also added as a reference for rejecting common-mode interferences. The general output of this type of sensory systems is not a particular gas target detection but a collection of relative losses for each illumination wavelength. In fact, gas recognition is implemented in the numerical domain by correlating this absorption fingerprint with a pattern database. Hence, detection of multiple targets is then a matter of measuring enough wavelength bins, extending the catalog of patterns and developing specific identification algorithms. In counterpart, this system approach requires in general multi-channel complex frontend circuits. In particular, the key CMOS design constraints are the integration of the Hz-range lock-in processing for a compact packaging with the sensor array, low-power operation to avoid heating the IR thermal sensors, and high-linearity to preserve attenuation information of the lock-in signal. Previous multi-channel read-out solutions for LWIR [6]–[8] or for general purpose sensors [9] do not include dedicated A/D converters (ADC) per channel and exhibit high-power consumption levels. On the other hand, the existing few low-power built-in ADC proposals for LWIR sensors like [10] lack of Hz-range lock-in processing.

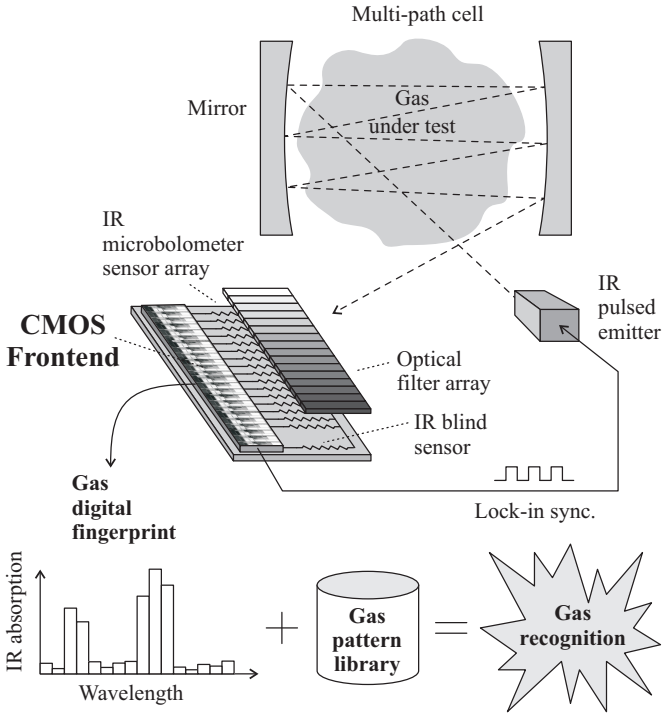

Figure 1. General view of an IR spectroscopic gas recognition system.

This paper presents a fully-integrated digital-output CMOS frontend channel for LWIR spectroscopic gas recognition, which exhibits low-power consumption and compact area. The proposed circuit module allows the CMOS integration of sub-Hz lock-in filtering and pre-amplification, blind sensor cancellation and A/D conversion. Furthermore, the extensive

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digital programmability of each channel also enables the compensation of process deviations inside the IR sensing array.

II. IR Spectroscopic Gas Recognition System

The simplified scheme of the gas recognition system is shown in Fig. 1. Basically, the pulsed IR emitter illuminates the gas under test inside the optical chamber, and the mirror structure implements a multi-path cell in order to magnify the gas absorption losses. Once IR light reaches the sensor head, it is first split through a passive array of optical filters according to the interesting set of wavelength bins. Then, the array of LWIR thermal sensors translates the incoming light power into an equivalent change in resistance.

Hence, the aim of the CMOS frontend is to supply a multi-channel interface between the LWIR thermal sensor array and the digital domain where the gas recognition is really performed. As part of the integrated circuit signal processing, each channel includes lock-in demodulation capabilities in phase with the IR emitter for improving the overall signal sensitivity. In fact, the required dynamic range per channel is derived from the minimum attenuation factor to be detected in the lock-in signal before and after the gas is inside the optical chamber, which in turn depends on the minimum gas concentration.

III. Read-Out Channel

From the general view of the gas recognition system of Fig. 1, each frontend channel should meet the following specifications: built-in ADC to minimize the overall noise bandwidth of the system thanks to the parallel A/D conversion of all the read-out channels; no external components and reduced area to allow a compact packaging with the sensor array; high programmability to compensate for IR sensor process deviations; and very low-power consumption to avoid any temperature drift close to the LWIR thermal sensors and to maximize the battery life in portable applications.

For such purposes, the channel architecture of Fig. 2 is proposed, being V_{com} the common voltage bias for the LWIR sensor array. Each CMOS read-out channel consists of a sensor bias current source, a sub-Hz high-pass pre-amplifier for DC decoupling and low-frequency noise reduction, a linearized differential transconductor for the rejection of the common disturbing signals detected by the blind sensor, and a current-input continuous-time first-order 3-level $\Delta\Sigma$-modulation ADC [11] with built-in lock-in demodulation capabilities. For this predictive ADC, the pulse density modulation (PDM) stage is in charge of the in-band noise shaping, while lock-in demodulation is digitally implemented by cross-coupled multiplexers, and the 24bit counter is used here for the decimation filtering. In fact, the overall ADC scheme is operating asynchronously in order to optimize channel power consumption. Since each stage of the channel can be digitally programmed, a 15bit configuration register is incorporated as well. Finally, an analog reference and bias generator block is also included, so each channel can operate independently to avoid crosstalk.

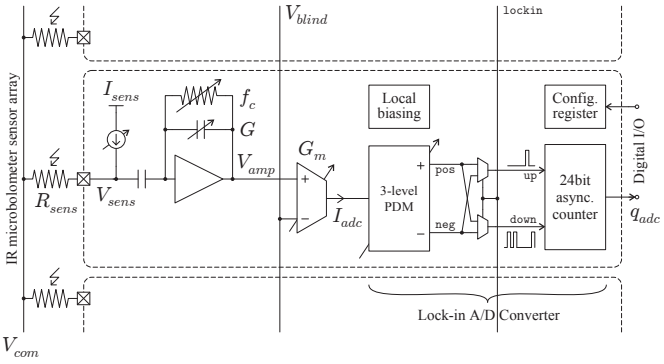

Figure 2. Functional description of the fully-integrated read-out channel.

The signal from each individual LWIR sensor (ΔR_{sens}) is obtained by biasing it to a constant but programmable current level (I_{sens}). The resulting voltage signal:

$$\Delta V_{sens} = I_{sens}\Delta R_{sens} \tag{1}$$

is first restored in terms of both amplitude and frequency by the high-pass pre-amplifier according to the programmable gain (G) and cut-off frequency (f_c), respectively. Then the obtained waveform (V_{amp}) is differentially sensed respect to the equivalent output of the blind channel (V_{blind}) by the programmable transconductor (G_m) in order to cancel any disturbing signal not related with the optical measurement itself. The effective current signal (I_{adc}) is finally converted into the digital domain by the lock-in ADC. The first stage of this ADC consists of a bi-phase PDM modulator, which pushes the instantaneous A/D quantification errors of the modulated pulses (`pos`,`neg`) into high frequency [11]. The cross-coupled multiplexing stage performs the digital lock-in demodulation in synchronization with the IR emitter reference (`lockin`), so it attenuates non in-phase noise and disturbing signals in its output pulse streams (`up`,`down`). Finally, the asynchronous ripple counter plays the role of a first-order low-pass decimator filter in order to obtain the digital output (q_{adc}).

A. Pre-Amplification and Filtering

The first stage of the frontend channel depicted in Fig. 2 has two main signal processing tasks: decoupling the IR lock-in pulses from the sensor DC bias point, and recovering the signal integrity of such IR pulses. Obviously, both tasks require a combined high-pass filtering response together with amplitude gain. In the context of CMOS integrated circuit design, the key bottle neck for this pre-amplification stage is the full integration of the typical very low corner frequencies for the LWIR thermal sensor lock-in demodulation. Previous proposals based on active control loops require external capacitors [12] or the use of mismatching sensitive floating voltage sources [13]. In order to overcome these issues, the MOS-C high-pass pre-amplifier of Fig. 3 is proposed. In what follows, all MOSFET bulk terminals are connected to their corresponding power supply rails.

This CMOS circuit implements both high-pass filtering and voltage amplification in a single stage without any external

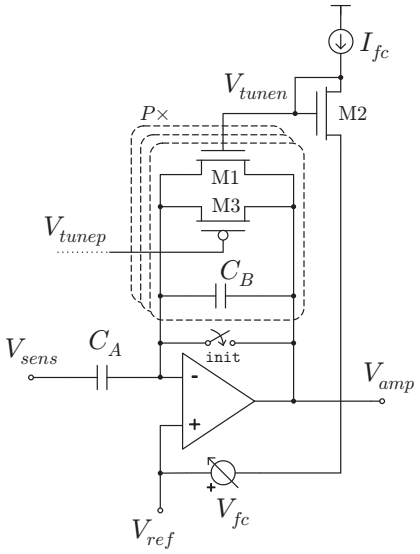

Figure 3. Proposed sub-Hz programmable MOS-C high-pass pre-amplifier.

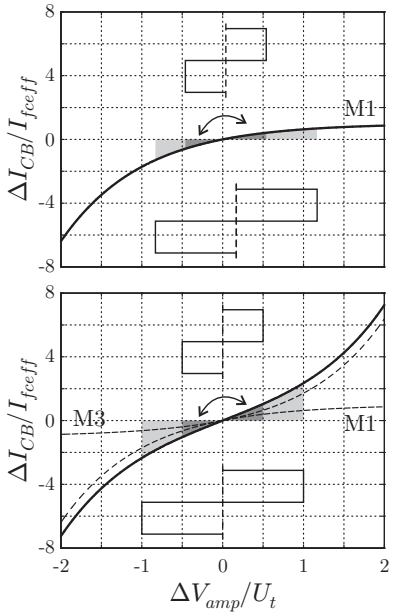

Figure 4. Dynamic output offset effect due to MRC non-linearity (top) and proposed compensation (bottom) for the high-pass pre-amplifier of Fig. 3. Gray areas illustrate charge balancing to show output DC dependence on signal amplitude.

component by using a MOS resistive circuit (MRC) operating in weak inversion (i.e. subthreshold). For high-frequency, the circuit behaves as a highly linear capacitive amplifier with a gain factor:

$$G = \frac{\Delta V_{amp}}{\Delta V_{sens}} = \frac{C_A}{C_B} \tag{2}$$

where ΔV_{amp} is the signal at the pre-amplifier output. On the other hand, the MOS feedback network M1-M3 supplies a feedback path for DC decoupling. A switch is also added in parallel to the feedback network for a fast initialization of the pre-amplifier (`init` high) even for very low corner frequencies. In the case of M1, the tuning of the corner frequency is automatically obtained by introducing a matched transistor M2, which generates the suitable M1 gate potential (V_{tunen}) according to the tuning current (I_{fc}) and the differential source potential (V_{fc}). The generation of the equivalent control V_{tunep} for M3 is not shown here for simplicity. Supposing M1 and M2 operating in weak inversion conduction and saturation respectively, the equivalent high-pass corner frequency is found to be:

$$f_c = \frac{1}{2\pi}\frac{I_{fceff}}{C_B U_t} \tag{3}$$

$$I_{fceff} = I_{fc} e^{-\frac{V_{fc}}{U_t}} \tag{4}$$

where U_t and I_{fceff} stand for the thermal potential the effective tuning current respectively. Hence, this topology enables a multi-decade log control of f_c through a compressed voltage range of V_{fc} (e.g. $f_c \times 10^{\pm 3}$ requires just $V_{fc} \pm 173$mV at room temperature).

Concerning MRC non-linearity, the asymmetrical I/V law of M1 does not generate signal distortion but a dynamic offset at the output, as illustrated in Fig. 4(top). Such and undesired effect is compensated by the complementary M3 transistor of Fig. 3 thanks to the combined I/V symmetry shown in Fig. 4(bottom).

Finally, the V_{fc} voltage source required in Fig. 3 is internally generated by the programmable circuit of Fig. 5. Again, supposing weak inversion saturation for the M1-M2 pair:

$$V_{fc} = M U_t \ln(NK) \tag{5}$$

$$f_c = \frac{f_{co}}{(NK)^M} \quad \text{for} \quad f_{co} = \frac{1}{2\pi}\frac{I_{fc}}{C_B U_t} \tag{6}$$

a large scaling of the corner frequency can be obtained even for high G factors (i.e. low absolute C_B values). What is more, the proposed f_c programming circuit is independent from both temperature and technology variations. In fact, the remaining thermal dependence of f_{co} in (6) is compensated here using a proportional-to-absolute temperature (PTAT) current reference circuit for I_{fc} as proposed by these authors in [14]. Combining the V_{fc} tuning with the addition of the parallel networks (P) in Fig. 3, both f_c and G values can be programmed independently, as validated in Section IV.

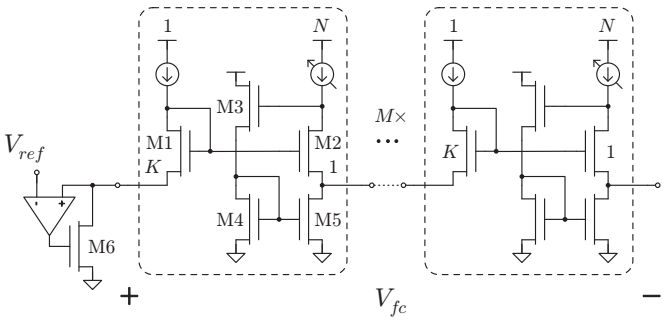

Figure 5. Floating voltage source proposed for the tuning of f_c in Fig. 3.

B. Blind Cancellation

The second stage of the channel scheme of Fig. 2 is in charge of performing the differential to single-ended amplification of the active pre-amplifier output respect to the blind pre-amplifier reading. The main purpose of this processing step is double: cancellation of unwanted disturbing signals generated by thermal, optical, mechanical or even electrical interferences; and V/I conversion of the LWIR signal to be integrated by the current-mode ADC scheme presented in next subsection.

For these purposes, the transconductance amplifier of Fig. 6(a) is proposed. The required linearization to preserve amplitude information of the lock-in signal is based on the classical cross-coupled differential pair topology M1-M4 operating in strong inversion saturation [15]. However, a new built-in limiter mechanism is introduced here through M5-M6, which allows programmability of the linear and saturation ranges according to Fig. 6(b). This feature is of special importance in order to not overload the ADC stage of next section. Basically, the purpose of M5 (and M6) is to ensure linearity of the cross-coupled structure by keeping a constant current flowing through M2 (and M3). When the output signal current reaches $+I_{max} - I_{gm}$ (or $-I_{max} + I_{gm}$), M5 (or M6) is cut-off and the circuit shows a non-linear compressing curve above (or below) that point. The resulting large signal programmable transconductance is:

$$G_m = \frac{I_{adc}}{V_{amp} - V_{blind}} = 2\sqrt{\frac{2\beta I_{gm}}{n}} \tag{7}$$

where β and n are the current factor and the subthreshold slope [16] respectively.

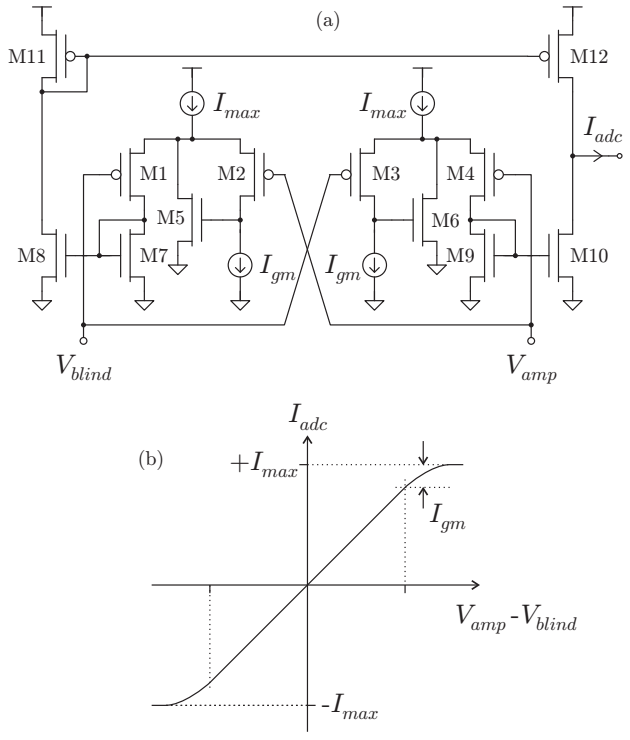

Figure 6. Proposed linear transconductor (a) and equivalent built-in limiter function (b).

C. Current-to-Frequency Conversion

For the 3-level PDM section of the channel A/D converter of Fig. 2, the scheme of Fig. 7(a) is presented consisting on a close loop containing an analog integrator and a window comparator. The analog integrator is based on a previous idea from these authors [17], which exhibits high robustness against reset times. Basically, the principle of operation is as follows: during initialization (`init` high), the analog integrator is reset, while C_{res} remains connected to V_{int}; once in acquisition (`init` low), I_{adc} is integrated in C_{int} while C_{res} is tracking the offset, the low frequency noise and the output signal itself of the operational amplifier; finally, when the $\pm V_{th}$ threshold is reached, the comparator generates a pulse (`pos` or `neg`) causing C_{res} to be connected to the input of the analog integrator. As a result, the charge stored in C_{int} is compensated by the matched C_{res} and the reset is completed. It is important to note that this topology does not block the integration of I_{adc} in C_{int} during the reset time, behaving like a continuous-time integration during the full acquisition window. Thanks to the absence of dead times during the pulse width (T_{pulse}) of the PDM stream, this scheme exhibits a high linear behavior even for output frequency rates (f_{PDM}) close to the hard limit of $1/2T_{pulse}$, as shown in Section IV. In this scenario:

$$f_{PDM} = \frac{I_{adc}}{C_{int} V_{th}} \tag{8}$$

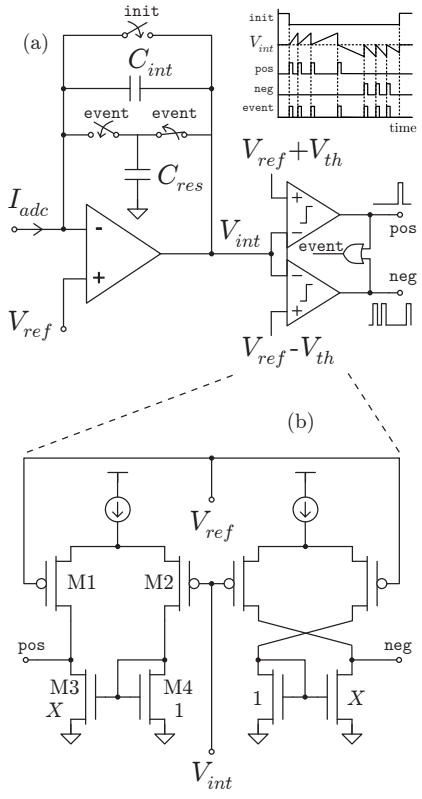

Figure 7. Reset-insensitive analog integrator (a) with built-in threshold window comparator (b) proposed for the 3-level PDM stage of Fig. 2.

For the implementation of the window comparator, a very compact circuit is proposed in Fig. 7(b). Instead of generating a dual $\pm V_{th}$ floating source, an equivalent threshold is built

inside the comparators themselves through circuit asymmetries in the M1-M4 cell. In this case, supposing weak inversion saturation for M1-M2:

$$V_{th} = nU_t \ln X \tag{9}$$

Finally, the digital output word of the asynchronous counter of Fig. 2 at the end of the acquisition window T_{samp} can be expressed as:

$$q_{adc} = \lfloor n_{adc} \rfloor \tag{10}$$

$$n_{adc} = T_{samp} f_{PDM} = \frac{C_A}{C_B} \frac{G_m}{V_{th}} \frac{T_{samp}}{C_{int}} \Delta R_{sens} \tag{11}$$

IV. CMOS Integration and Experimental Results

Based on all the building blocks proposed in the previous sections, a channel test circuit has been fully integrated in 0.35μm CMOS technology, as shown in Fig. 8. The main design parameters for this channel implementation are: C_A=20pF, C_B={0.1,0.2,0.4,1}pF, K=10, N={1,11}, M=3, I_{fc}=100nA, I_{gm}=3μA, I_{max}=8μA, $C_{int,res}$={5,10}pF, V_{th}=120mV and T_{pulse}=725ns. The experimental results measured for the different digital configurations are plotted in Fig. 9 to Fig. 14 and summarized in Table I.

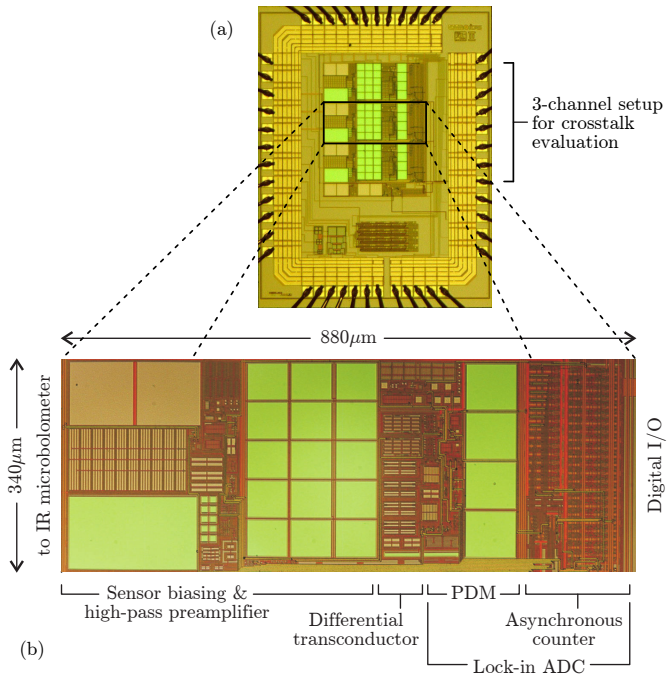

Figure 8. Microscope photography of the test chip (a) and the frontend channel module (b).

Firstly, the programmability of the sub-Hz high-pass pre-amplifier of Fig. 3 is studied. As it can be seen in Fig. 9, independent control of both gain and corner frequency is achieved, resulting in up to 16 possible transfer functions (not shown here for simplicity). In order to demonstrate the robustness of the pre-amplifier tuning scheme of Fig. 5, the same transfer functions are measured for all the available integrated prototype samples, returning the well aligned statistical results of Fig. 10.

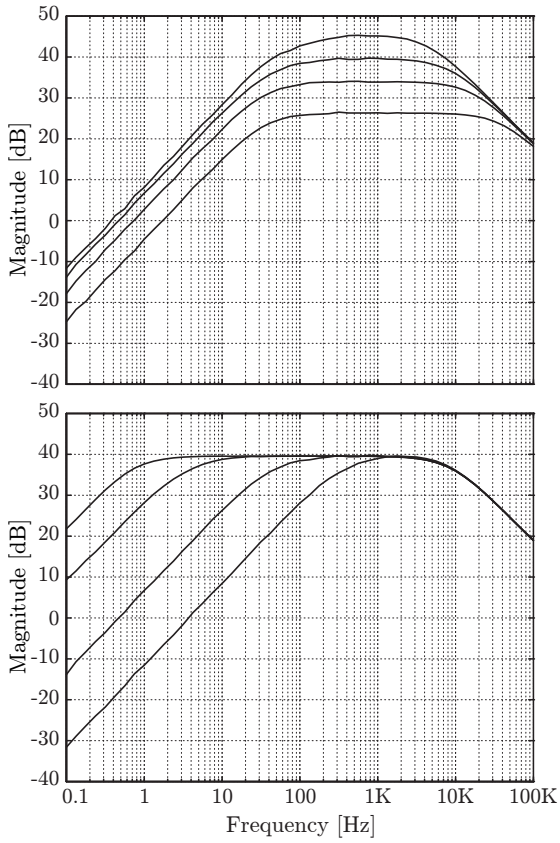

Figure 9. Experimental transfer function of the high-pass pre-amplifier stage for independent gain (top) and corner frequency (bottom) digital programming.

Still at the pre-amplifer block, the electronic noise contributions of this first stage are reported in Fig. 11, showing the typical flicker spectral roll-off. Around the target lock-in frequencies of the thermal LWIR sensors (typ. 10Hz), the equivalent input noise ($V_{sensneq}$) levels are close to 250nV$_{\text{rms}}$/$\sqrt{\text{Hz}}$. In practice, the estimation of the equivalent noise bandwidth in lock-in architectures is somehow difficult due to its strong dependence on the quality of the external lock-in signal (e.g. loop delay, overlapping and jitter specifications). Anyway, noise bandwidth values smaller than 1Hz should be reached easily, resulting in integrated noise levels below the spectral density of Fig. 11.

Concerning linearity of the pre-amplifier block, harmonic signal distortion results are presented in Fig. 12. Clearly, this first stage returns good enough linearity performance for the gas recognition application up to output levels of 300mV$_{\text{pp}}$. Hence, the system can deal with large variations of the incoming lock-in amplitude without saturating, and non-linearity can be then avoided by lowering the gain of the cascaded stages.

For the differential transconductance circuit of Fig. 6(a), its static transfer function is extracted in Fig. 13. The shape of the obtained curve matches with the theoretically predicted behavior of Fig. 6(b), with a remarkable linearity inside the programmed input range. Also, the fixed limiting knee

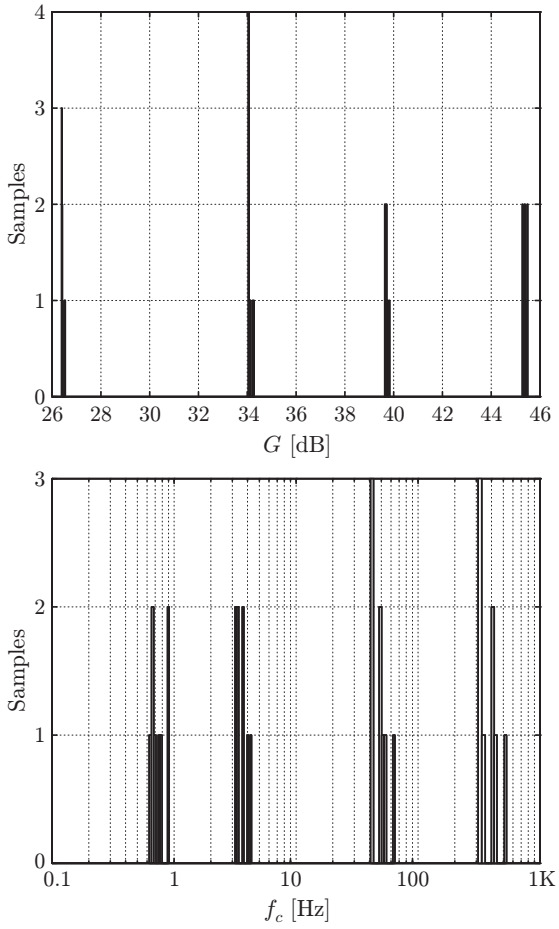

Figure 10. Experimental gain (top) and corner frequency (bottom) statistics of the pre-amplifier stage for the digital programming codes of Fig. 9.

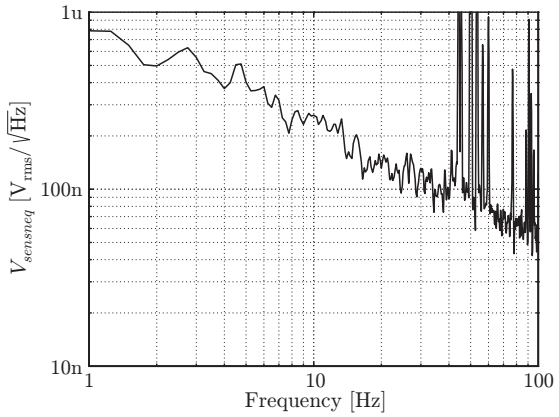

Figure 11. Experimental equivalent input spectral density noise of the pre-amplifier stage for maximum programmable gain.

threshold is correctly maintained for the different digital gain configurations.

Finally, the dynamic performance of the PDM modulator proposed in Fig. 7 is fully verified in Fig. 14. The resulting amplitude-to-frequency conversion curves show a linear response even for stream rates close to the hard limit imposed by the width of the reset pulse T_{pulse} itself defined in Section III-C.

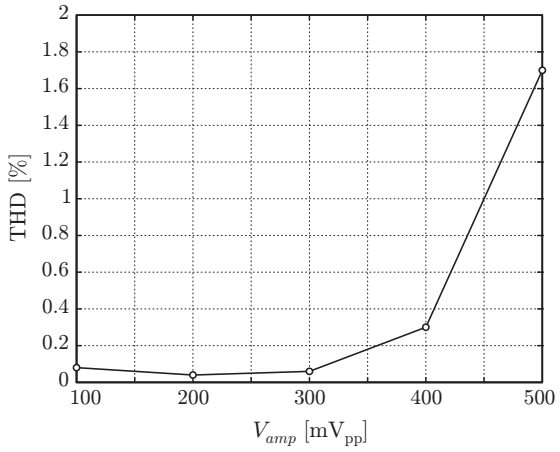

Figure 12. Experimental output total harmonic distortion of the pre-amplifier stage at 1kHz.

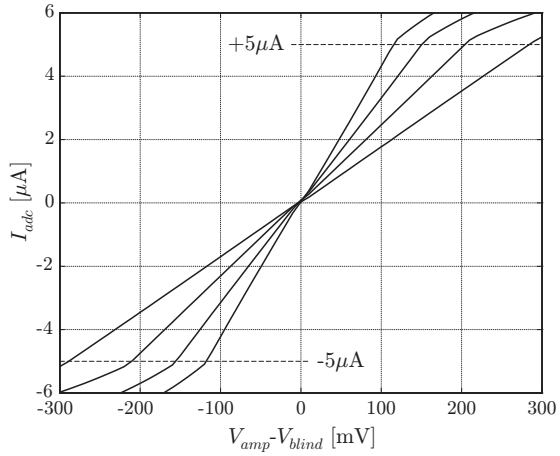

Figure 13. Experimental differential transfer function of the linearized transconductor stage for different transconductance digital programming.

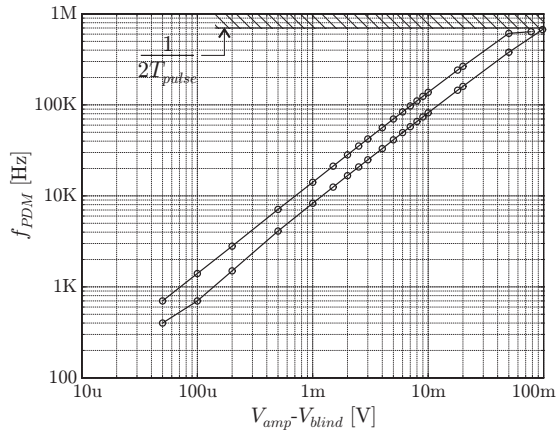

Figure 14. Experimental combined transfer function of the transconductor and PDM stages for different integration capacitor digital programming. T_{pulse} stands for the width of the reset pulses, as detailed in Section III-C.

According to Table I, no crosstalk has been experimentally observed between two physically adjacent channels. This fact reinforces the advantage of including dedicated local biasing circuits inside each channel in order to avoid sharing any

analog references.

Table I
EXPERIMENTAL RESULTS FOR THE FRONTEND CHANNEL.

Parameter	Value	Units
I_{sens}	1 to 10	μA
f_c	0.75±0.10 3.6±0.4 49±8 389±76	Hz
G	26±0.1 34±0.1 40±0.1 45±0.1	dB
G_m	18 25 36 45	μS
$1/C_{int}V_{th}$	1.7 0.8	Hz/pA
$V_{sensneq}$@10Hz	250	$nV_{rms}/\sqrt{Hz}$
THD V_{amp}<300mV$_{pp}$	<0.1	%
Crosstalk	<0.5	LSB
Supply voltage	3.3	V
Supply current	120	μA
Silicon area	0.3	mm^2

V. CONCLUSIONS

A low-power, compact and fully-integrated frontend channel has been presented for LWIR spectroscopic gas recognition. The proposed CMOS module includes input sensor biasing, sub-Hz high-pass filtering and pre-amplification, differential blind cancellation, and lock-in A/D conversion, all together with independent digital programmability. A 0.3mm^2 400μW channel prototype has been integrated in standard 0.35μm CMOS technology. Exhaustive experimental results are reported to prove the validity of the proposed circuits.

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