12.9 A 400-to-900 MHz Receiver with Dual-domain Harmonic Rejection Exploiting Adaptive Interference Cancellation

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Wideband direct-conversion harmonic-rejection (HR) receivers for software-defined radio aim to remove or relax the pre-mixer RF filters, which are inflexible, bulky and costly [1,2]. HR schemes derived from [3] are often used, but amplitude and phase mismatches limit HR to between 30 and 40dB [1,2]. A quick calculation shows that much more rejection is wanted: in order to bring harmonic responses down to the noise floor (e.g. -100dBm in 10MHz for 4dB NF), and cope with interferers between -40 and 0dBm, an HR of 60 to 100dB is needed. Also in terrestrial TV receivers and in applications like DVB-H with co-existence requirements with GSM/WLAN transmitters in a small telephone, high HR is needed.

In this work, an architecture aiming for >80dB HR is shown in Fig.12.9.1. It consists of an analog front-end followed by adaptive interference cancellation (AIC) in the digital domain. AIC is known for its ability to adapt to and mitigate unknown system non-idealities [4], e.g. gain and phase imbalances [5]. Due to its adaptivity it can achieve large improvements, provided the interference estimate is accurate [5]. To the authors' knowledge, they are the first to explore AIC for HR and previously presented simulation results in [6]. Here a new & different architecture and measured results with the RF part implemented in 65nm CMOS and the AIC in software are presented.

Figure 12.9.1 shows the architecture with analog HR-mixers followed by low-pass IF filters, A/D converters and digital AIC. To use highly linear switched passive mixers, it is necessary to address harmonic down-mixing (square-wave LO). To realize 3rd- and 5th-order HR, an 8-phase LO is used, adding weighted RF-signals to mimic a sine-wave LO, similar to [3]. However, instead of producing two differential signals (0°/180° and 90°/270°), the circuit produces four differential outputs (also 45°/225° and 135°/315°) to generate an interference estimate.

The antenna signal enters parallel power-to-current blocks with common-gate transistors for impedance matching and cross-coupled inverters for V-I conversion. The blocks are scaled as 2:3:2, an integer ratio approximating 1:√2:1 as needed for 3rd and 5th order HR [3]. Integer ratios are more accurately and easily implemented on chip and the error is compensated by the digital AIC. The blocks drive an 8-phase switching mixer, which produces four differential current-mode IF signals. Without RF voltage amplification, transimpedance amplifiers (TIAs) with low-pass RC-filters convert the IF-signals to voltage-mode, while also filtering out-of-band interferers [7].

The ADCs convert the filtered signals to ×0, ×45, ×90 and ×135, see Fig. 12.9.1. Two I/Q pairs are formed: $IQ_1 = x_0 + j \cdot x_{90}$ and $IQ_2 = x_{45} + j \cdot x_{135}$. Note that IQ_2 has a 45-degree phase shift with respect to IQ_1. An estimate of the interference, v(n), is formed by *rotating IQ_2 by -45 degrees* and subtracting the result from IQ_1, *which removes the desired signal* (see the simplified phasor diagram in Fig. 12.9.2). However, the 3rd- and 5th-harmonic image responses have a phase difference of 3×45°=135° and 5×45°=225° and are thus not canceled by the subtraction.

The AIC removes the interference, caused by the unwanted harmonic mixer responses, by aligning the interference estimate v(n) *in phase and amplitude* with the interference in the received signal, r(n). The alignment is performed by two single-tap FIR filters with complex coefficients w_1 and w_2. The aligned version of v(n) is subtracted from r(n) to obtain a cleaned-up signal e(n) (see Fig. 12.9.1). Coefficients w1 and w2 are adapted so that the cross-correlation between the cleaned signal e(n) and the interference estimate v(n) is minimized [5]. The AIC uses the normalized LMS [5] update rule, shown in Fig. 12.9.1, to adapt the coefficients each sample.

The AIC performance depends on the quality of the interference estimate v(n); the estimate must contain as little desired signal energy as possible [5]. Ideally, the interference-to-signal ratio (ISR) of v(n) is infinite. Each harmonic mixer response, e.g. the 3rd- and 5th-harmonic images, has a distinct solution of w_1 and w_2. In effect, the AIC is only able to cancel one harmonic response. In many receive conditions only a few very strong interferers exist and this is sufficient. The strongest cross-correlating harmonic image is cancelled. More than one interference estimate would be needed to reject multiple interferers. The performance of the analog HR scheme depends on amplitude and phase accuracy [3], and the same holds for a good interference estimate. To obtain good amplitude equality, the RF G_m blocks are time-multiplexed equally amongst the outputs by the mixer block (switches), while at IF the feedback resistors in the OPAMP feedback path ensure good matching. Accurate phase relations are obtained with an 8-stage shift register in a ring acting as a multi-phase clock generator with one master clock determining the output timing, resulting in a simulated 3σ phase error of only 0.34° at 0.8GHz.

The AIC was implemented in software and uses a commercial four-channel 14b ADC. The algorithm uses 16 real multiplies and 12 real adds per output sample. A sample rate of 5MHz was used. The AIC converges to its steady state within 1000 samples (measured), irrespective of the interference power levels.

To evaluate AIC performance, two RF sinusoidal signals are applied: 1) a desired signal with -66.1dBm; and 2) a 3rd-harmonic signal with -20.1dBm (SIR=-46dB at RF). Figure 12.9.3 shows that the interference estimate v(n) over the whole band is good, as its ISR is >52 dB, i.e. the "desired signal" is indeed suppressed. The SIR at the output e(n) of the AIC is at least 38dB, i.e. the total 3rd harmonic image rejection (HR3) is 46+38=84dB. This figure is a minimum because the residual interference is below the noise floor of the measurement equipment.

The analog HR and total HR for the 3rd-and 5th-harmonic images across 10 chips are shown in Fig. 12.9.4. Under the previously described RF conditions, the minimum total HR3 is 82.5dB. The minimum total HR5 is 81dB. Because the HR3 and HR5 are so high, we see that the even-order HR is now becoming the main limitation (worst-case rejection 64dB). The ISR, and therefore the quality, of the interference estimate is determined by the analog front-end, as mentioned previously, but also by the interference power. The lower the power, the worse the interference estimate and the lower the HR will be. Fortunately, less HR is needed in such a case. It is observed that the SIR at the AIC output is almost constant over interference power. To show that the AIC works with real-life modulated interferers, Fig. 12.9.5 shows the IF-spectra for an FM-modulated interferer. The AIC improves HR by about 40dB, limited by the noise floor and ground loop induced interference.

In addition to the HR, the other receiver performance data (see Fig. 12.9.6) is competitive with [1,2]. As this is the first HR concept with AIC, benchmarking is difficult. Clearly, compared to competing wideband analog HR-techniques, 2 additional ADCs and DSP are needed. It is expected that the cost of this overhead will reduce in the future, while the AIC achieves unprecedented HR, about 22dB better than the best results of which the authors are aware [7].

References:
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[4] B. Widrow, et al., "Adaptive Noise Cancelling: Principles and Applications", *IEEE Proceedings,* vol. 63, no. 12, pp. 1692-1716, Dec. 1975.
[5] S. Haykin, *Adaptive Filter Theory*, 4th ed., Prentice Hall, 2002.
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[7] Z. Ru, E. Klumperink, G. Wienk, and B. Nauta, "A Software-Defined Radio Receiver Architecture Robust to Out-of-Band Interference," *ISSCC Dig. Tech. Papers,* paper 12.8, Feb. 2009.
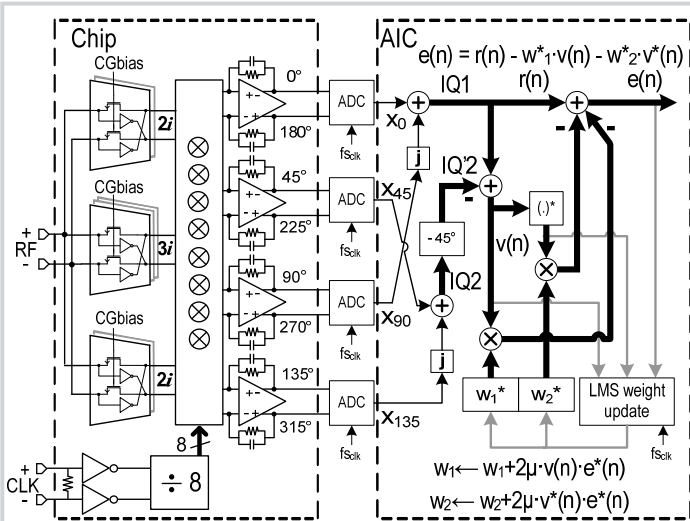
Figure 12.9.1: Dual-domain harmonic rejection (HR): 8-phase RF HR-mixing front-end & digital Adaptive Interference Cancellation (AIC) block.
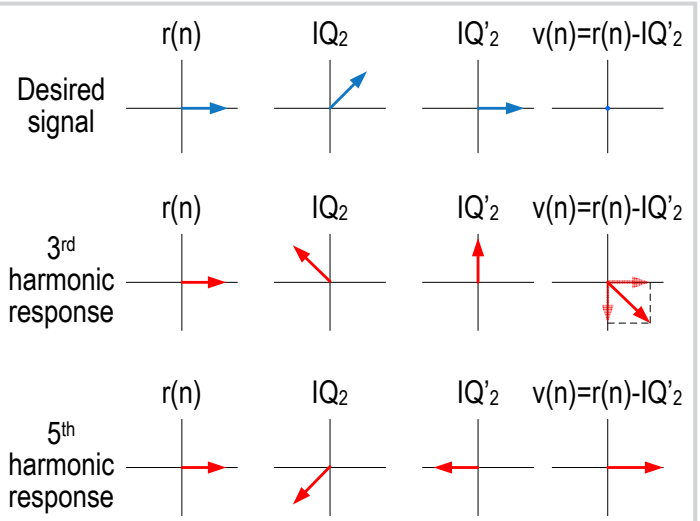

Figure 12.9.2: Interference estimation for the 3rd- and 5th-harmonic response cancelling the desired signal.
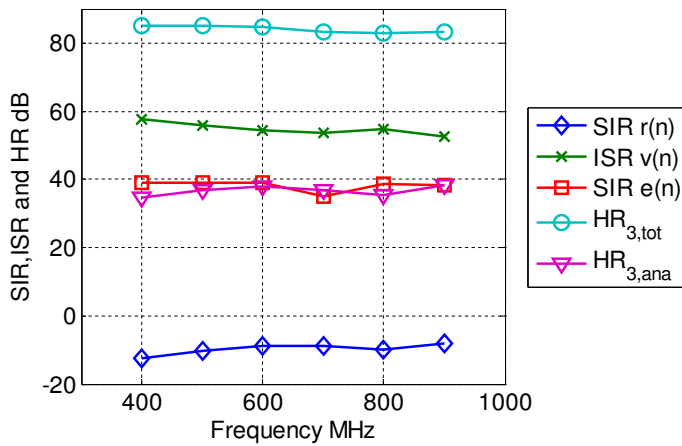

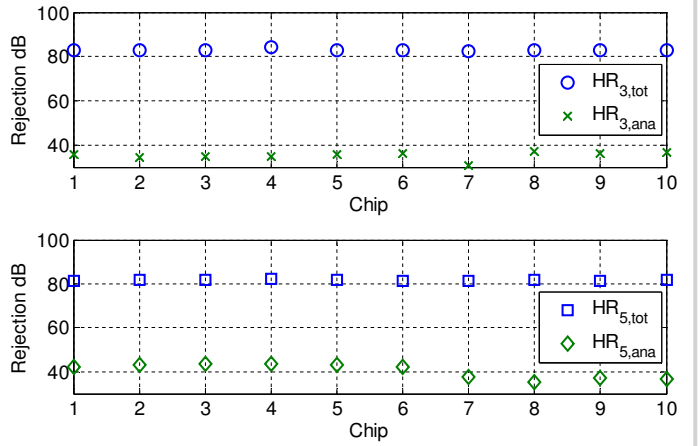**Figure 12.9.3: Measured SIR, ISR and HR (analog and total) of AIC signals.**

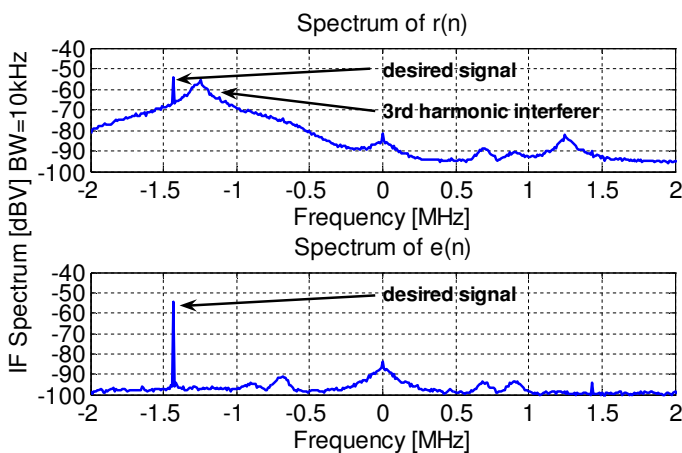**Figure 12.9.4: Measured HR3 and HR5 across 10 chips at an RF of 800MHz.**

Figure 12.9.5: HR3 test with modulated signals.

Gain (400 - 900 MHz)	27.6 +/- 0.2dB
Noise Figure (DSB)	4dB
1/f corner frequency	30kHz
IF bandwidth	22MHz
In-band IIP3 [1]	+6dBm
In-band IIP2 [2]	+52dBm
HR3 for -18 dBm interferer	>82.5dB
HR5 for -18 dBm interferer	>81dB
Front-end without clock : Clock generator:	28mA @ 1.2V 17mA @ f_{LO} = 900MHz 8mA @ f_{LO} = 400MHz

1 IIP3 tested with two tones at 803MHz & 803.01MHz
2 IIP2 tested with two tones at 803MHz & 806.01MHz

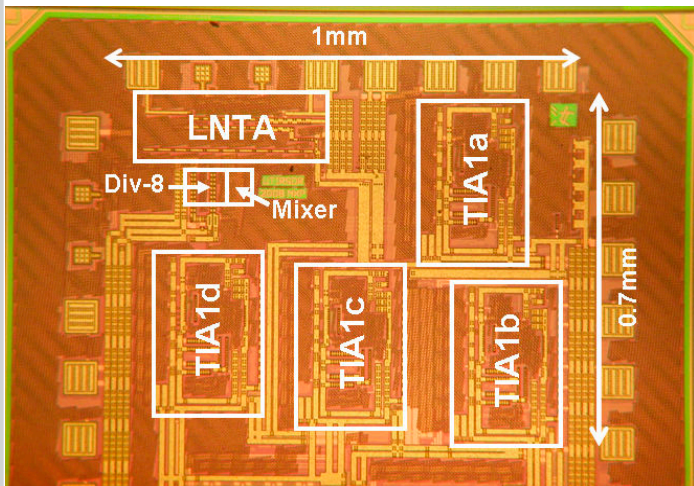**Figure 12.9.6: Performance figures of the analog front-end.**

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Figure 12.9.7: Micrograph of the chip fabricated in 65nm CMOS.