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A 48 GHz Fundamental Frequency PLL with Quadrature Clock Generation for 60 GHz Transceiver

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Abstract: This paper presents a design of a 48 GHz CMOS phase-locked loop (PLL) for 60 GHz millimeter-wave (mmWave) communication systems. For the sliding intermediate frequency (sliding-IF) transceiver applications, a fundamental frequency PLL with quadrature clock generation scheme is proposed. Specifically, with an implicit capacitive-bridged shunt peaking network, a second order harmonic filtering technique is realized in the voltage control oscillator (VCO) to broaden the bandpass response, thereby avoiding the complex common-mode resonant tank calibration and improving the phase noise performance. A robust current mode logic (CML) static frequency divider topology is adopted to realize the prescaler and to generate the quadrature clock. With the capacitive-bridged shunt peaking load and robust biasing circuit, the static frequency divider locking range and high frequency performance is improved and its reliability is enhanced over the PVT corners. To improve the image suppression ratio of the transceiver, a quadrature clock phase calibration scheme is proposed and verified. Fabricated in a 65 nm CMOS process, the PLL occupies a core area of 800 μm × 950 μm. Over the frequency range of 45.2 to 52.6 GHz, the measured PLL in-band phase noise PLL is better than −90 dBc/Hz@100 KHz offset, and its jitter is less than 155 fs. Moreover, the reference spur is less than −60 dBc/Hz.

Keywords: phase-locked loop; 60 GHz; voltage control oscillator; frequency divider; quadrature phase calibration; CMOS

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1. Introduction

With the wide bandwidth nature, the unlicensed 60 GHz band is considered as a solution for the several short distance and high data rate applications, such as wireless backhaul, augmented reality (AR), and virtual reality (VR). Benefiting from the aggressive scaling down of a CMOS transistor, several 60 GHz transceivers for wireless communication and radar sensing have been realized [1–5]. For above applications, the higher order modulation scheme, e.g., 16QAM, is required to achieve the high throughput rate. From the implementation perspective, due to very high operating frequency, the challenges are still imposed on the high-frequency transceiver building blocks. Particularly, as a key building block of the 60 GHz transceiver, the PLL is required with stringent phase noise, spur, and tuning range specifications.

In the past few years, several PLLs for mmWave applications have been reported. In [6], a 60 GHz chipset with 22.5–26.23 GHz integrated PLL, which achieved a phase noise of −92 dBc/Hz at 1 MHz offset, was realized with 0.13 μm BiCMOS process. In [7,8], all-digital mmWave PLL (ADPLL) was realized, but its in-band phase noise performance was limited to around −85 dBc/Hz. To improve the phase noise performance and attenuate the parasitic effect on the circuit operating frequency, frequency multiplication techniques, such as the injection locked oscillator [9,10], harmonic extraction [11], or push-push operation [12], were used. In [9], the injection locked oscillator was locked to 10th and 11th

harmonics of the reference, obtaining the 20 GHz and 22 GHz quadrature clock with 132 mW power consumption. In [10], based on 20 GHz PLL and a 60 GHz sub-harmonic quadrature injection locked oscillator, a 60 GHz frequency synthesizer was realized in a 65 nm CMOS, achieving a phase noise of −96 and −117 dBc/Hz at 1 MHz and 10 MHz offset, respectively, at the cost of a large power consumption of the calibration loop. In [11], a 52 GHz frequency synthesizer was realized with VCO-doubler co-design, extracting the inherent 2nd harmonics of the differential oscillator. To realize differential output signal, the common gate and common source amplifiers were needed. It should be noticed that frequency multiplication techniques are typically sensitive to PVT issues and relative complex calibration schemes are needed. In [13], a 40 GHz mmWave sub-sampling PLL was realized with a 65 nm CMOS process, showing the advantages of low power consumption and low in-band phase noise performance. However, due to the narrow capture range of the sub-sampling, the sub-sampling PLL was sensitive to external disturbance and needed an extra control loop [14]. As an alternative approach, the reference sampling PLL offers a low in-band phase noise and a low spur performance. In [15], based on the reference sampling and injection-locked VCO (ILO) topology, a two stage 35 GHz mmWave frequency synthesizer was realized with a 45 nm CMOS process, achieving 251 fs rms jitter. To improve the working reliability, a digital frequency tracking loop was proposed. Also with the reference sampling topology, Ref. [16] proposed a reference oversampling digital PLL at low frequency. With the reference oversampling, the noise contribution from the loop components were suppressed, improving the in-band phase noise and making it possible to realize wide bandwidth and better oscillator noise filtering. Fabricated in a 28 nm CMOS, this PLL achieved 67.1 fs rms jitter at 4 GHz.

As two essential circuits, the VCO and high-speed frequency divider played important roles in determining the PLL phase noise and tuning range performance. To minimize the flicker noise up-conversion and improve the phase noise performance, the second harmonic filtering technique was introduced in a 1 GHz VCO [17]. An additional LC filter was needed, increasing the chip area occupation. In [18], the dual-core and multi-core LC tank schemes were proposed in a 35 GHz VCO, with the penalty of relatively large area and power consumption. Recently, the implicit common-mode resonance VCO topology was proposed without using any additional inductor. By introducing a common-mode resonance with common return path inductor, [19] proposed a 3 GHz VCO with an implicit common-mode resonance. With the common-mode resonance, high common-mode impedance was realized, increasing the VCO phase noise performance. A tunable common-mode capacitor array was intentionally employed in the VCO to achieve common-mode resonance at the second order harmonic frequency, with the penalty of increased VCO calibration complexity. In [20], together with explicit common-mode return path and embedded decoupled capacitor, the implicit second harmonic resonance was realized in a 30 GHz VCO, minimizing the flicker noise up-conversion and improving the phase noise performance. Moreover, the common-mode and differential-mode tank had a good frequency tracking with each other, improving the phase noise over the tuning range. To achieve high operating frequency, the injection-locked frequency dividers (ILFDs) can be used for mmWave PLL, but it is very sensitive to PVT corners [21,22]. In [23], as an alternative approach, to achieve fine frequency resolution, a 6.48 GHz delta-sigma fractional-N frequency divider was designed for 60 GHz transceiver with a 0.18-µm BiCMOS process. Note that to support high order quadrature amplitude modulation (QAM) modulation, the quadrature clock is needed, which has been realized with quadrature injection locked oscillator (QILO) [24] and poly-phase filters (PPF) [25]. For the QILO scheme, a complex calibration is required to ensure accurate phase performance and correct working, increasing the power consumption. For the PPF scheme, typically two or three stages are needed to achieve wideband PPF operation and accurate quadrature phase, therefore its insertion loss is relatively high.

To address above issues, targeting at the sliding-IF 60 GHz transceiver applications, a robust 48 GHz fundamental frequency PLL with 12 GHz quadrature clock generation scheme is proposed in this paper. Specifically, by introducing an implicit capacitive-

bridged shunt peaking network, a broadband second order harmonic filter is realized in the VCO, thereby relaxing its common-mode resonant tank calibration issues and improving the phase noise performance. Moreover, with the benefits of the broadband capacitive-bridged shunt peaking load, a compact wide-locking range CML static divider is realized. To improve its reliability over the PVT corners, a feasible biasing scheme is employed. Different from QILO and PPF solutions, the 12 GHz quadrature clock is realized with the static CML frequency divider in this paper. To improve the image rejection ratio (IRR) performance, a phase calibration scheme is proposed and verified. Fabricated in a 65 nm CMOS process, the PLL achieves a measured in-band phase noise of better than −90 dBc/Hz @100 KHz offset from 45.2 to 52.6 GHz. Moreover, its jitter and reference spur are less than 155 fs and −60 dBc/Hz, respectively.

This paper is organized as follows. Section 2 briefly introduces proposed PLL topology for the 60 GHz sliding-IF transceiver. In Section 3, the design of the proposed mmWave VCO with a capacitive-bridged shunt peaking common-mode filtering technique is presented. Section 4 describes the implementation of a robust CML high speed frequency divider. Then, in Section 5, the quadrature clock phase calibration diagram is shown. In Section 6, the measurement results of the PLL are given. Finally, a summary is given in conclusion.

2. Proposed PLL Topology for the 60 GHz Sliding-IF Transceiver

Figure 1 shows a sliding-IF transceiver architecture [26,27]. To support the operation of the transceiver, a low phase noise integer-N fundamental frequency PLL topology is used, and the quadrature clock generation is also needed for the quadrature modulation/demodulation [27,28]. Compared with the direct conversion transceiver, the tuning range and operating frequency of the VCO and frequency dividers can be greatly reduced. Moreover, the pulling effect of the VCO due to strong interference from the power amplifier (PA) can be attenuated. As the operating frequency of the quadrature mixer is 12 GHz, it is also easier to calibrate quadrature clock to achieve better image injection performance.

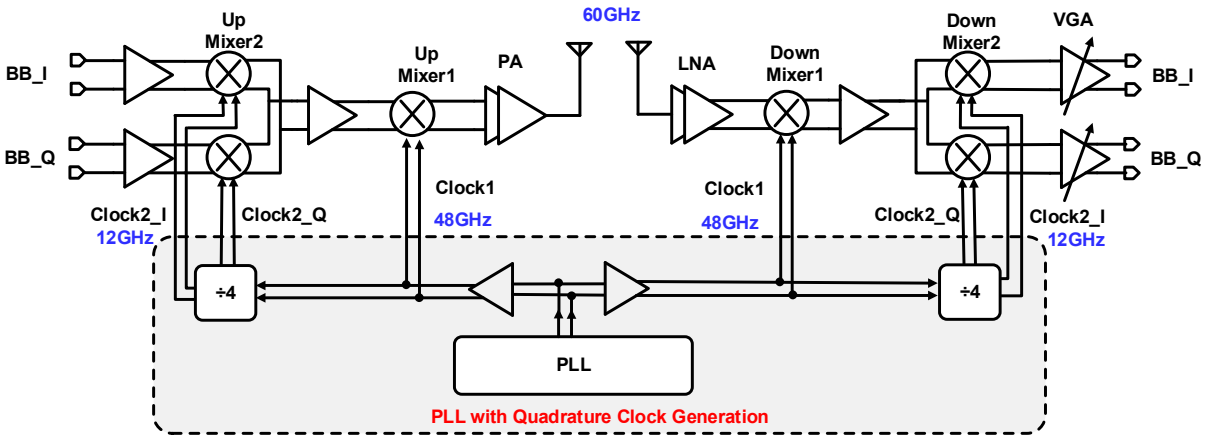

Figure 1. Block diagram of the sliding-IF 60 GHz transceiver.

Figure 2 shows the simplified block diagram of the PLL, in which the fundamental VCO is working at 48 GHz. By cascading two out-of-loop divide-by-2 frequency dividers, a divide-by-4 frequency divider is realized to generate the 12 GHz quadrature clock. Together with the programmable multi-modulus dividers (MMD), the in-loop divide-by-4 frequency divider divides the VCO output frequency further and compares with the 108 MHz reference clock through the phase/frequency detector (PFD). In the following sections, the design issues of the VCO and high-speed frequency divider will be discussed.

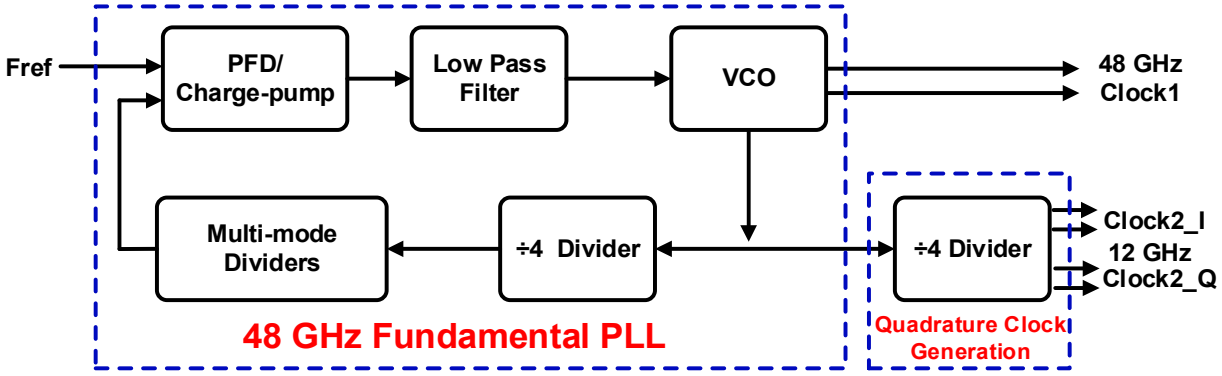

Figure 2. The proposed PLL and quadrature clock generation circuit.

3. VCO Implementation

Figure 3 shows the implemented cross-coupled VCO topology. A 4-bit binary-weighted switched capacitor array is deployed to enhance the tank quality factor and to reduce K_{VCO}, while a varactor is used to fulfill the frequency gaps between the 16 discrete frequency tuning curves. The differential resonant tank consists of the NMOS cross-coupled pair $M_{1,2}$, the differential inductor L_{DM}, switch capacitor C_{SW}, varactor C_{VAR}, and shunt capacitor C_{SP}. Accordingly, its differential resonant frequency is given by:

$$f_{osc} = \frac{1}{2\pi\sqrt{L_{DM}(C_{SW} + C_{VAR} + C_{SP})}} \quad (1)$$

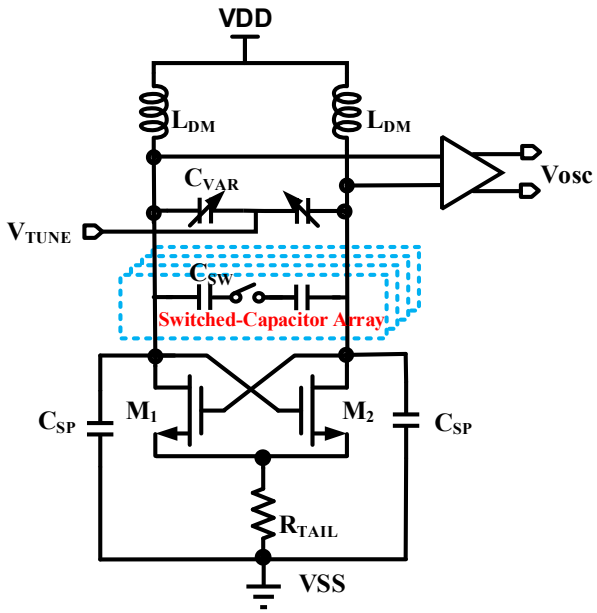

Figure 3. Schematic of the implemented VCO.

In this design, to increase the VCO phase noise performance, an implicit common-mode capacitive-bridged shunt peaking filter is realized by introducing tail resistor R_{TAIL} and shunt capacitor C_{SP}. As will be discussed shortly, by taking the advantage of the broadband characteristics of the capacitive-bridged shunt peaking network, a broadband common-mode resonance network is realized.

To illustrate the working mechanism of the implicit common-mode capacitive-bridged shunt peaking filter, Figure 4 shows the common-mode loop of the VCO. As indicated, the common-mode second harmonics current loop is composed of transistor $M_{1,2}$, the

common-mode tank inductor L_{CM}, the shunt capacitor C_{SP}, tail resistor R_{TAIL}, and the switched-capacitor parasitic.

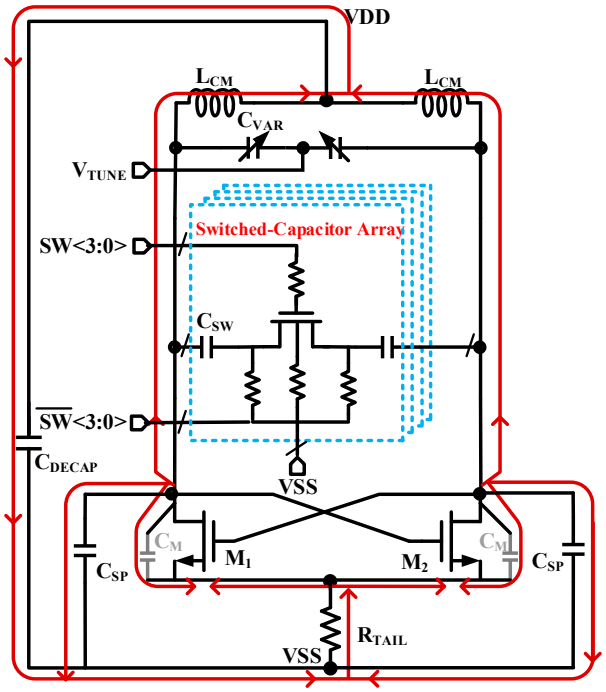

Figure 4. The common-mode loop of the VCO.

As an important part of the common-mode loop, the switch capacitor parasitic capacitance has an important effect. To illustrate this, Figure 5 shows the realized switched capacitor structure and the parasitics are highlighted. In this design, the triple-well CMOS process is used, and the resistors R_G, R_D, and R_B with high value are inserted to bias the switch. Note that R_G helps to reduce the parasitic capacitance between the switch gate and the switch control lines, while R_D is used to block the switch capacitors C_{SW}. Moreover, R_B is used to isolate the buck parasitic capacitor C_B from the ground VSS. In this way, the parasitic capacitance of the switched capacitors array is minimized in the common-mode loop, irrespective of whether the switch state is on or off.

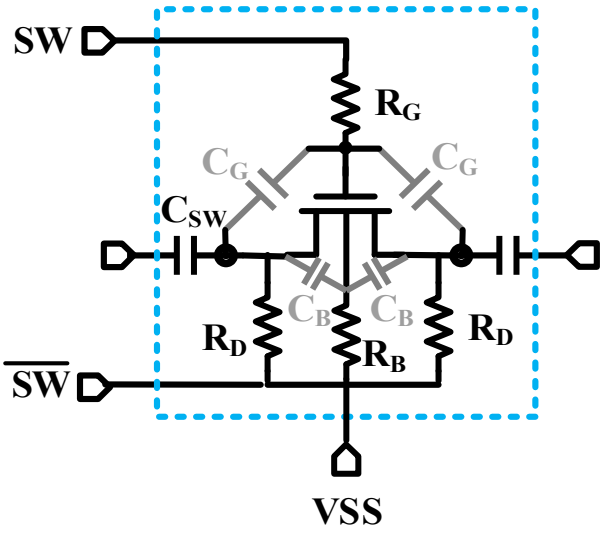

Figure 5. The switched capacitor structures.

For calculation convenience, Figure 6 shows the simplified common-mode topology. Note that together with the transistor $M_{1,2}$ parasitic capacitor C_M, an implicit capacitive-bridged shunt peaking network [29] is realized.

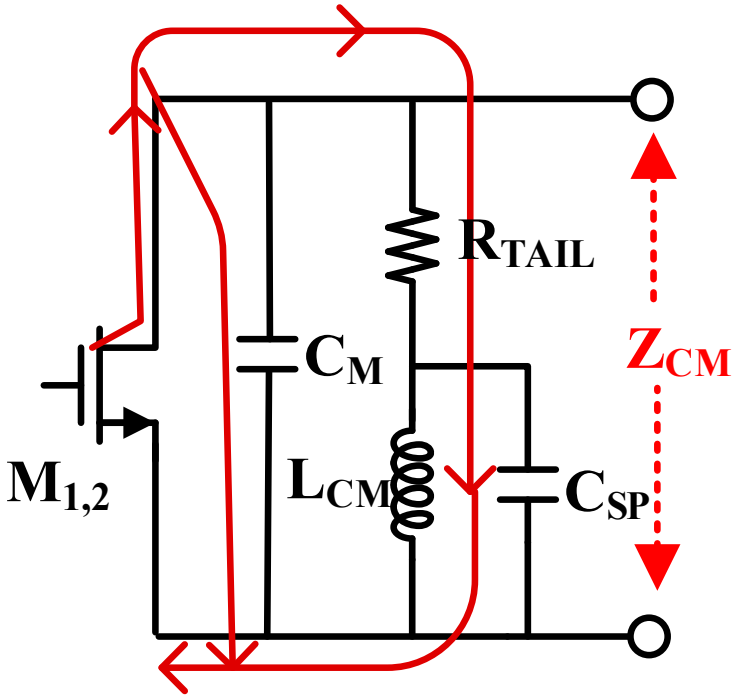

Figure 6. The implicit capacitive-bridged shunt peaking filtering network.

Accordingly, the common mode impedance between the cross-coupled pair $M_{1,2}$ drain and source terminals, Z_{CM}, can be derived as

$$Z_{CM} = \frac{R_{TAIL}(1 + sL_{CM}/R_{TAIL} + s^2 L_{CM}C_{SP})}{s^3 R_{TAIL}L_{CM}C_{SP}C_M + s^2 L_{CM}(C_M + C_{SP}) + sC_M R_{TAIL} + 1} \quad (2)$$

With calculation, it is found that the common mode impedance Z_{CM} has 3 poles and 2 zeros. By carefully choosing the R_{TAIL} and C_{SP} value, the common-mode impedance Z_{CM} can be optimized. For illustration, Figure 7a shows the simulated fundamental differential mode impedance Z_{DM}, and the second harmonic common-mode impedance Z_{CM}. The dashed lines show the fundamental differential mode impedance Z_{DM} across the tuning range from 45 to 52.5 GHz. In contrast, the solid line indicates common-mode impedance Z_{CM}. As indicated, Z_{CM} is larger than 70 Ohm over 90 to 105 GHz, which is the second harmonic frequency of the fundamental frequency. In other words, a broadband high impedance is realized over large frequency range, relaxing the calibration requirements of the common-mode loop over a wide tuning range. For performance comparison, Figure 7b shows the simulated phase noise of the VCO with and without the proposed implicit second harmonic filter. Clearly, due to broadband high impedance in the common mode loop, the flicker noise performance is improved.

In this design, the tail resistor is also optimized to set the overdrive voltage for the cross-coupled transistors to be around 0.65 V, which is a near-optimal biasing voltage for the transistor in terms of speed, g_m efficiency, and noise performance [30]. By tuning the varactor control voltage Vtune from 0.5 to 1.5 V, Figure 8 shows the simulation results of the VCO output frequency tuning curve. As indicated, the simulated tuning range is from 45.2 to 52.6 GHz. Note that with the overlapping of 16 discrete tuning curves, a continuous frequency coverage over the tuning range can be guaranteed.

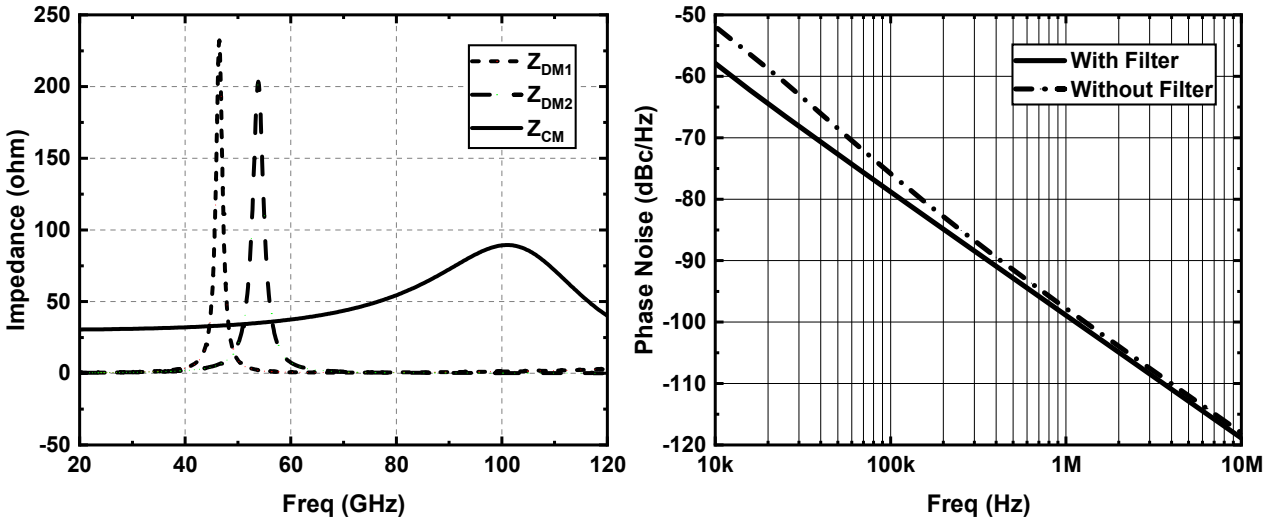

Figure 7. Simulated common-mode and differential-mode impedance and phase noise of the VCO: (**a**) The fundamental and second harmonic impedances over with the tuning range; (**b**) the simulated phase noise with and without the implicit second harmonic filter.

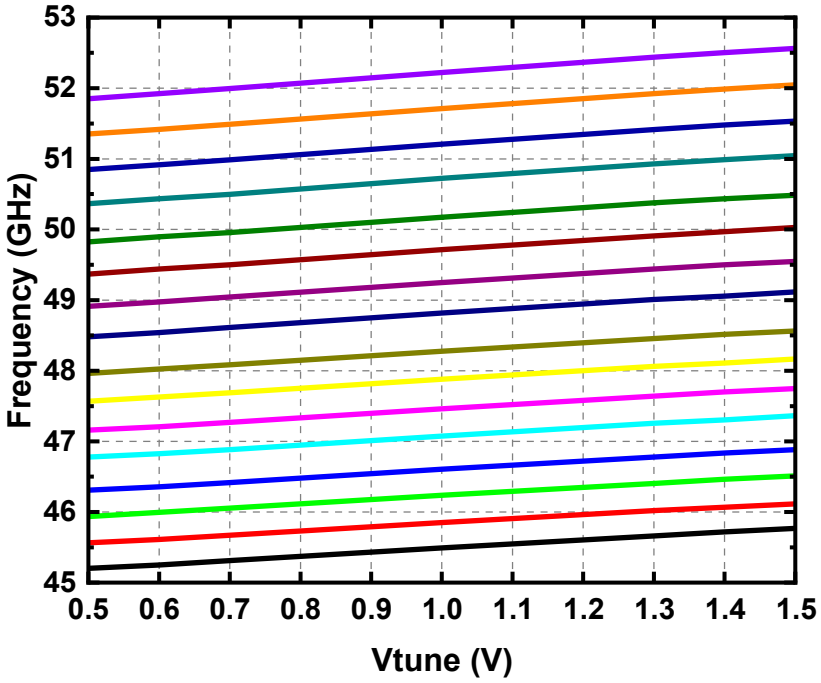

Figure 8. Simulated frequency tuning curve of VCO.

The simulated performance of the VCO is compared with several publication results as shown in Table 1. Compared with >10 GHz oscillators, the proposed work yields the smallest area occupation and achieves the best FOM of −186.4 dBc/Hz, which is a widely accepted figure of merit and is defined as follows:

$$FOM = L\{\Delta f\} - 20log(f_O/\Delta f) + 10log(P_{DC}/1mW) \quad (3)$$

Table 1. VCO performance summary and comparison.

References	[19]	[20]	[18]	This Work
	65 nm	28 nm	65 nm	65 nm
Oscillation Frequency (GHz)	51.9–67.3	27.3–31.2	28.6–36.2	45.2–52.6
Tuning Range (GHz)	16.4	14	23.5	15.1
PN@1MHz (dBc/Hz)	−80	−106	−103	−99
Power consumption (mW)	5.4	11.6	4.6	5
FOM	−168	−184	−186.2	−186.4
Core Aera (mm^2)	0.03	0.064	0.12	0.018

4. Frequency Dividers Implementation

As mentioned before, the frequency divider should operate at high frequencies with very large locking bandwidth in mmWave PLL. To address above mentioned PVT sensitivity issues of ILFD [21,22], it is highly desired to use static CML frequency divider in practice with its benefit of robustness over large locking range [31].

Based on the above consideration, the CML static frequency divider topology, as shown in Figure 9, is used in this design. As indicated, the divider consists of 2 D-latches with the capacitive-bridged shunt peaking load.

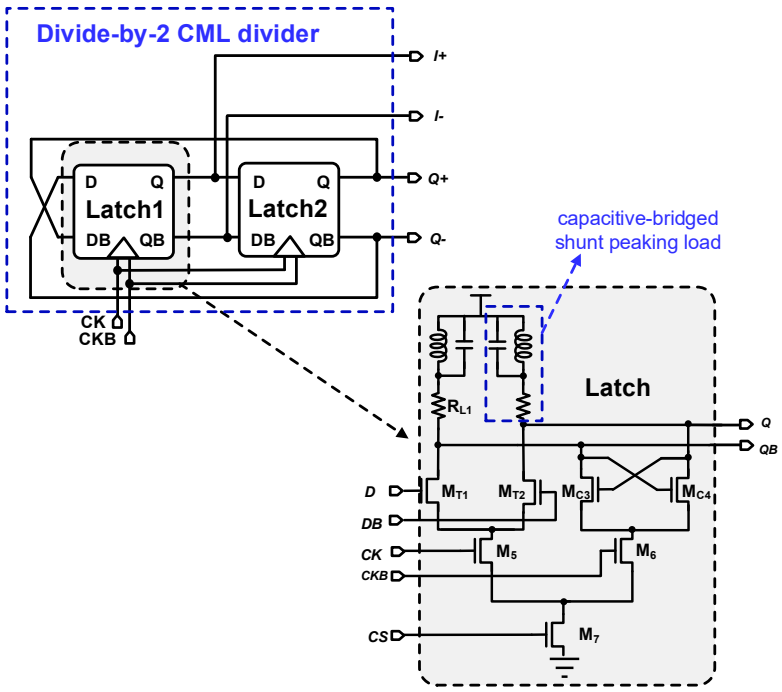

Figure 9. Proposed CML static frequency divider structure.

To improve the operating speed and bandwidth, the stack inductor is used as the load of the frequency divider. As shown in Figure 10, this stack inductor is realized with multiple coupled metal layers, and the space between the metal turns of the inductor is minimized. In this way, the inductor value is increased with magnetic coupling, reducing the inductor area substantially and introducing extra parasitic capacitor between the metal lines. By absorbing the parasitic capacitor in the inductor, a kind of capacitive-bridged shunt peaking network is realized. With simulations shown in the following sections, benefiting from the inductor and extra parasitic capacitor, the working speed and bandwidth of the frequency divider is improved substantially.

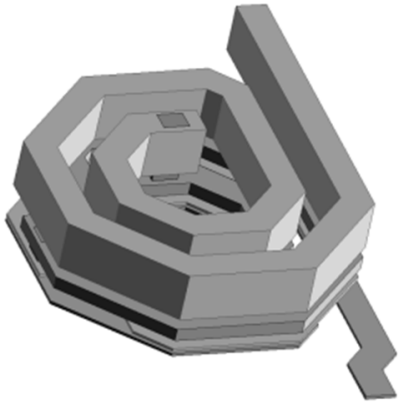

Figure 10. Implementation of the stack inductor.

To optimize the divider performance and to ensure the robustness, the working mechanism of the D-latch flip-flop is discussed briefly as below. As indicated in Figure 9, the D-latch flip-flop consists of pre-amplifier transistors and cross-coupled transistors. When the input clock amplitude is zero, self-oscillation will be observed if the pre-amplifier and the cross-coupled pair have sufficient gain. Typically, to ensure correct operation of the divider with high power efficiency, it is better to set the self-oscillation frequency around the center of the input frequencies.

For calculation convenience, Figure 11 shows a simplified small signal model of the latch. In this small signal model, the cross-coupled pair produces a negative resistance, and it is controlled by its complementary output $-V_{\mathrm{O}}$.

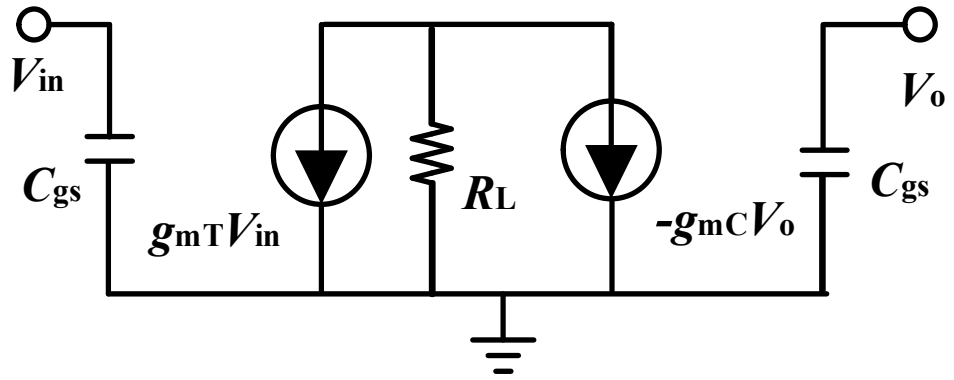

Figure 11. The small-signal model of the D-latch.

Accordingly, the small signal gain A_{FD} of the latch can be obtained as below

$$A_{\mathrm{FD}} = \frac{V_0}{V_{in}} = -\frac{g_{mT}R_{\mathrm{L}}}{1 - g_{mC}R_{\mathrm{L}}} \tag{4}$$

where g_{mT} is the transconductance of the transistors $\mathrm{M_{T1,T2}}$, and g_{mC} is the transconductance of the cross-coupled transistors $\mathrm{M_{T3,T4}}$. R_{L} is the resistive load of the latch. Apparently, A_{FD} is determined both by $g_{mT}R_{\mathrm{L}}$ and $g_{mC}R_{\mathrm{L}}$ product. To obtain a constant A_{FD} value over different PVT corners, a constant g_mR product biasing circuit is proposed, as shown in the left part of Figure 12. As will be discussed shortly, by using this biasing circuit, both $g_{mT}R_{\mathrm{L}}$ and $g_{mC}R_{\mathrm{L}}$ product can be kept constant over PVT corners.

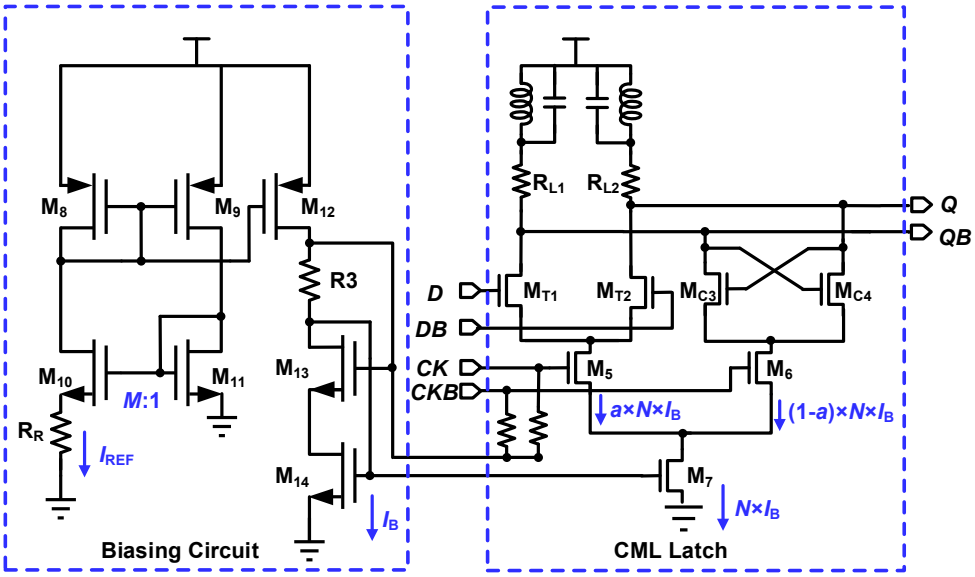

Figure 12. The proposed biasing circuit of the frequency divider.

The product of transconductance of M_{10} and resistor R_R in the biasing circuit is expressed as

$$g_{m10}R_R = 2 \times (1 - \sqrt{\frac{(W/L)_{11}}{(W/L)_{10}}}) \tag{5}$$

Since M_8, M_9, and M_{12} have the same size, I_B has the same value as I_{REF}. In this design, the size ratio of transistor M_{14} and M_7 is 1:N, so

$$I_{M7} = N \times I_{REF} \tag{6}$$

Given the size ratio of M5 and M6 is $a : (1 - a)$, their currents are

$$I_{M5} = aN \times I_{REF} \tag{7}$$

$$I_{M6} = (1 - a)N \times I_{REF} \tag{8}$$

Consequently,

$$I_{MT1} = I_{MT2} = \frac{a}{2}N \times I_{REF} \tag{9}$$

$$I_{MT3} = I_{MT4} = \frac{(1 - a)}{2}N \times I_{REF} \tag{10}$$

In this design, the size ratio of M_{10} and M_{T1} is set to be $1 : aN$, then

$$g_{mT1} = \sqrt{2\mu_n C_{ox}(W/L)_{11} \times I_{MT1}} = \sqrt{2\mu_n C_{ox} aN (W/L)_{10} \times (\frac{1}{2}aN \times I_{REF})} = \frac{aN}{\sqrt{2}}g_{m10} \tag{11}$$

In the same way,

$$g_{mT3} = \frac{(1 - a)N}{\sqrt{2}}g_{m10} \tag{12}$$

As a result,

$$g_{mT1}R_L = \frac{aN}{\sqrt{2}}\frac{R_L}{R_R}g_{m10}R_R = \sqrt{2}aN\frac{R_L}{R_R}(1 - \sqrt{\frac{(W/L)_{11}}{(W/L)_{10}}}) \tag{13}$$

$$g_{mT3}R_L = \frac{(1-a)N}{\sqrt{2}}\frac{R_L}{R_R}g_{m10}R_R = \sqrt{2}(1-a)N\frac{R_L}{R_R}(1-\sqrt{\frac{(W/L)_{11}}{(W/L)_{10}}}) \quad (14)$$

As long as R_L and R_R are of the same type, according to Equations (4), (13) and (14), a very constant gain of the divider can be obtained over PVT corners by utilizing the proposed constant biasing circuit. To illustrate effect of the above biasing circuit, Figure 13 shows the simulated sensitivity curve of the 48 GHz divider-by-2 frequency divider under three temperature and process conditions. As indicated, the sensitivity curves are close to each other, and the locking range of the divider fully covers the VCO tuning range with 0 dBm input power under these three PVT cases.

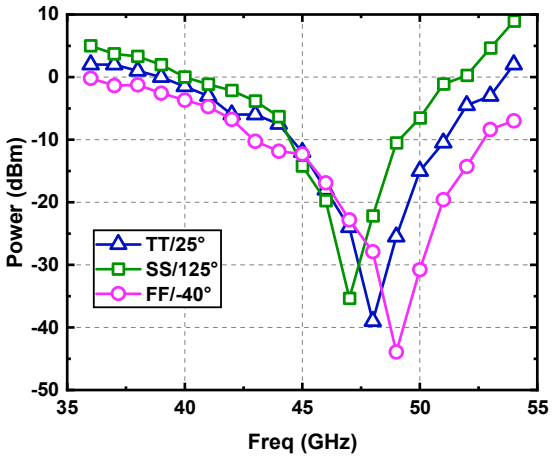

Figure 13. Simulated sensitivity curves of the frequency divider.

The simulated performance of the proposed frequency divider is summarized in Table 2 and compared with several published mmWave frequency dividers. As indicated, the proposed design has the widest locking range among the publication results with a compact layout size. Note that the wide locking range is acquired without extra complex sub-bands tuning.

Table 2. Frequency divider performance summary and comparison.

References	[21]	[22]	[31]	This Work
Technology	65 nm	130 nm	65 nm	65 nm
Architecture	ILFD	ILFD	ILFD	CML
Operation Frequency (GHz)	60.8–67	49.8–62.0	53.9–54.2	38–54
Locking Range	6.2	12.2	0.8	16
Power Consumption (mW)	6.3	10.8	21	14
Core Area (mm^2)	0.058	<0.32	0.005	0.008
Sub-bands Tuning Needed	Yes	No	No	No

5. Quadrature Clock Calibration

For 60 GHz millimeter wave communication, the in-phase and quadrature (I/Q) signal imbalance performance is very critical. In general, the I/Q signal imbalance is measured by the IRR, which is defined as below

$$IRR = \frac{\alpha^2 + 2\alpha\cos\Delta\theta + 1}{\alpha^2 - 2\alpha\cos\Delta\theta + 1} \quad (15)$$

where α is the signal amplitude error, and it is defined as the ratio of I and Q signal output amplitude, θ the signal phase error. For the ideal matching, IRR tends to be ideal.

However, there are some mismatches in reality within the quadrature mixer, worsening the IRR performance. Improving the IRR performance calls for the quadrature clock phase calibration.

As mentioned in Section 2, the 12 GHz 4-phases quadrature clock is generated with the out-of-loop divide-by-4 CML frequency divider. As shown in Figure 14, the quadrature clock phase error calibration is realized by tuning the phase delay of two 12 GHz output clocks. As indicated, it consists of the phase tuners and limiting amplifiers. The biasing current of the phase tuner is adjusted to change the charging and discharging speed of its output load capacitor, thereby changing the phase of the output signal with 4-bit digital control bits. With the above different phase setting states, the output amplitude of the phase tuner is constrained to be constant by the limiting amplifier, relaxing the conversion gain variation of the mixer.

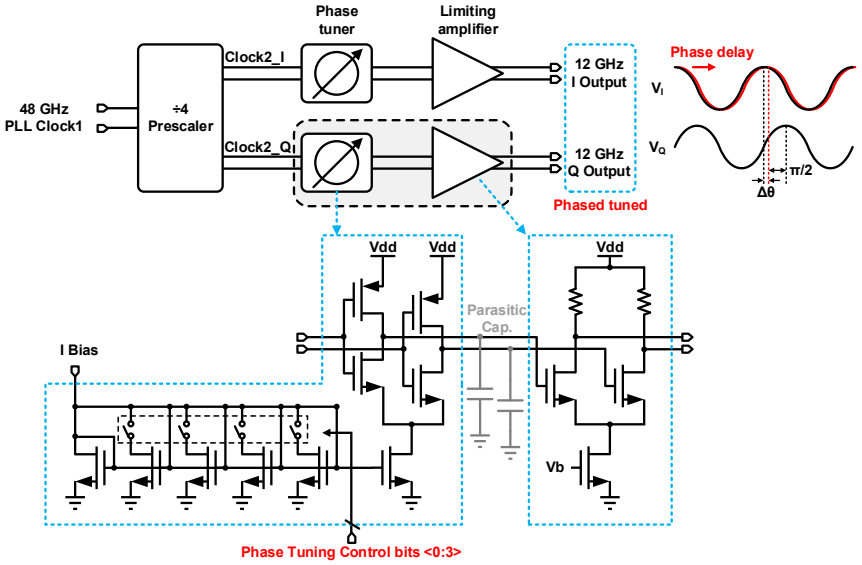

Figure 14. Diagram of the phase tuning circuits.

Figure 15 shows the simulated phase delay with respect to the control bits. As indicated, the phase tuning range is about 6° with a 0.4° step, thereby making it possible to realize good IRR performance.

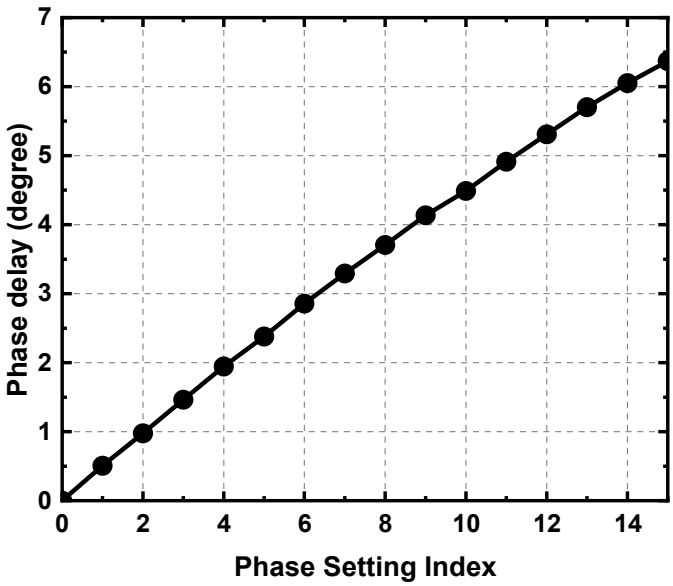

Figure 15. Phase delay with respect to the control bits.

6. Measurement Results

Fabricated in a 65 nm CMOS process, Figure 16 shows the 60 GHz transceiver chip photograph. As indicated, the core chip area of the PLL is 800 µm × 950 µm, which integrated the 48 GHz PLL and quadrature clock generation circuits.

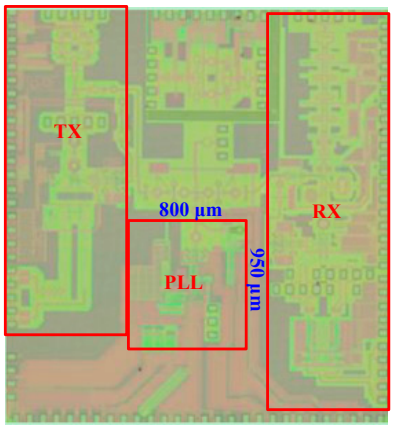

Figure 16. Photography of the 60 GHz CMOS transceiver with the integrated PLL.

With a 108 MHz reference clock, by tuning division ratio of the MMD circuit, four typical clock frequencies (46.656, 48.384, 50.112, and 51.840 GHz) are generated, which correspond to four channel center frequencies of the 60 GHz band. Figure 17 shows the measured phase noise of these four frequencies. Clearly, benefiting from the above-mentioned design techniques of the VCO and frequency divider, the PLL can cover the four channels of the 60 GHz band, and the in-band phase noise is better than −90 dBc/Hz at 100 KHz offset. Figure 18 shows the measured reference spur at the above-mentioned four channel center frequencies. As indicated, the spurious performance of the PLL is less than −60 dBc.

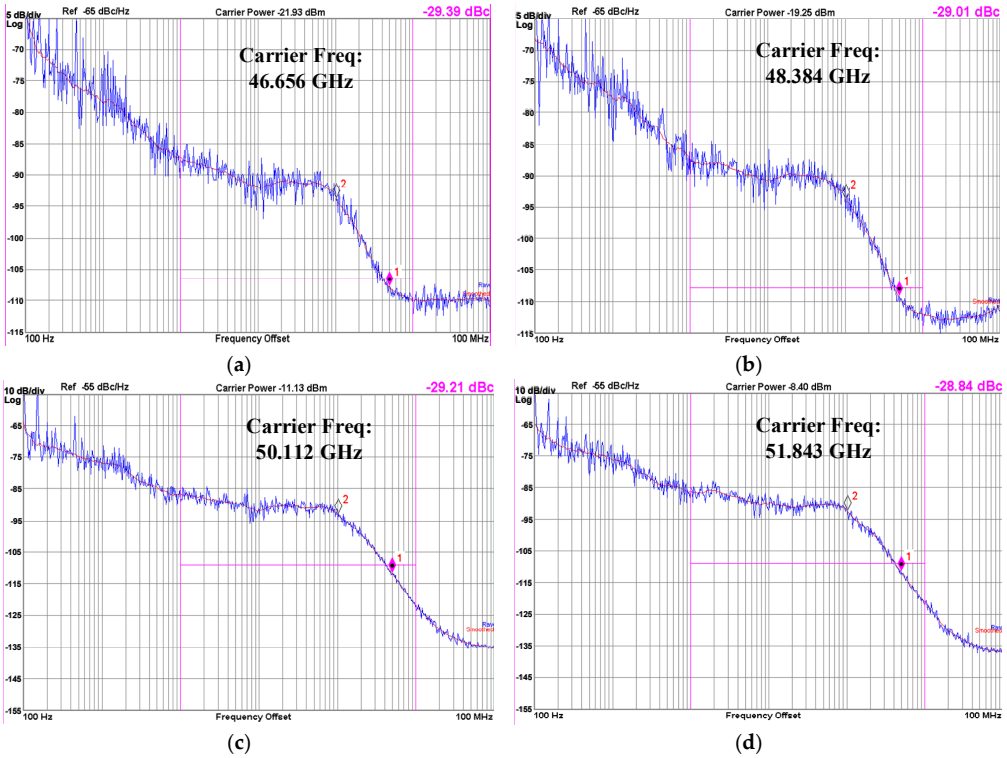

Figure 17. Measured phase noise of the PLL: (**a**) 46.656 GHz; (**b**) 48.384 GHz; (**c**) 50.112 GHz; (**d**) 51.840 GHz.

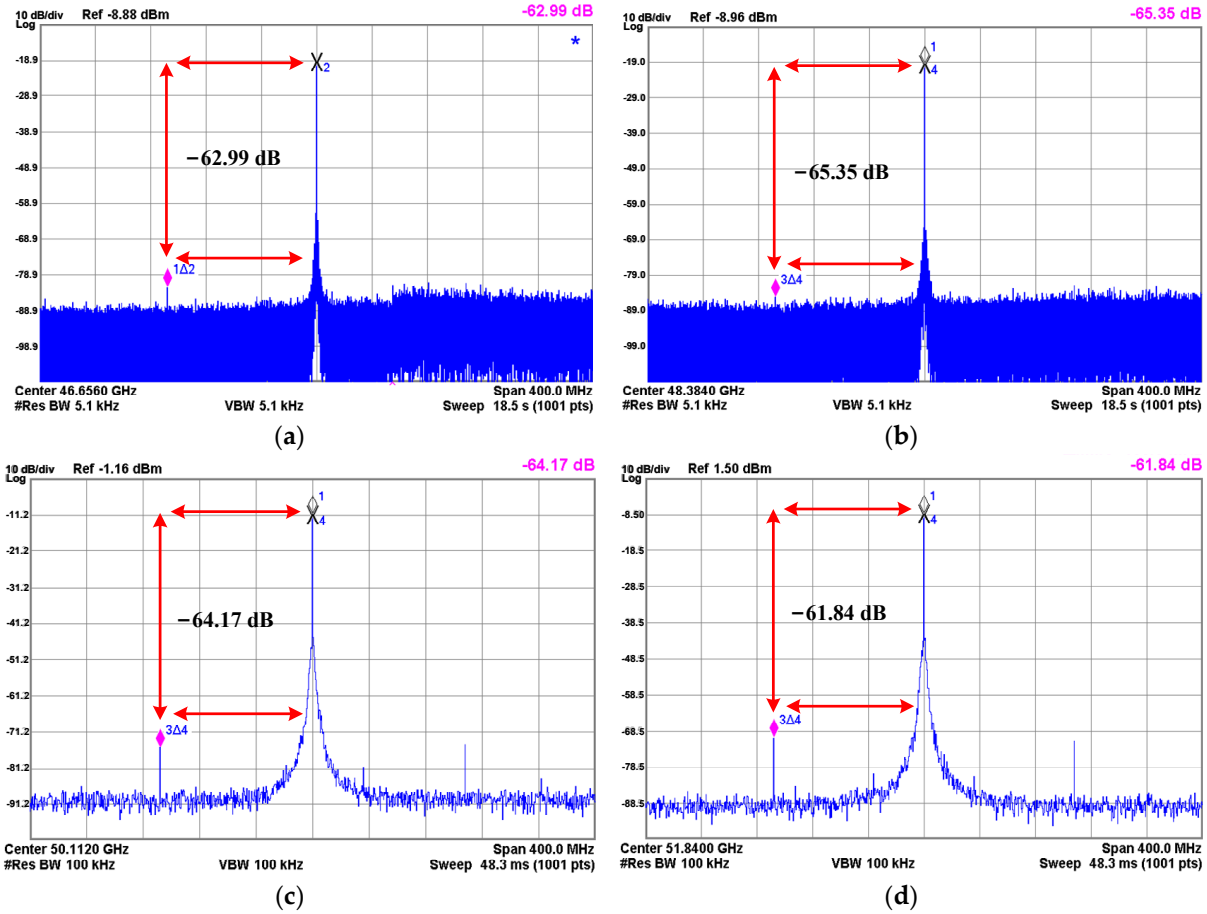

Figure 18. Measured reference clock spurious of the PLL: (**a**) 46.656 GHz; (**b**) 48.384 GHz; (**c**) 50.112 GHz; (**d**) 51.840 GHz.

Table 3 summarizes the measured PLL results at four channels of the 60 GHz bands. The power consumption of the PLL is about 80 mW. The integrated phase noise and RMS jitter are about −29 dBc and 155 fs, respectively.

Table 3. PLL measurement results at four channels of the 60 GHz band.

	Channel 1	Channel 2	Channel 3	Channel 4
Frequency (GHz)	46.656	48.384	50.112	51.84
Int.PN (dBc)	−29.4	−29	−29.2	−28.8
Int.PN (Degree)	2.7	2.9	2.8	2.9
RMS Jitter (fs)	163	165	155	157
PN@1MHz (dBc/Hz)	−93.7	−93.8	−92.8	−92.3
Spur (dBc)	−63	−65	−64	−62
Power consumption (mW)	75	77	78	80

Table 4 shows the performance comparison of this work with the state-of-the-art PLLs for the 60 GHz transceiver applications. As indicated, this fundamental PLL achieves the lowest jitter performance. Moreover, the in-band phase noise and spur performance are also very competitive.

Table 4. Performance comparison with the state-of-the-art PLL for 60 GHz applications.

References	[7]	[8]	[15]	[24]	[32]	[33]	[34]	**This Work**
Topology	ADPLL	ADPLL	SSPLL	SSPLL + QILO	PLL + Doubler	CP PLL + QVCO	CP PLL	CP PLL
Technology	65 nm	65 nm GP	45 nm	65 nm	90 nm	65 nm	65 nm LP	65 nm LP
Locking range (GHz)	56.4–63 (11.6%)	50–66.5 (28%)	33.6–36 (6.9%)	55.6–65 (15.9%)	38.6–45 (14.3%)	57.9–68 (16.5%)	65–67.4 (1.6%)	45.2–52.56 (15%)
Fref (MHz)	100	100	80	36/40	33.75	135	515	108
In-band PN (dBc/Hz)	−75	−79–−83	–	−78.5	−82.5	−91–−84	–	<−90
PN@1MHz (dBc/Hz)	−90	−88–−93	−94.9	92	<−80	−89.8	−84.4	<−92
RMS jitter (fs)	590.2	223–261	251	290	–	238	–	155–165
Spur (dBc)	−74	−59–−68	<−60	−73	−46	−54	–	<−60
Area (mm^2)	0.48	0.45	0.41	1.08	1.38	0.19	0.37	<0.72
Power consumption (mW)	48	46	20.6	32	76	24.6	88	80

With help of the receiver, the IRR performance can be measured. As mentioned before, by tuning the phase of the I- or Q-channel quadrature clock, an optimal IRR performance can be realized. As shown in Figure 19, IRR is better than 30 dB, which indicates that the phase difference of the quadrature signal after calibration is less than 3°.

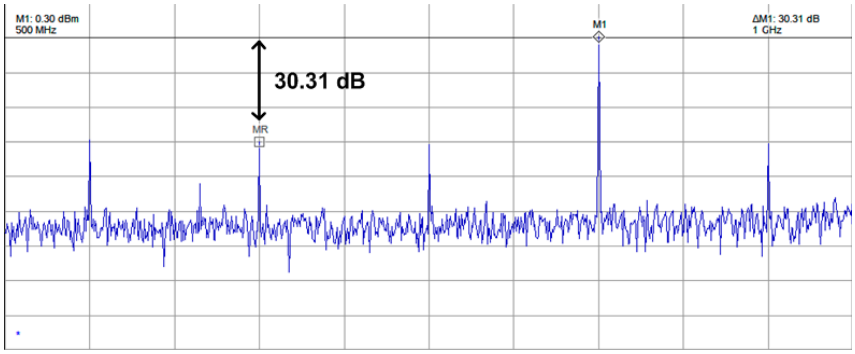

Figure 19. The measured IRR performance of the receiver.

7. Conclusions

Based on a 65 nm CMOS process, a fundamental frequency 48 GHz PLL with quadrature clock generation scheme was realized for the sliding-IF 60 GHz transceiver. With a capacitive-bridged shunt peaking network, an implicit broadband second harmonic filtering was realized, improving the VCO phase noise performance. Also with the capacitive-bridged shunt peaking network and robust biasing circuit, the working speed and locking range of the CML static frequency divider was improved, and its robustness was enhanced over PVT corners. A phase tuning scheme was presented for the quadrature clock calibration and was proven with IRR measurement results. With tests, this fundamental frequency PLL can cover four channel frequencies of the 60 GHz band and exhibited a phase noise and reference spur of lower than −92 dBc/Hz at 1 MHz offset and −60dBc, respectively. Moreover, its in-band phase noise was less than −90 dBc/Hz, and the integrated phase noise was less than −29 dBc, corresponding to a jitter less than 155 fs. With such results, the proposed PLL can be used for 60 GHz communication. Moreover, the proposed PLL was equally applicable to other mmWave bands, such as 5G NR 37–40 GHz and 64–71 GHz.

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