A 4Gb/s/ch 356fJ/b 10mm Equalized On-chip Interconnect with Nonlinear Charge-Injecting Transmit Filter and Transimpedance Receiver in 90nm CMOS Technology
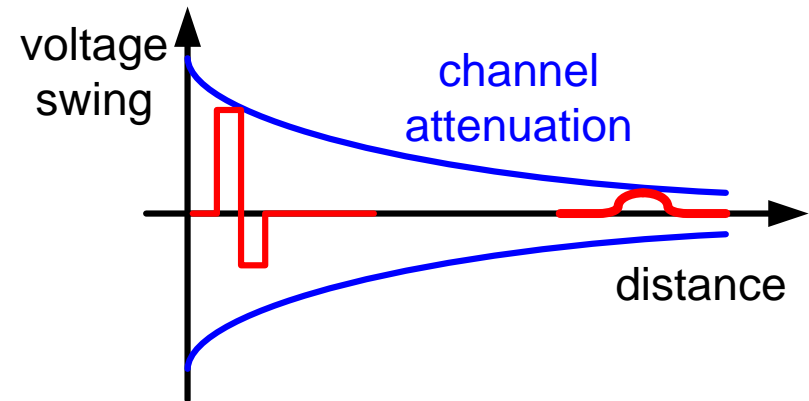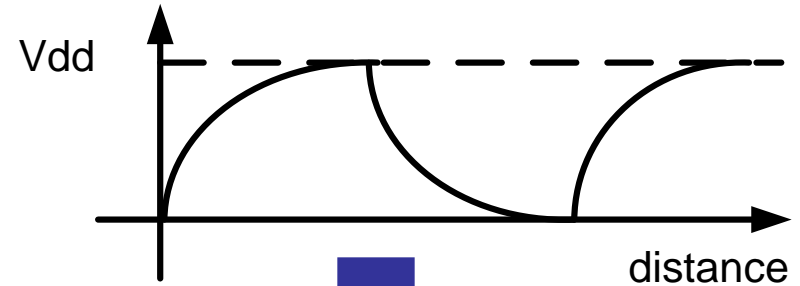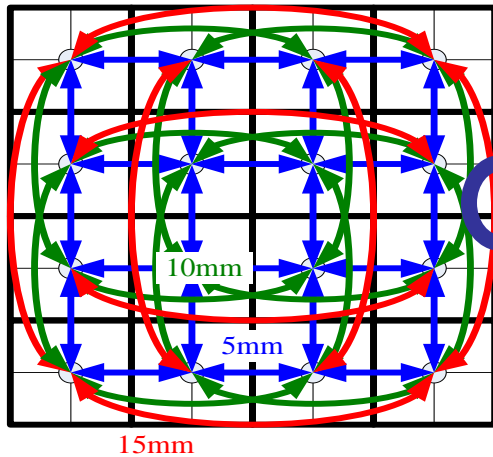
Byungsub Kim

Vladimir Stojanović
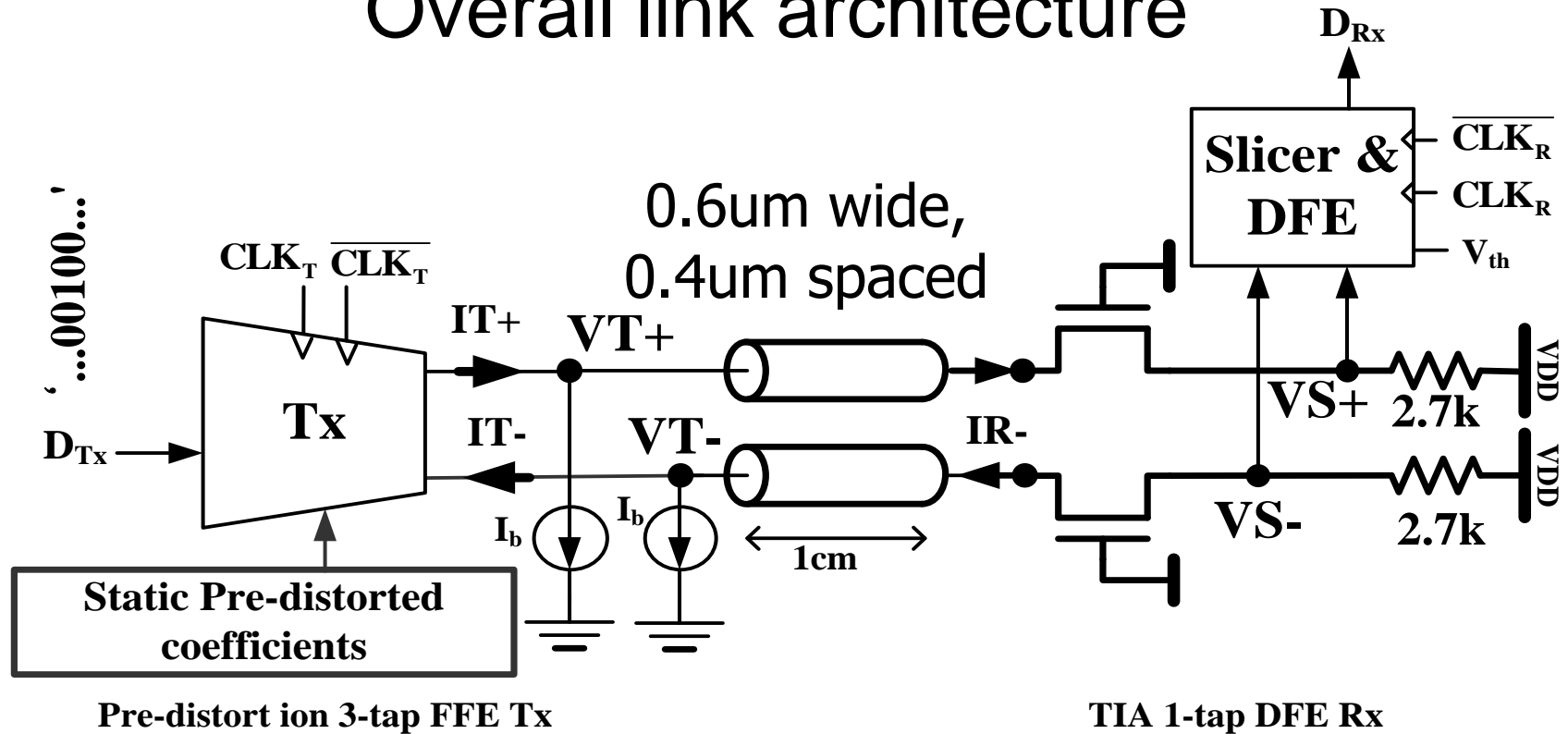
Massachusetts Institute of Technology

Application

Flattened Butterfly NoC
of 64 core processor

10mm
5mm
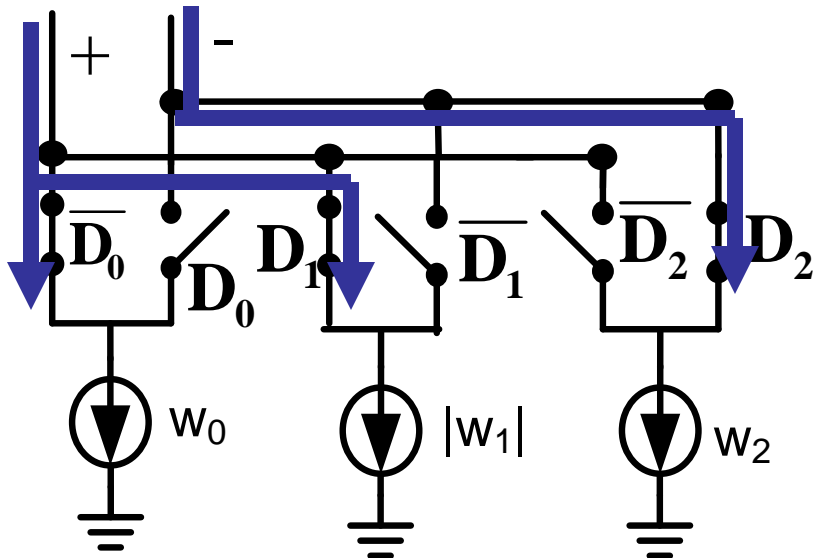15mm

- Long distance interconnect for NoC of many-core processor

- Equalizer benefit
  – Better energy efficiency
  – Lower latency

Vdd

distance

voltage swing

channel attenuation

distance

Overall link architecture

Pre-distort ion 3-tap FFE Tx　　　　　　　　　　　　**TIA 1-tap DFE Rx**

- 3-tap Nonlinear Charge-Injecting Feed Forward Equalizer (FFE) improves driver power efficiency.
- Trans-impedance Amplifier (TIA) before 1-tap DFE improves the bandwidth-power-amplitude trade-off.
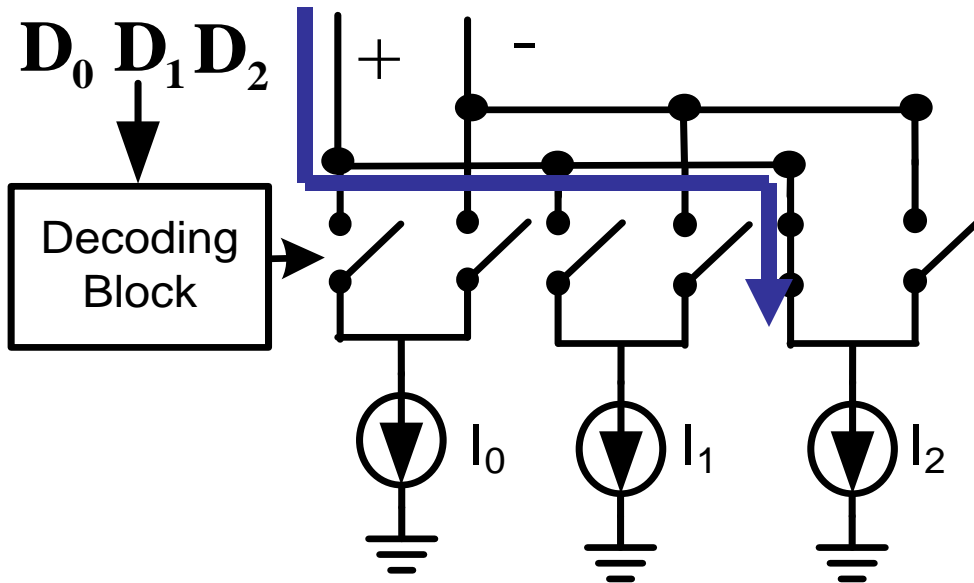
Power lost in linear analog subtraction

Analog FFE

$D_0 D_1 D_2$	FFE sum	IT+
1 1 1	$w_0+w_1+w_2$	I_0
1 1 0	$w_0+w_1-w_2$	$-I_1$
1 0 1	$w_0-w_1+w_2$	$I_0+I_1+I_2$
1 0 0	$w_0-w_1-w_2$	I_2
0 1 1	$-w_0+w_1+w_2$	$-I_2$
0 1 0	$-w_0+w_1-w_2$	$-(I_0+I_1+I_2)$
0 0 1	$-w_0-w_1+w_2$	I_1
0 0 0	$-w_0-w_1-w_2$	$-I_0$

- Linear analog subtraction wastes current
  - $Isup=|w_0|+|w_1|+|w_2|=I_0+I_1+I_2,$ $w_1<0$
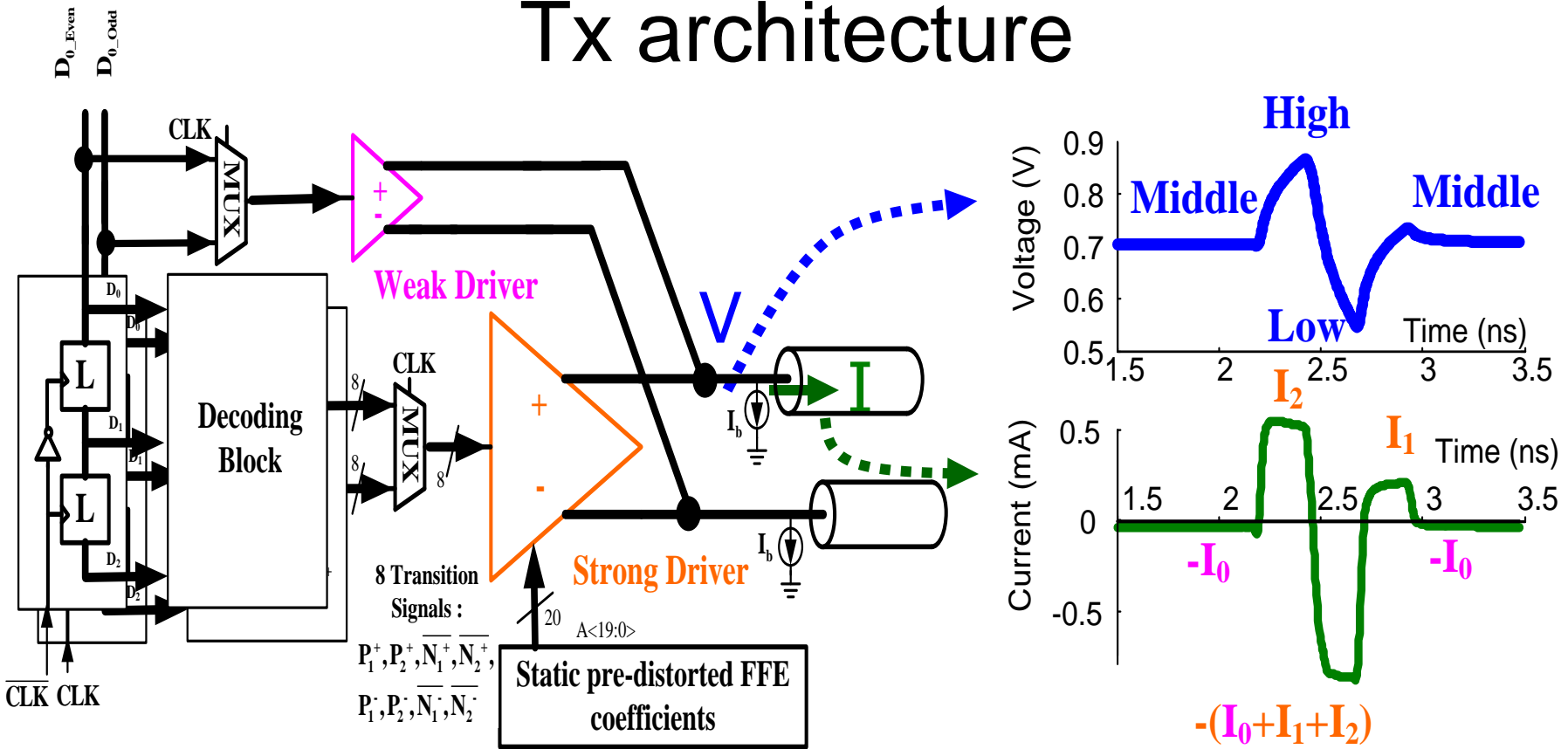 - $Isig=-w_0+w_1+w_2=-I_2,$ $w_1<0$

Charge Injecting FFE

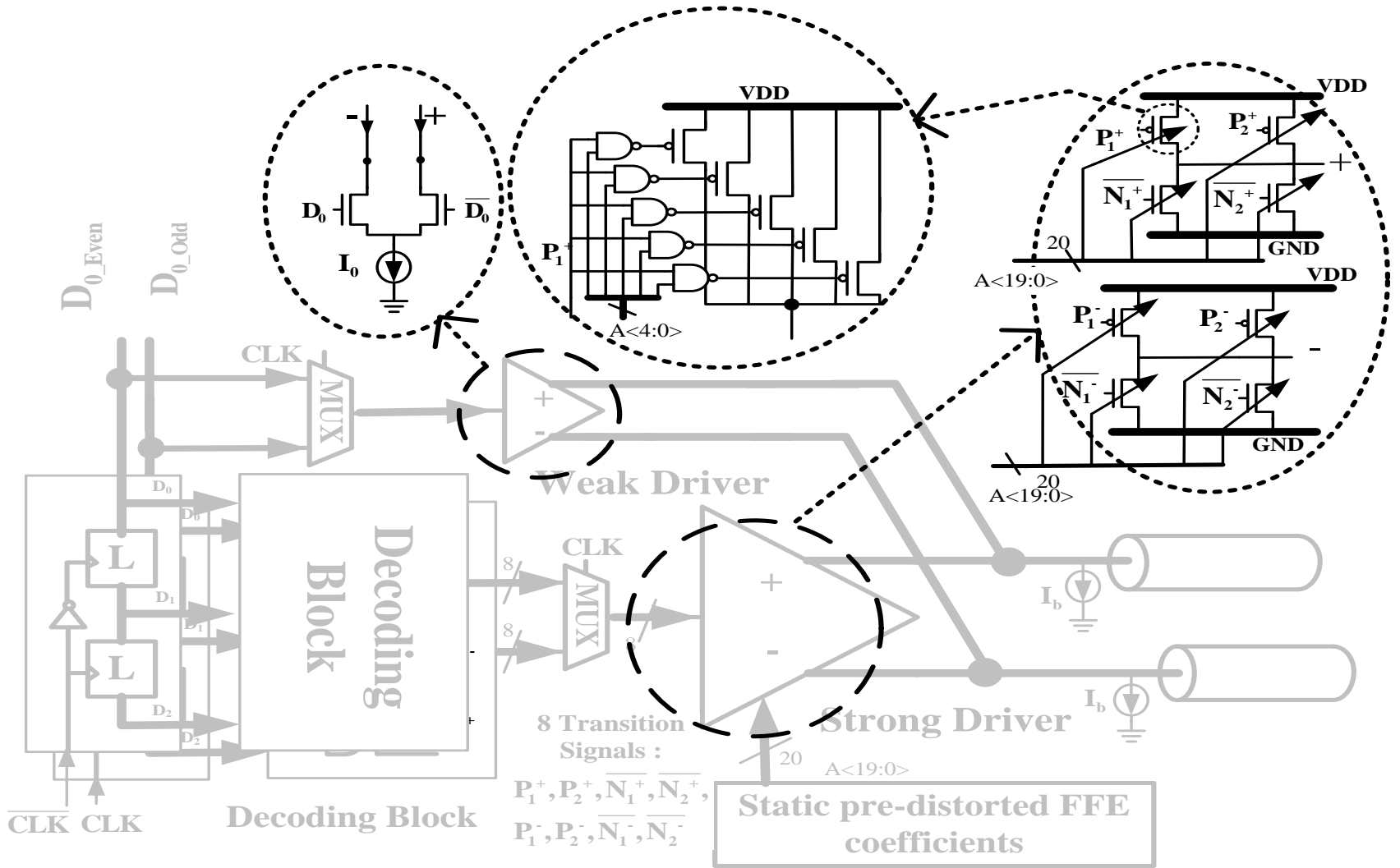| $D_0D_1D_2$	FFE sum	IT+
1 1 1	$w_0+w_1+w_2$	I_0
1 1 0	$w_0+w_1-w_2$	$-I_1$
1 0 1	$w_0-w_1+w_2$	$I_0+I_1+I_2$
1 0 0	$w_0-w_1-w_2$	I_2
0 1 1	$-w_0+w_1+w_2$	$-I_2$
0 1 0	$-w_0+w_1-w_2$	$-(I_0+I_1+I_2)$
0 0 1	$-w_0-w_1+w_2$	I_1
0 0 0	$-w_0-w_1-w_2$	$-I_0$

Charge injection FFE

- Avoid linear analog subtraction → linearity issue
  - $Isup=|-w_0+w_1+w_2|=I_2$, $w_1<0$
  - $Isig=-w_0+w_1+w_2=-I_2$, $w_1<0$
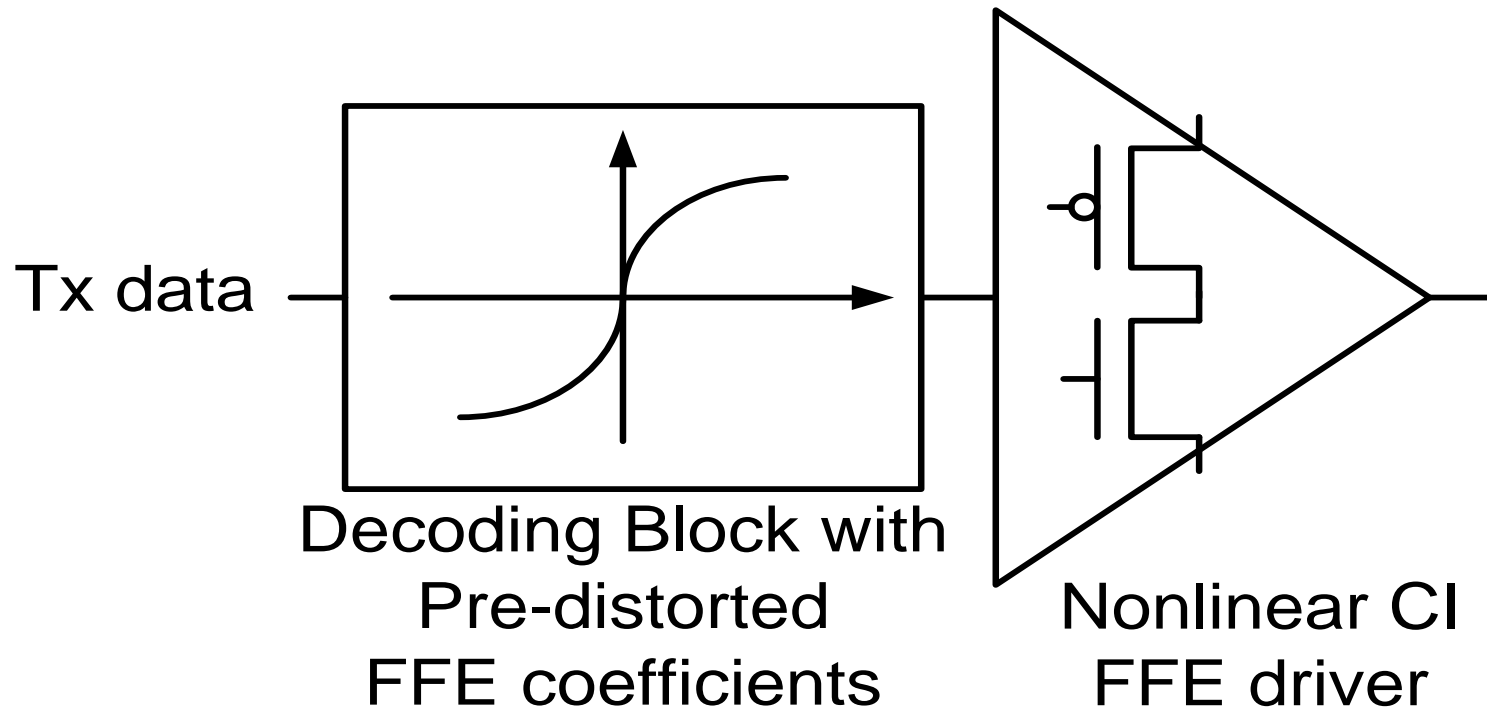
5

Tx architecture

- Strong driver: Large current (I_1, I_2, I_1+I_2) at data transition (AC) ➔ channel attenuation relieves current resolution requirement (3-5bit)

- Weak driver: Small current (I_0) at static level (DC). ➔ accurate control of current resolution required (3-5bit)

6

Tx architecture detail

Nonlinearity compensation concept

Tx data

Decoding Block with
Pre-distorted
FFE coefficients
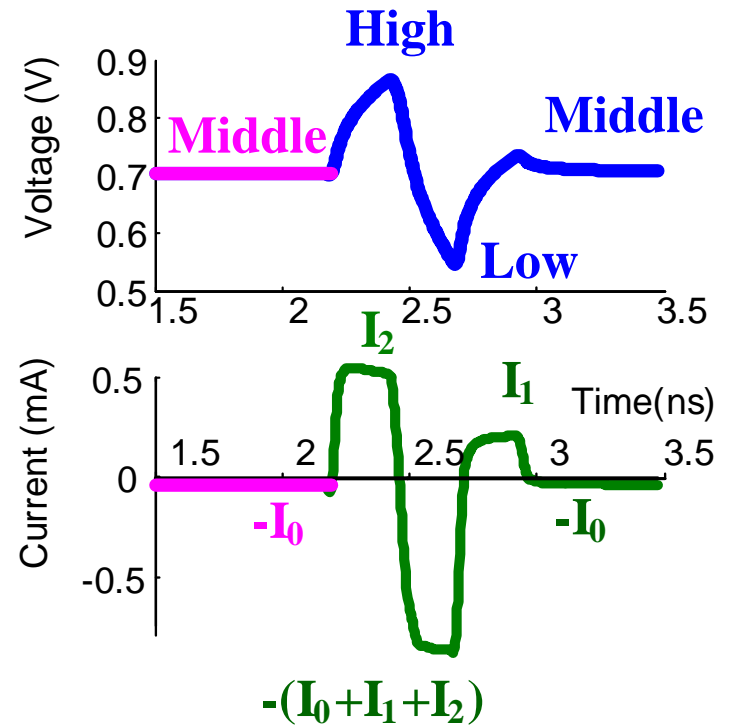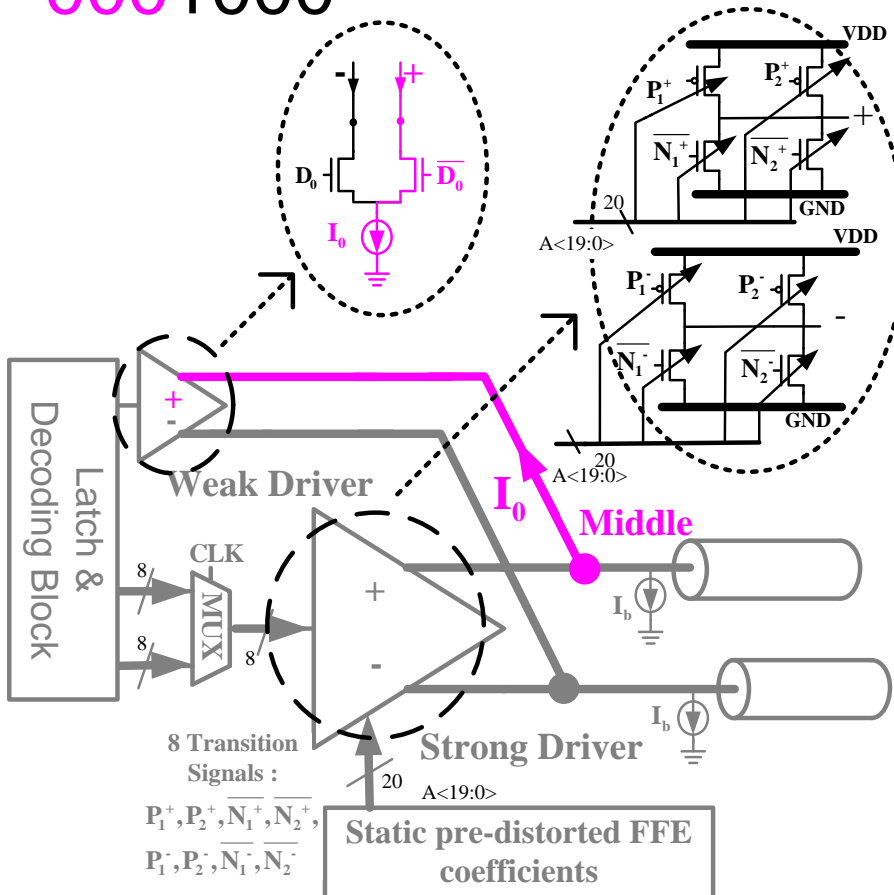
Nonlinear CI
FFE driver

- Non-linear CI FFE driver
- Pre-distorted FFE coefficients in decoding block

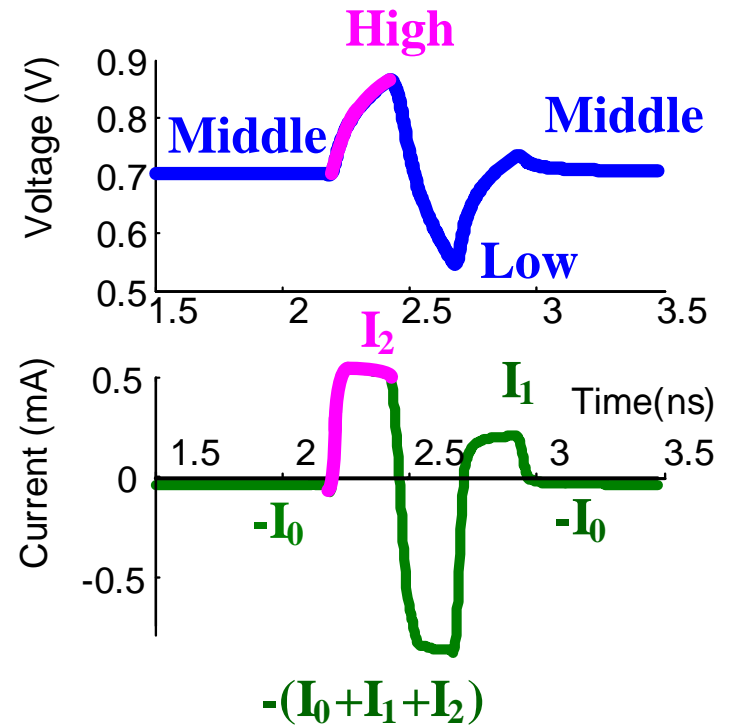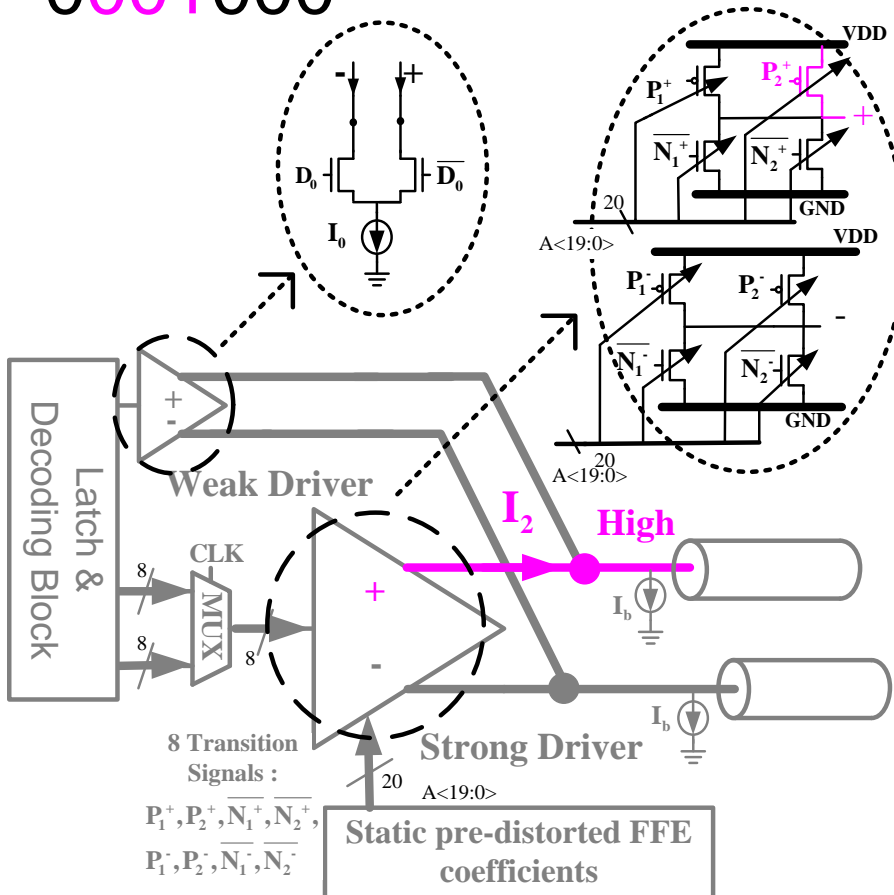# Tx control and nonlinearity compensation

- **0001000**

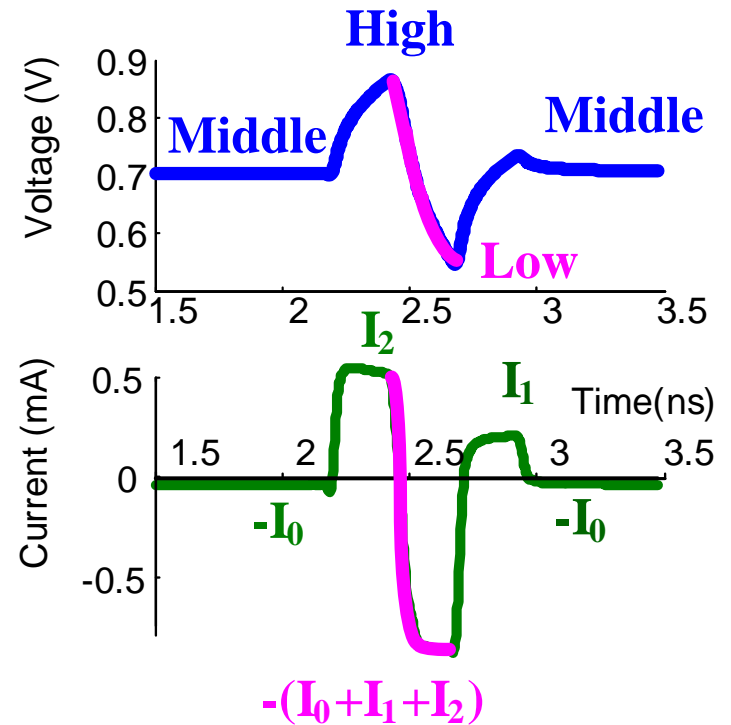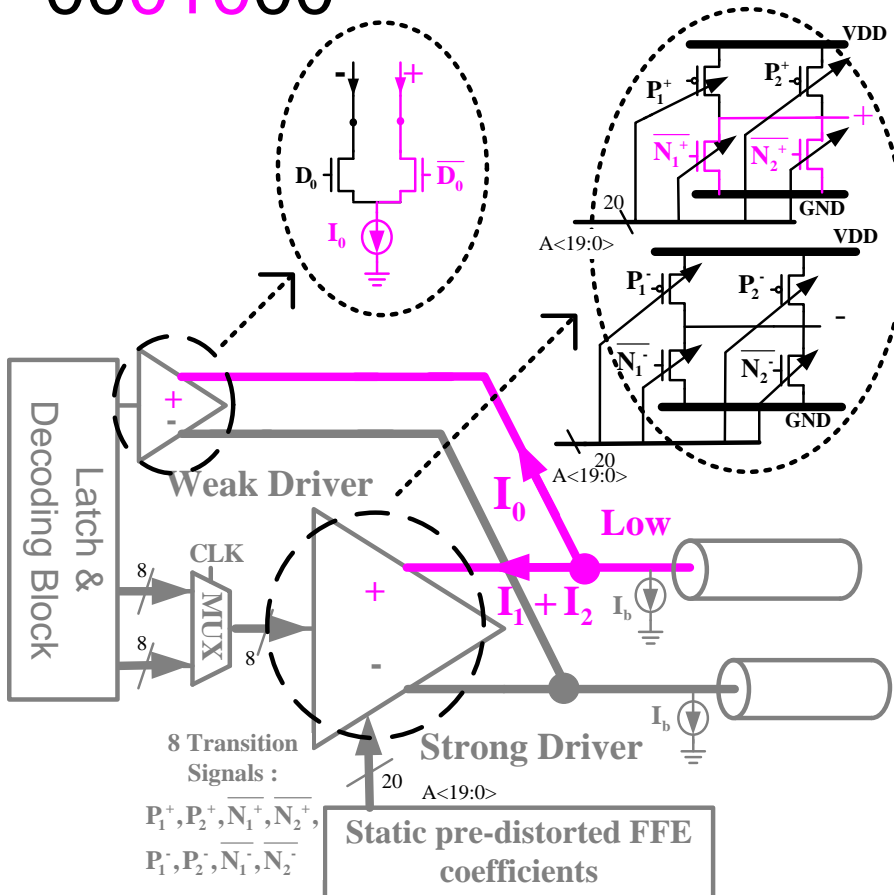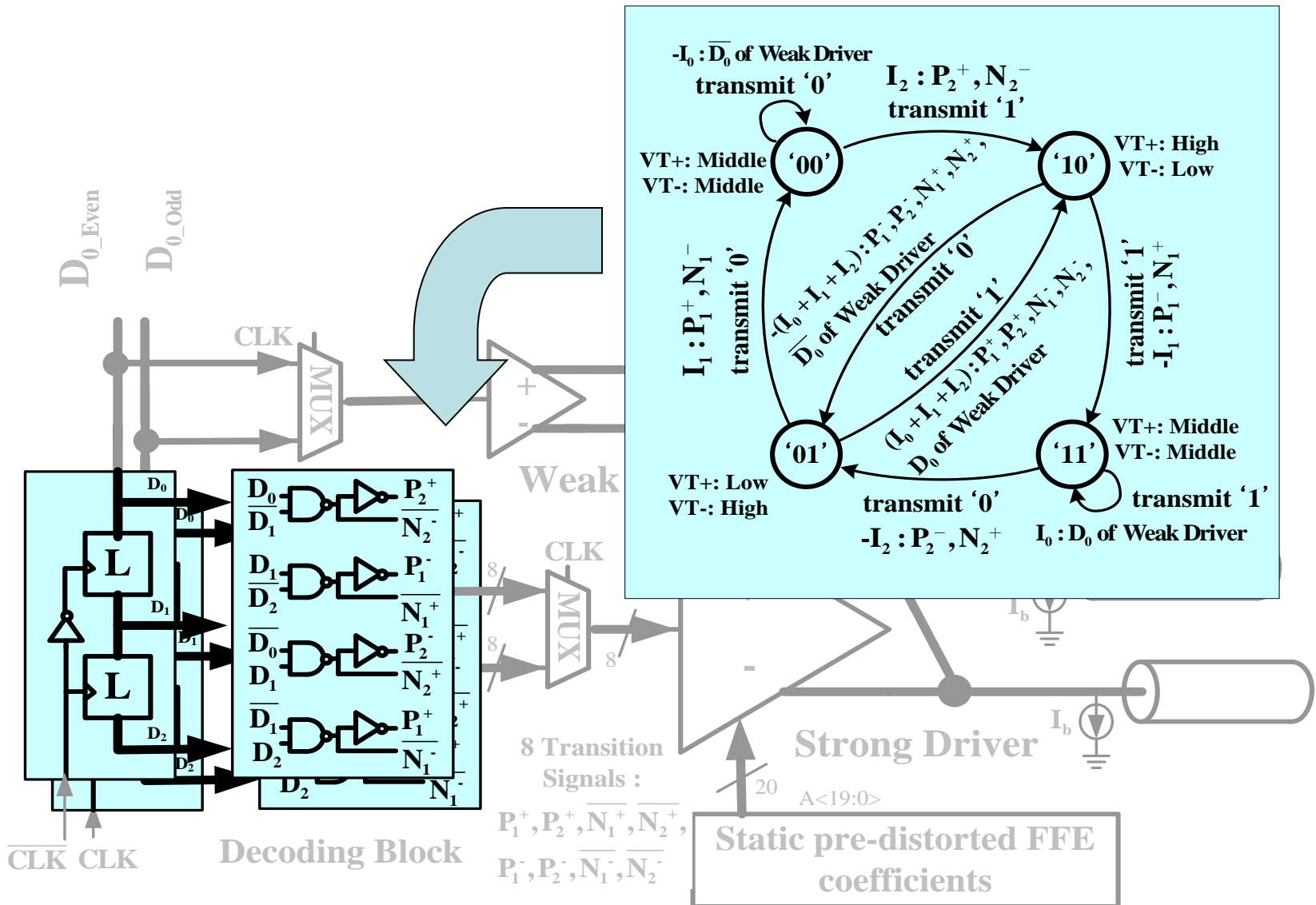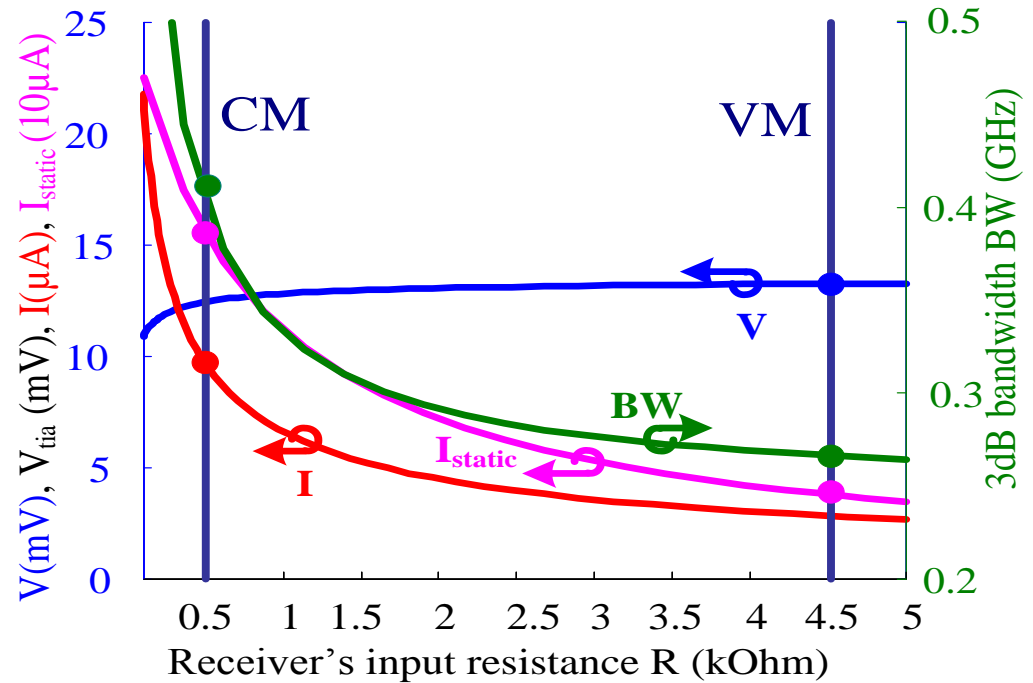# Tx control and nonlinearity compensation

- 0001000

Tx control and nonlinearity compensation

- 0001000

State diagram and decoding block

D_{0_Even} D_{0_Odd}

CLK

MUX

D_0

$\overline{D_0}$

L

L

$\overline{CLK}$ CLK

Decoding Block

$$\frac{D_0}{D_1} \quad P_2^+ / N_2^-$$
$$\frac{D_1}{D_2} \quad P_1^- / N_1^+$$
$$\frac{\overline{D_0}}{D_1} \quad P_2^- / N_2^+$$
$$\frac{\overline{D_1}}{D_2} \quad P_1^+ / N_1^-$$

Weak

CLK

MUX

8 / 8 / 8 /

8 Transition Signals :

$P_1^+, P_2^+, \overline{N_1^+}, \overline{N_2^+},$
$P_1^-, P_2^-, \overline{N_1^-}, \overline{N_2^-}$

Strong Driver

I_b

I_b

20 / A<19:0>

Static pre-distorted FFE coefficients

State diagram:

$-I_0 : \overline{D_0}$ of Weak Driver
transmit '0'

$I_2 : P_2^+, N_2^-$
transmit '1'

VT+: Middle   '00'
VT-: Middle

'10'   VT+: High
          VT-: Low

$I_1 : P_1^+, N_1^-$
transmit '0'

$-(I_0+I_1+I_2) : P_1^-, P_2^-, N_1^+, N_2^+,$
$\overline{D_0}$ of Weak Driver
transmit '0'

transmit '1'
$(I_0+I_1+I_2) : P_1^+, P_2^+, N_1^-, N_2^-,$
D_0 of Weak Driver

transmit '1'
$-I_1 : P_1^-, N_1^+$

VT+: Low   '01'
VT-: High

'11'   VT+: Middle
          VT-: Middle

transmit '0'
$-I_2 : P_2^-, N_2^+$

transmit '1'
$I_0 : D_0$ of Weak Driver

Receiver's termination trade off

- Current mode (CM) : small R : A.P. Jose, VLSI'05
- Voltage mode (VM) : large R : E. Mensink ISSCC'07

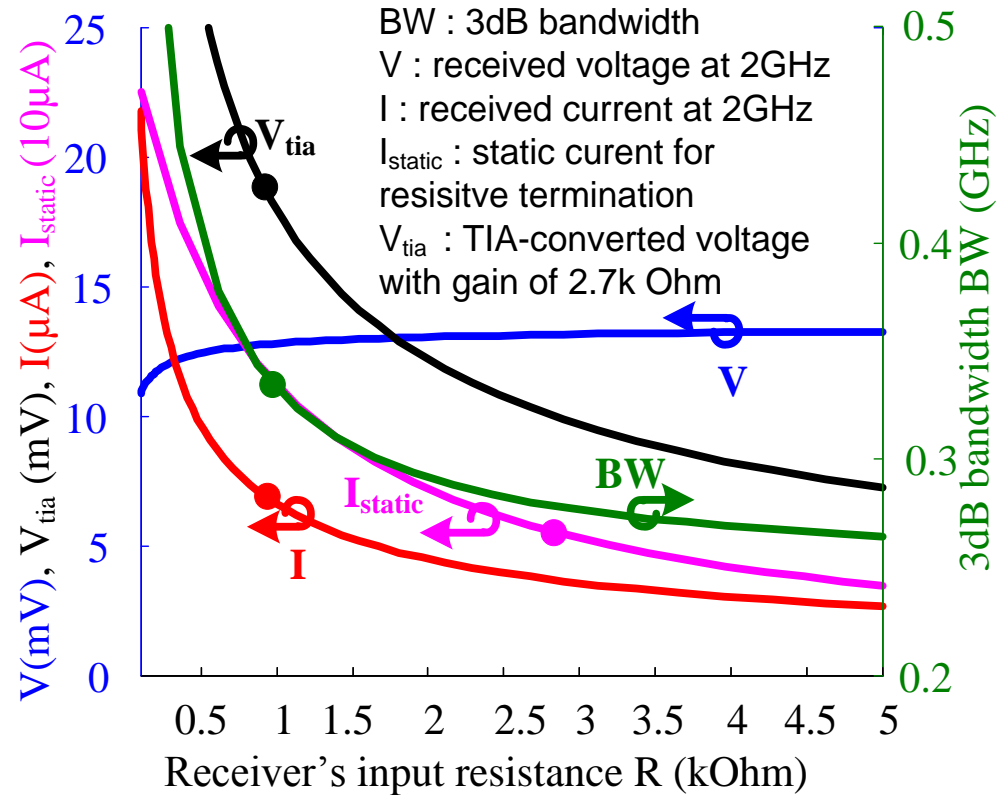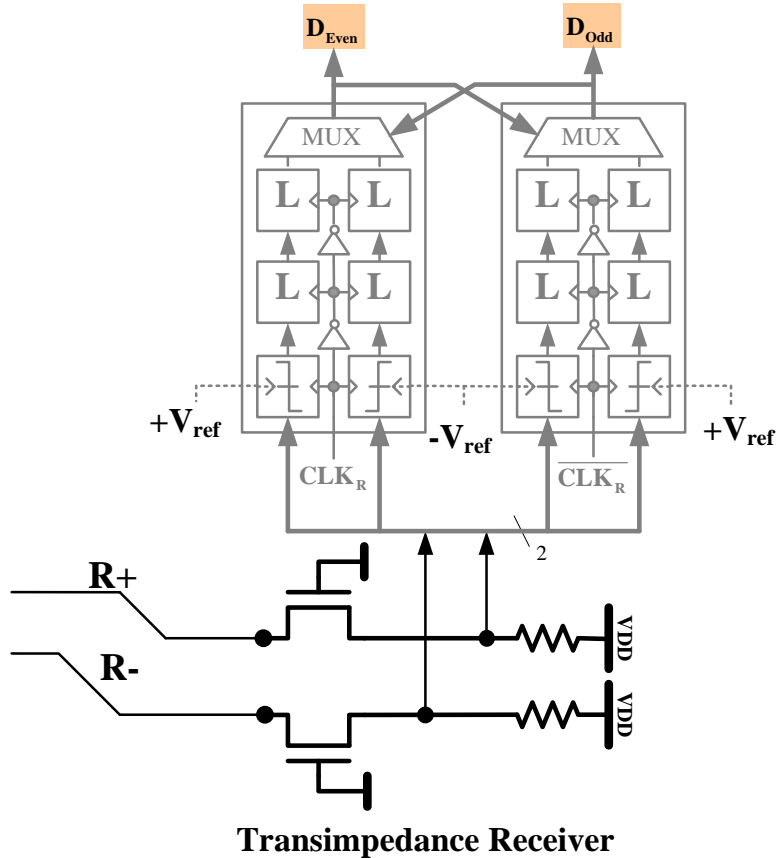# Trade-off of trans-impedance amplifier (TIA)

Transimpedance Receiver

BW : 3dB bandwidth
V : received voltage at 2GHz
I : received current at 2GHz
I_{static} : static curent for resisitve termination
V_{tia} : TIA-converted voltage with gain of 2.7k Ohm

- TIA achieves high bandwidth, small static power, large amplitude simultaneously.
  - 50% static current, 150% voltage amplitude for the same bandwidth

Chip Infrastructure for *in-situ* characterization
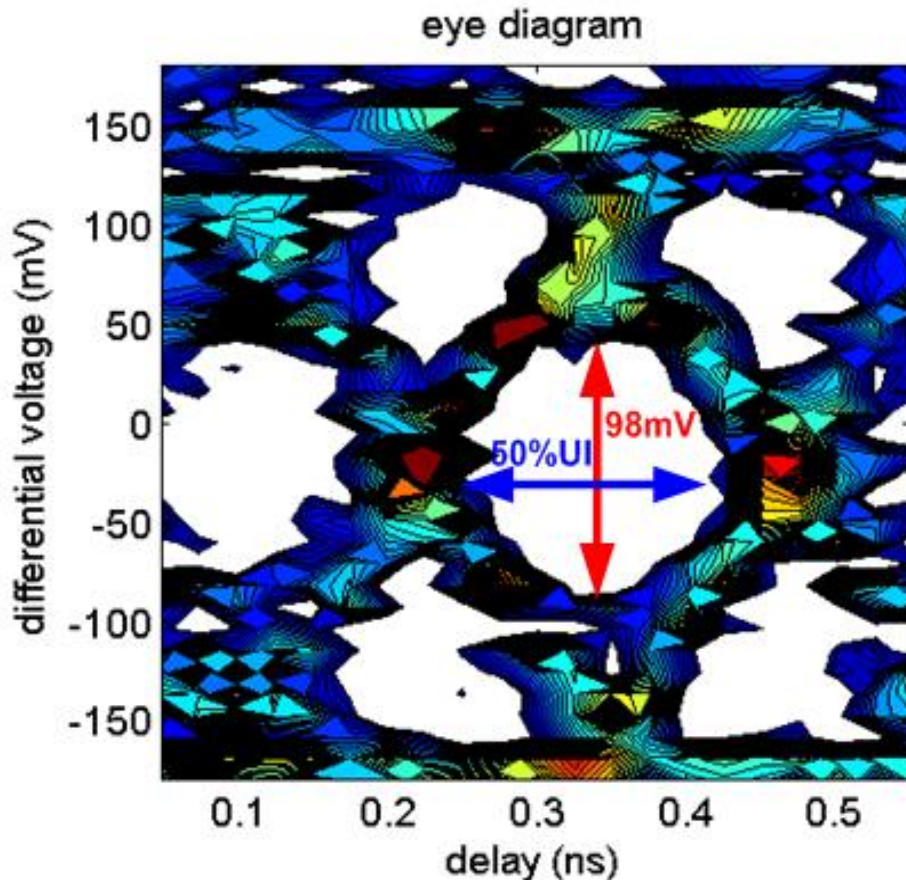
Eye diagram (4Gb/s/ch, 2Gb/s/um)

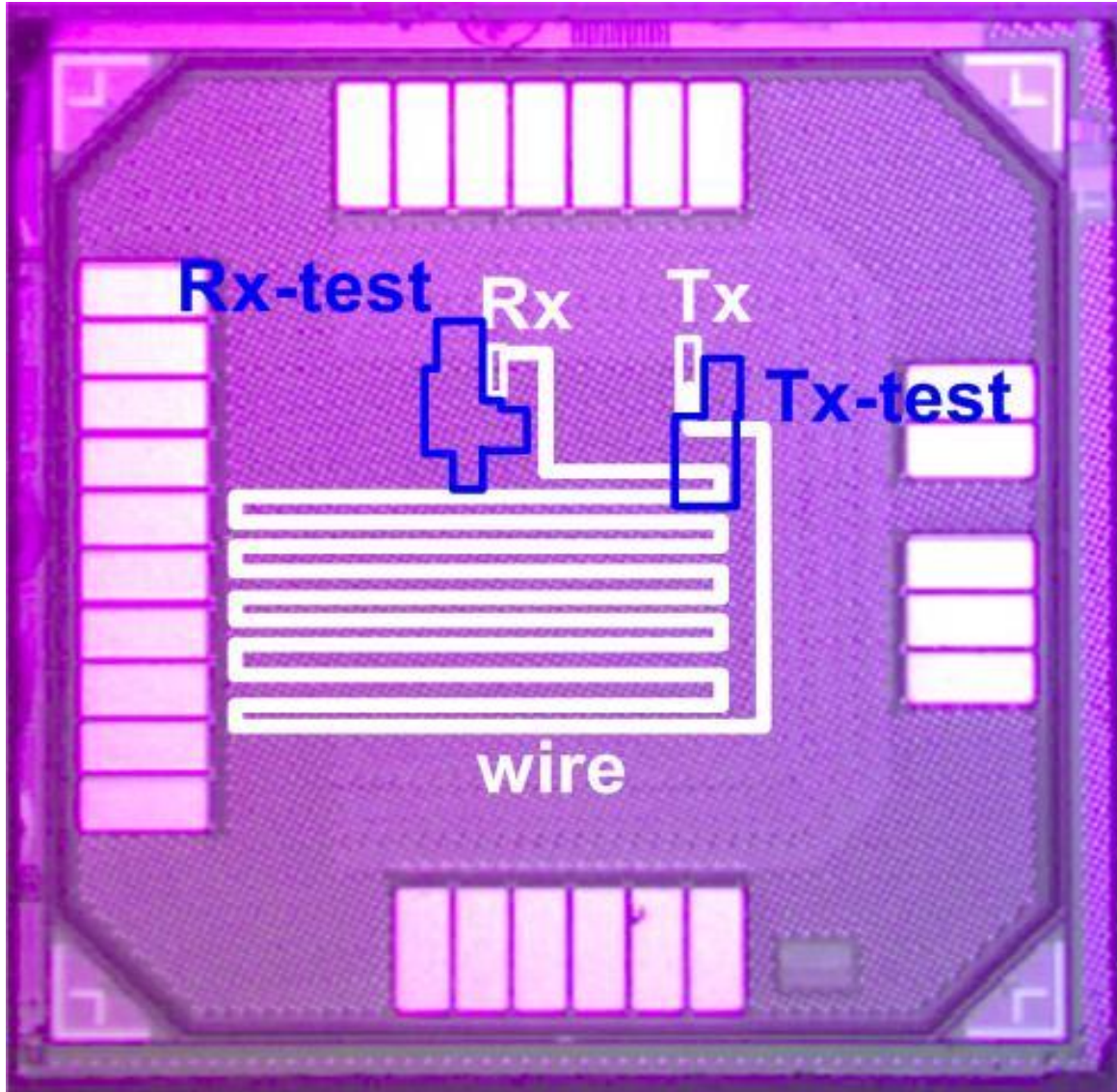eye diagram

- 98mVdpp vertical
- 50%UI horizontal
- First measured *in-situ*
  - Sweep threshold
  - Sweep receiver delay
- FFE: only
- DFE: not necessary

Chip die photo

- 1mm x 1mm
- 90nm CMOS
- Tx core : 70um x 16um
- Rx core : 40um x 16um

Comparison to relevant work

	This work				Mensink ISSCC07	Repeater Kim ICCAD07
Data rate	4Gb/s/ch				2Gb/s/ch	4Gb/s/ch
Data rate density	2Gb/s/μm				1.1628Gb/s/μm	2Gb/s/μm
Channel length	1cm				1cm	1cm
Vertical Eye	98mV				N/A	rail-to-rail
Horizontal Eye	50%UI@(4Gb/s) measured on-chip				44%UI @ (1.75Gb/s) after 50Ohm buffer	N/A
Measured Energy Cost (fJ/b) at room temperature	total	356			280	1500
	Tx	total	277			
		Strong driver	51			
		Weak driver + TIA bias	48			
		Decoder	24			
		Clock	67			
		Pre-driver	87			
	Rx	total	79			
		Slicer/Latch	30			
		Clock	49			
Technology	90nm				90nm	90nm

- 30% more energy, x2 more speed

Summary

- Charge-injection + non-linear compensation reduces driver's power (< 50%).
  - Avoid analog subtraction
  - Utilize efficient nonlinear driver
- Trans-impedance amplifier (TIA) achieves high bandwidth, small power, and large amplitude simultaneously.
  - 50% static power
  - 150% amplitude

Acknowledgement

- Trusted Foundry for chip fabrication
- Interconnect Focus Center (IFC)
- Semiconductor Research Corporation Program
- Intel Corporation
- Center for Integrated Circuits and Systems (CICS) at MIT

- Fred Chen, Sanquan Song