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A 5.7~6.0 GHz CMOS PLL with Low Phase Noise and -68dBc Reference Spur

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Abstract: **This paper presents a 5.7~6.0 GHz Phase-Locked Loop (PLL) design using a 130nm 2P6M CMOS process. We propose to suppress reference spur through reducing the current mismatch in charge pump (CP), controlling the delay time in phase frequency detector (PFD), and using a smaller VCO gain (K_{VCO}). With a reference frequency of 32.768 MHz, chip measurement results show that the frequency tuning range is 5.7~6.0 GHz, the reference spur is -68dBc, the phase noise levels are -109dBc/Hz and -135dBc/Hz at 1MHz and 10MHz offset respectively for 5.835 GHz. Compared with existing designs in the literature, this work's reference spur is improved by at least 17% and its phase noise is the lowest. Under a 1.5V supply voltage, the power dissipation with an output buffer of the PLL is 12mW.**

Keywords—PLL, reference spur, current mismatch, low phase noise

I. Introduction

Modern system-on-chip applications rely on PLLs to provide high-precision carrier signals. The quality of carrier signals significantly impacts the performance of transceivers such as the sensitivity of receivers and the spectrum of transmitted signals. With the emergence of new wireless communication standards, PLLs require to improve phase noise and suppress reference spur. As key performance parameters in PLLs (*i.e.*, phase noise, reference spur level, power consumption, frequency range, and chip area) are interactive, it is a challenging task to consider design tradeoffs and optimize PLL designs [1].

Phase noise represents random frequency instability, and reference spurs are undesired frequency content in a VCO output spectrum [2]. The objective of this work is to reduce phase noise and reference spur in PLLs. We first analyze the underlying

factors that determine reference spur levels, and then apply three techniques (*i.e.*, a low current mismatch in CP, delay controllable PFD, and a lower VCO gain) in a PLL to minimize reference spurs.

The mismatch between charging and discharging currents in a charge pump (CP) causes PLL phase offset and increases reference spurs. So far, a few techniques have been presented to address the current mismatch issue in CP. In [3], a symmetrical layout was used to reduce the CP current mismatch. In [4], an active loop filter was used to isolate V_{CTR} and V_{CP} (CP output node). Yet, the match between V_{CP} and an extra V_{REF} is highly dependent on the layout. In [5], a digital calibration technique was proposed to reduce the current mismatch in CP. Yet, this technique relies on accurate current sources and requires extra calibration time. In [6], in order to mitigate current mismatch in CP, an adaptive gate bias technique was presented to enhance output impedance of CP. Yet, the effect of channel length modulation affects the current mismatch. In [7], a high gain amplifier was used in CP to reduce current mismatch. Simulation results show the current mismatch is only 0.5%. Therefore, instead of developing new circuits to tackle current mismatch in CP, we adopt the existing approach in [7] to our PLL system.

In addition to minimizing current mismatch in CP, we also explore other building blocks in PLLs that may contribute to reference spurs. We propose a delay time controllable PFD, and adopt a lower gain VCO which also reduces phase noise. In addition, a 5-bit register enables 32 tuning points for a switched capacitor array, which ensures accurate PLL frequency locking between 5.7 and 6 GHz. We have implemented and fabricated the proposed PLL design in a standard 0.13μm CMOS technology. Measurement results show that the reference spur is -68dBc, and the phase noise levels are -109dBc/Hz and -135dBc/Hz at 1MHz and 10MHz offset respectively for 5.835 GHz. Compared with existing designs in the literature, the measured reference spur is improved by at least 17%, and our PLL achieves the lowest phase noise.

The rest of this paper is organized as follows. Section II introduces the proposed PLL architecture. Section III analyzes potential factors that determine reference spur, and describes the design details of CP, PFD, and VCO blocks. Chip measurement results are discussed and compared with the state-of-the-art designs in the literature in Section IV. Finally, Section V concludes this paper.

II. Proposed PLL Architecture

Fig. 1 depicts the architecture of our proposed PLL, which mainly includes a phase frequency detector (PFD), a charge pump (CP), a low-pass filter (LPF), a voltage controlled oscillator (VCO), a frequency divider (DIV), and an auto frequency calibration (AFC) circuit. The PLL output is given to receiver (RX) and transmitter (TX) in an RF communication system. In order to cover the frequency range of 5.7 ~ 6.0 GHz, a switched capacitor module is implemented to adjust the capacitance value in the VCO. A 5-bit register *SW<4:0>* enables 32 coarse points for tuning PLL

frequency. The AFC circuit consists of a calibration module (CAL) and a preset voltage module (PVM). The CAL determines the appropriate value for register SW<4:0>, while the PVM provides a preset DC voltage (V_{PRE}) as the initial VCO control voltage.

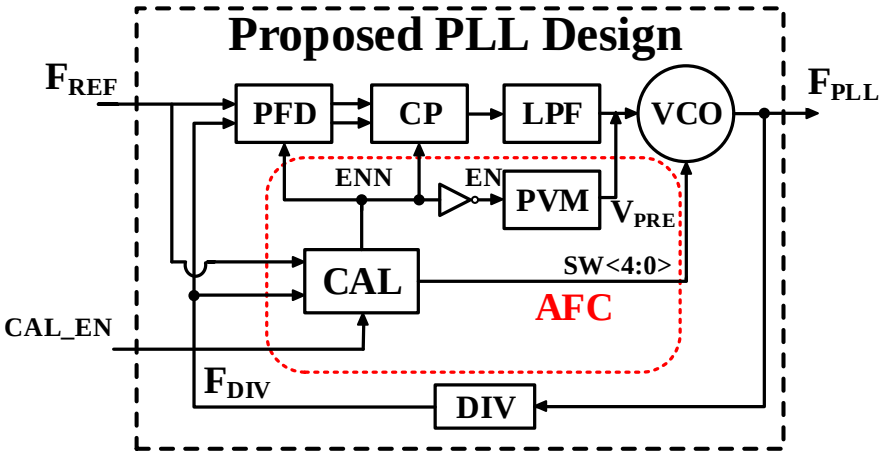
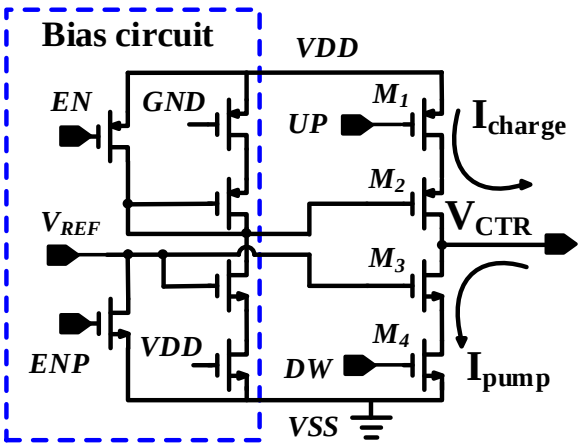


Fig. 1. Proposed PLL architecture and building blocks

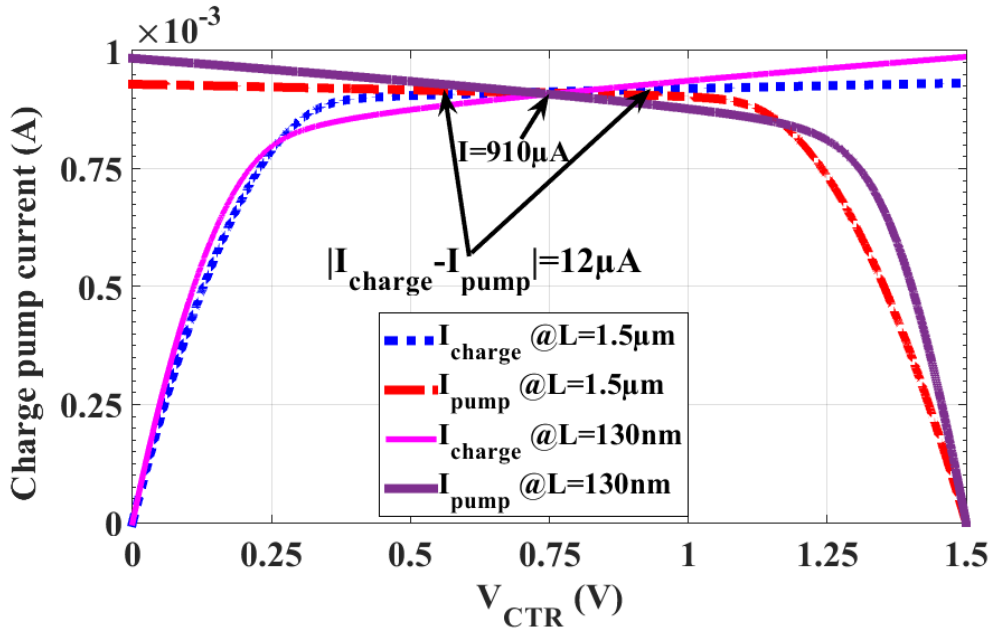
III. PLL Circuit Design and Implementation

A. Reference spur analysis

First, let us analyze the underlying factors that deteriorate the reference-spur. Fig. 2(a) shows schematic of a charge pump, where the charge and pump tube source-drain voltages oppositely change when V_{CTR} varies. As a result, I_{charge} and I_{pump} show a significant mismatch when V_{CTR} is away from VDD/2, as plotted in Fig. 2. Two currents match each other at 910μA when V_{CTR} is equal to VDD/2. The current mismatch is more severe when V_{CTR} moves away from this matching point. As illustrated in Fig. 2(b), current mismatch can be mitigated but not completely eliminated when using long-channel transistors (dashed lines).



(a)



(b)

Fig. 2. Simulated CP output currents against its control voltage (V_{CTR})

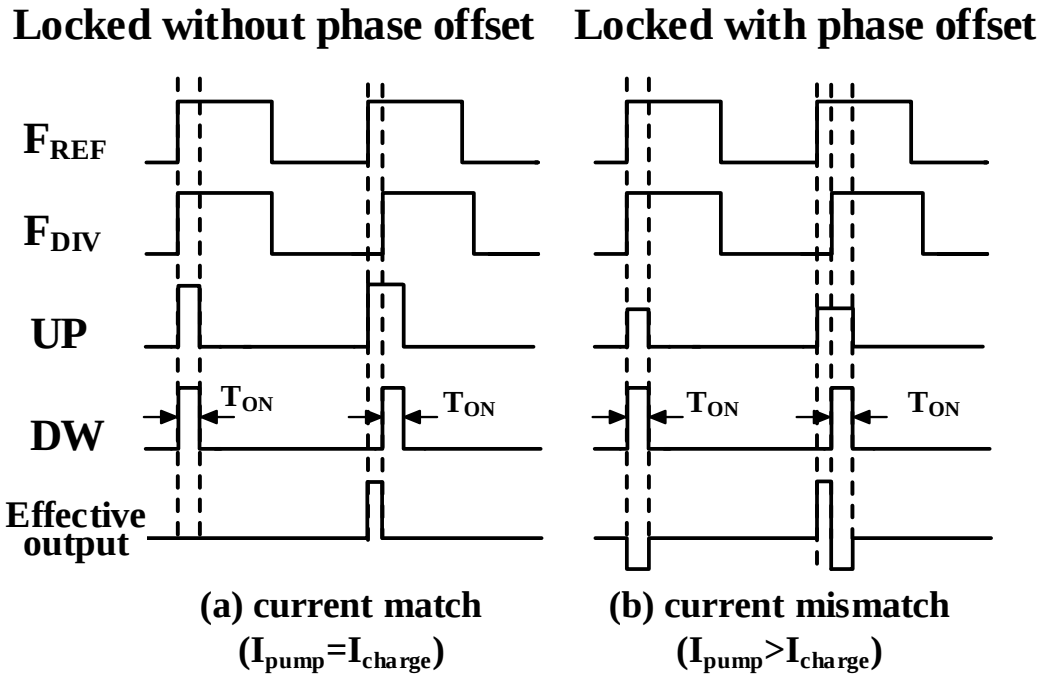


Fig. 3. PLL locking behaviors without and with current mismatch in CP

Fig. 3 show PLL locking behaviors for matched or mismatched CP currents. In order to eliminate dead zone, the PFD output has a common turn-on time (T_{ON}) for UP and DW. In Fig. 3(a) current match prevents a phase error after locking PLLs, while in Fig. 3(b) an additional phase error is produced when I_{pump} is greater than I_{charge}. According to [8], this additional phase error $|\varphi_S|$ and average current in CP are modeled as

$$|\varphi_S| = 2\pi \times \frac{T_{ON}}{T_{REF}} \times \frac{I_{MIS}}{I_{CP}} \quad (1)$$

$$I_{CP} = \frac{I_{charge}+I_{pump}}{2} \quad (2)$$

Here I_{MIS}, I_{CP}, T_{REF}, and T_{ON} are the mismatch current in CP, the average current in CP, the reference clock cycle, and the common effective time in a PFD, respectively. Then, based on [8], F_{BW} is used to approximate the PLL loop bandwidth in the equation (3). Here R, K_{VCO}, and N represent the resistance of 1-order loop filter, the gain of VCO, and the division ratio of a divider, respectively. Finally, the power of PLL reference spur is expressed as equation (4).

$$F_{BW} \approx \frac{I_{CP}\times R\times K_{VCO}}{2\pi\times N} \quad (3)$$

$$P_{SPUR} \approx 20\log(\frac{I_{CP}\times R\times|\varphi_S|\times K_{VCO}}{2\pi\times F_{REF}}) \approx 20\log(R\times K_{VCO}\times T_{ON}\times I_{MIS}) \quad (4)$$

Observing the equations (3) and (4), we find that in order to diminish P_{SPUR} and maintain a desired loop bandwidth F_{BW}, a good choice is to use a smaller K_{VCO} and a higher I_{CP}. Meanwhile, smaller I_{MIS} and T_{ON} are utilized to effectively suppress P_{SPUR}. This is the design methodology of our proposed PLL.

B. T_{ON} controllable PFD for improving reference spur

Due to the limited setup time, a typical PFD circuit cannot turn on charge pump switches instantly when F_{REF} and F_{DIV} are very close. As shown in Fig. 4, a controllable delay module enables a proper pulse in zero phase error to eliminate the risk of dead zone. The delay module extends the reset signal of D flip-flops to achieve common effective time (T_{ON}) of UP and DN. Yet, due to the current mismatch and excessive power dissipation in CP, delay time should be properly controlled. Assuming a given current mismatch in CP, the equation (1) indicates that an increase of T_{ON} leads to a larger phase error. The design uses *D<1:0>* to make minor changes to the T_{ON} and we can choose the best setting after the test. The simulation results of T_{ON} values are listed in Table I.

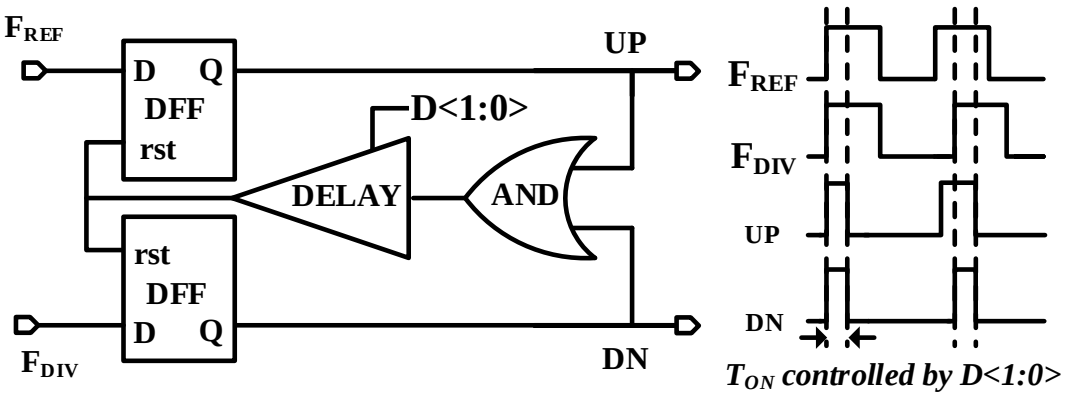


Fig. 4. Proposed PFD circuit with a controllable delay

TABLE I. Simulation results of T_{ON} value with respect to different $D<1:0>$

$D<1:0>$	00	01	10	11
T_{ON} (ns)	0.67	1.09	1.39	1.82

C. Low current mismatch charge pump

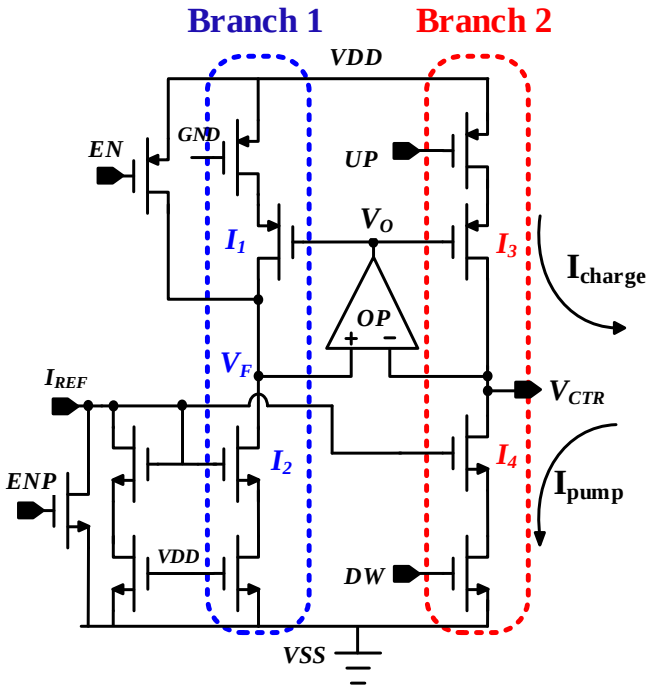


Fig. 5. Proposed CP circuit with an amplifier to improve current mismatch

The CP circuit in Fig. 5 adopts an amplifier to resolve mismatch issue. When V_{CTR} is equal to V_F, the bias voltages and each node of two branches are exactly the same. Negative feedback effect forces V_F always close to V_{CTR}. For example, if V_{CTR} is larger than V_F, V_O, I_1 and I_3 will decrease to force V_F to increase until $V_F = V_{CTR}$.

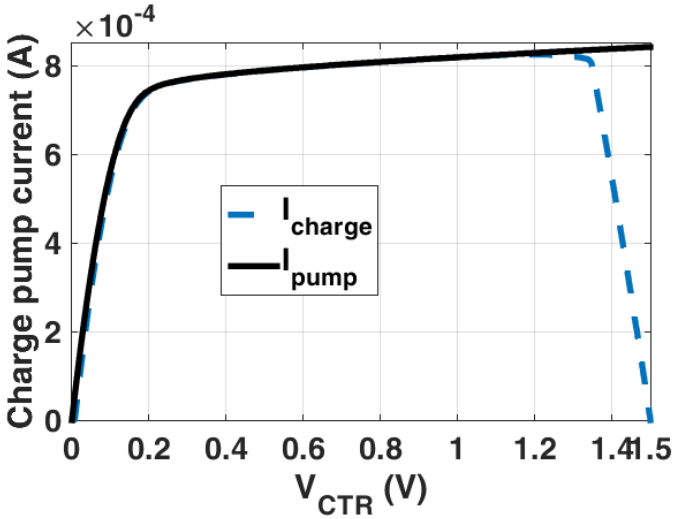


Fig. 6. Simulation results of current mismatch in the proposed CP

Regarding CP design requirements, both mismatch current and overall current variation need to be small [7, 9-10]. The current mismatch ratio is calculated by the equation (5). Assuming I_{MAX} (or I_{MIN}) is the maximum (or minimum) current in CP with respect to the maximum (or minimum) VCO control voltage V_{CTR}, equation (6) defines the current variation ratio in CP. When V_{CTR} varies from 0.2V to 1.2V, the current mismatch ratio (I_{MIS}/I_{CP}) is less than 0.5%, and the current variation ratio (I_X) is 11%. In order to ensure proper loop gain and bandwidth, V_{CTR} is chosen in the range of 0.4~1.1V in this design. As a result, according to the results in Fig. 6 and the equations (5)-(6), the current mismatch ratio is less than 0.1% and I_X is less than 5%.

$$\frac{I_{MIS}}{I_{CP}} = 2 \times \frac{|I_{charge} - I_{pump}|}{I_{charge} + I_{pump}} \quad (5)$$

$$I_X = 2 \times \frac{I_{MAX} - I_{MIN}}{I_{MAX} + I_{MIN}} \quad (6)$$

D. A wide tuning range VCO with low K_{VCO}

Since a larger VCO gain (K_{VCO}) deteriorates its phase noise, it makes sense to choose a smaller K_{VCO} for low phase noise. Fig. 7 shows the proposed LC-VCO circuit, where an on-chip inductor (L = 1.2nH) is used to build a resonant circuit. A switched capacitor array tunes the oscillation frequency. This capacitor array consists of a variety of switched capacitor units, and a 5-bit digital signal *SW<4:0>* controls on/off states in all capacitor units.

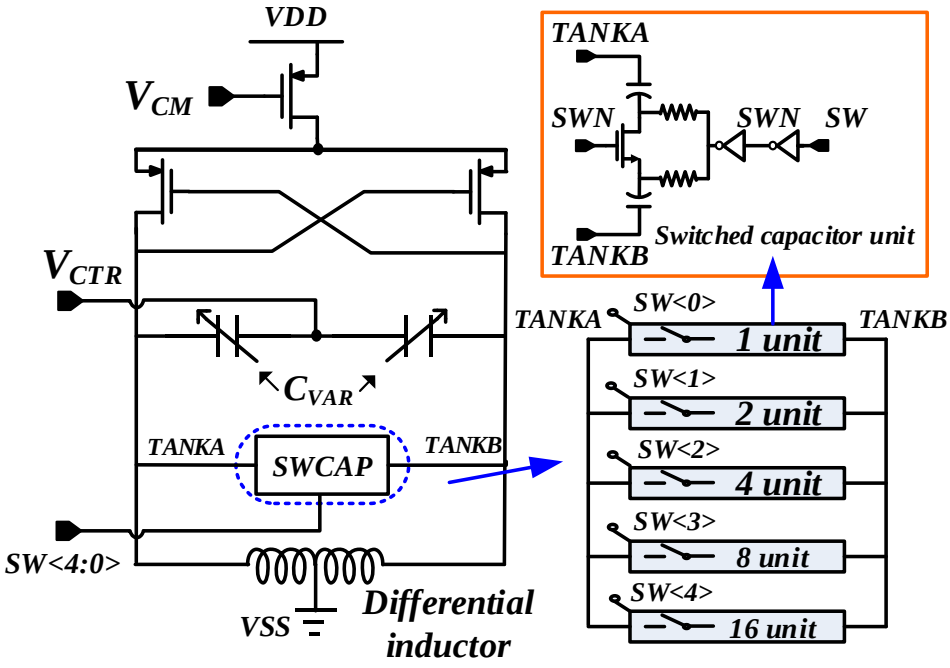


Fig. 7. A LC-VCO circuit with a digital controlled capacitor array

The total capacitance of the resonant circuit is expressed as

$$C_{TOTAL} = C_{VAR} + \sum_{i=0}^{i=4} 2^i \{SW\langle i\rangle \times C_{MIN} + SWN\langle i\rangle \times C_{MAX}\} \quad (7)$$

Here C_{VAR}, C_{MIN}, and C_{MAX} represent the voltage control capacitor value, the digital controlled capacitor values when a switch is on and off, respectively. The capacitor switches in Fig. 7 are turned on when $SW<i>$ = 1 and $SWN<i>$ = 0. Equation (8) models how the minimum and maximum VCO frequencies (F_{MIN} and F_{MAX}) vary with the total capacitance.

$$\begin{cases} F_{MIN} = \dfrac{1}{2\times\pi\times\sqrt{L\times C_{TOTAL,MAX}}} \\ F_{MAX} = \dfrac{1}{2\times\pi\times\sqrt{L\times C_{TOTAL,MIN}}} \end{cases} \quad (8)$$

Due to process, voltage and temperature (PVT) variations, the capacitance range needs to be wider to compensate the impact of PVT variations. In this design, 32 resonant points are sufficient to cover the entire frequency range (5.7~6.0 GHz). Therefore, the frequency interval between two adjacent points is about 10MHz. when V_{CTR} is between 0.4V and 1.1V, K_{VCO} is expected to be at least 15MHz/V. In order to ensure a low reference spur and continuous VCO frequency range, K_{VCO} was designed as 30MHz/V and 45MHz/V for $SW<4:0>$ = 00000 and 11111, respectively.

E. Automatic frequency calibration (AFC)

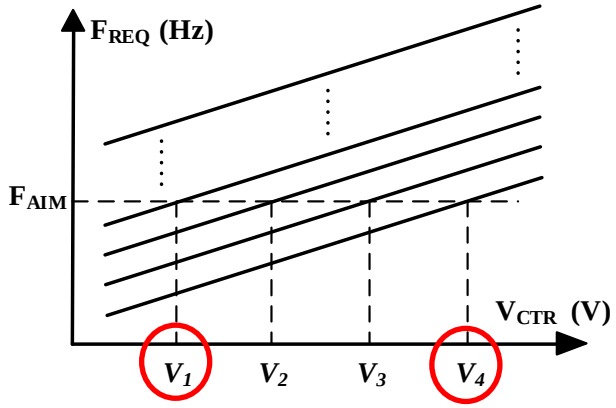


Fig. 8. PLL's aim frequency (F_{AIM}) versus the VCO control voltage (V_{CTR})

As illustrated in Fig. 8, due to the use of smaller K_{VCO}, adjacent VCO tuning points are very close. For a targeted frequency (F_{AIM}), a PLL has four possible locking points, which correspond to four switch capacitors and four V_{CTR} values. V_1 or V_4 is not a good choice to minimize current mismatch in CP. In this design, an AFC is used to determine the proper operating point in a PLL with a wide frequency range [11-14]. Frequency locking may be random without a specific AFC algorithm, especially when adjacent tuning points are very close.

Fig. 9 shows a PVM circuit, which provides a voltage (V_{PRE}) to VCO in an AFC process. When AFC begins, the PVM is firstly enabled. Hence, V_{CTR} is initially set as V_{PRE}, which is usually the middle voltage of whole V_{CTR} range. Later, when the charge pump is activated, the PVM will be disabled for low power purpose. The AFC process described in Fig. 10 is responsible for finding appropriate tuning parameter $SW<4:0>$ and VCO control voltage V_{CTR}.

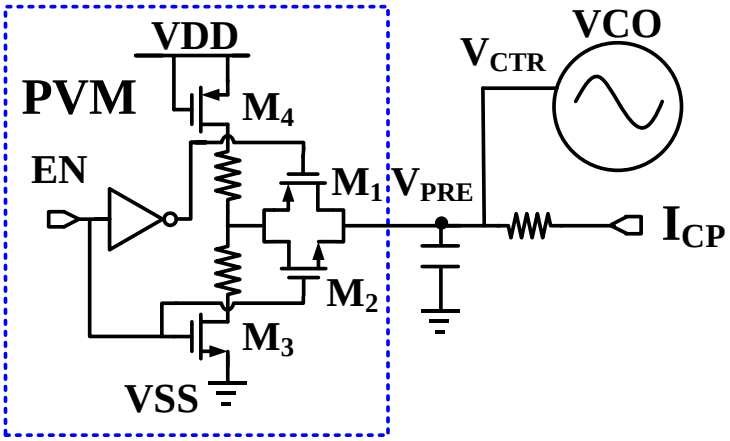


Fig. 9. The structure of *PVM* circuit and its connection to *VCO*

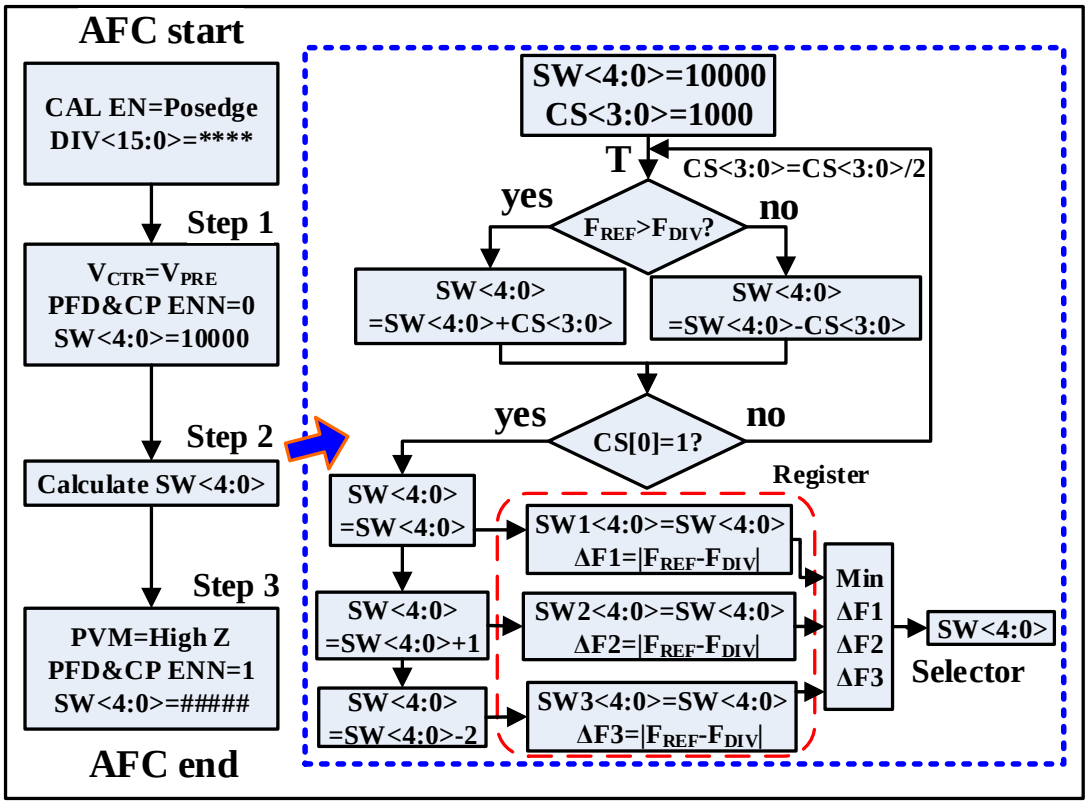


Fig. 10. Proposed flow chart of AFC algorithm

An AFC process starts after the signal (*CAL_EN*) is asserted and the division ratio is given. The main function in step 1 is initialization, where the CAL circuit has not enabled the PFD and CP. The PVM circuit forces V_{CTR} to VDD/2 and the *SW<4:0>* is set as 10000. Step 2 is the essential algorithm for calibration, which takes 7 cycles. In the first 4 cycles, a relatively accurate *SW<4:0>* is obtained through successive approximation. Then, in the next 3 cycles, the best configuration of switched capacitor units is determined. In step 3, the CAL circuit enables PFD and CP blocks. The PVM circuit is disabled. The obtained *SW<4:0>* will not change.

IV. Measurement Results and Discussion

Our PLL chip was fabricated with a standard 130nm CMOS technology, and was encapsulated in a QFN package. This package was mounted on a custom PCB for chip test. The measurement environment and the die micrograph are shown in Fig. 11. The total die area of this synthesizer is 0.56mm^2. Phase noise and reference spur were captured using an E4407B spectrum analyzer. Chip measurement results show that under a 1.5V supply voltage, the power dissipation with an output buffer of the PLL is 12mW.

This PLL is a part of a wireless transceiver chip. In order to better utilize chip area, there is no dedicated pad in the layout to enable direct measurement of PLL output. Instead, in this work, the PLL was configured to be directly connected to the transmitter. Then, without signal modulation, we measured the output of power amplifier (PA) using a spectrum analyzer. The existence of a PA in the signal path may slightly deteriorate the noise floor, but its contribution to phase noise is negligible. The phase noise of a PLL depends on loop bandwidth and noise of each circuit component. Since the delay time of PFD does not affect loop bandwidth nor contribute noise, during phase noise measurement, the delay time of PFD (*i.e.*, T_{ON}) was configured to be minimum. Fig. 12(a) plots the measured phase noise of our PLL system when an amplifier in CP. The phase noise is -65dBc/Hz at 10 KHz offset, -71dBc/Hz at 100 KHz offset, -109dBc/Hz at 1 MHz offset, and -135dBc/Hz at 10 MHz offset for 5.835 GHz output. Later, when this amplifier in CP was broken using Focused Ion Beam technology, the measured phase noise was shown in Fig. 12(b), where the phase noise is -66dBc/Hz at 10 KHz offset, -73dBc/Hz at 100 KHz offset, -108dBc/Hz at 1 MHz offset, and -133dBc/Hz at 10 MHz offset for 5.835 GHz output. Comparing Fig. 12(a) and (b), we can see that the mismatch current in CP is not very sensitive to phase noise.

Reference spur was measured and studied. When the delay time of PFD (*i.e.*, T_{ON}) was set to its minimum value (*i.e.*, 0.67ns), the measured reference spur is -68dBc as shown in Fig. 13(a). When the delay time of PFD (*i.e.*, T_{ON}) was reconfigured to its max value (*i.e.*, 1.82ns), according to the equation (4), reference spur is supposed to increase. This prediction was validated in the captured waveform of Fig. 13(b), where the measured reference spur is -64dBc. Next, the amplifier node V_O in the proposed charge pump was broken using focused ion beam technology. Consequently, the negative feedback loop was disconnected, and severe current mismatch occurred in the test chip. The captured output spectrum of this synthesizer in Fig. 13(c) shows that the reference spur is -50dBc, which is 14~19dB higher than our prior measurements. The above measurements successfully validate our proposed design methodology that a larger delay time of PFD and a less current mismatch lead to a reduction of reference spur.

Fig. 14 plots the measured VCO tuning range with a 5-bit control register *SW<4:0>*, which corresponds to 32 coarse tuning curves. If *SW<4:0>* was set to 00000, the measured VCO gain (K_{VCO}) was about 30MHz/V. If *SW<4:0>* was set to

11111, the measured VCO gain (K_{VCO}) was about 45MHz/V. The minimum frequency spacing between two adjacent curves is 11MHz. When the voltage lock range is within 0.4~1.1V, the covered frequency range is 5.7~6 GHz.

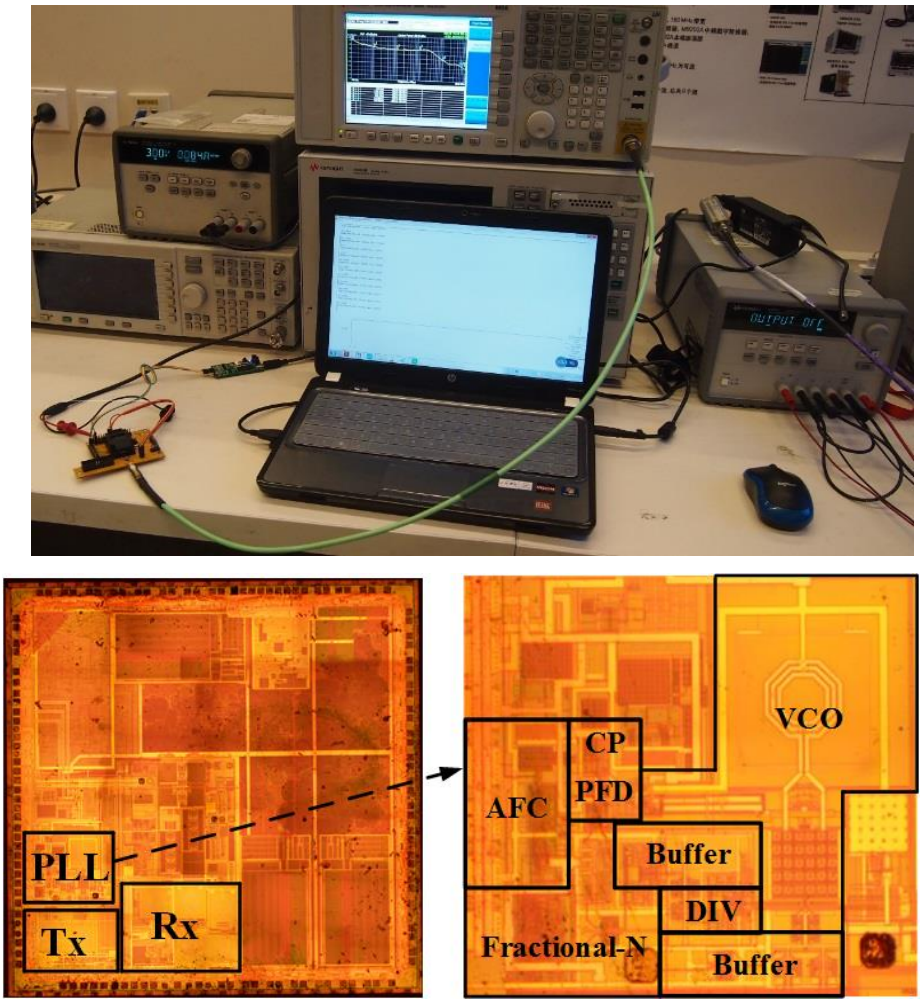
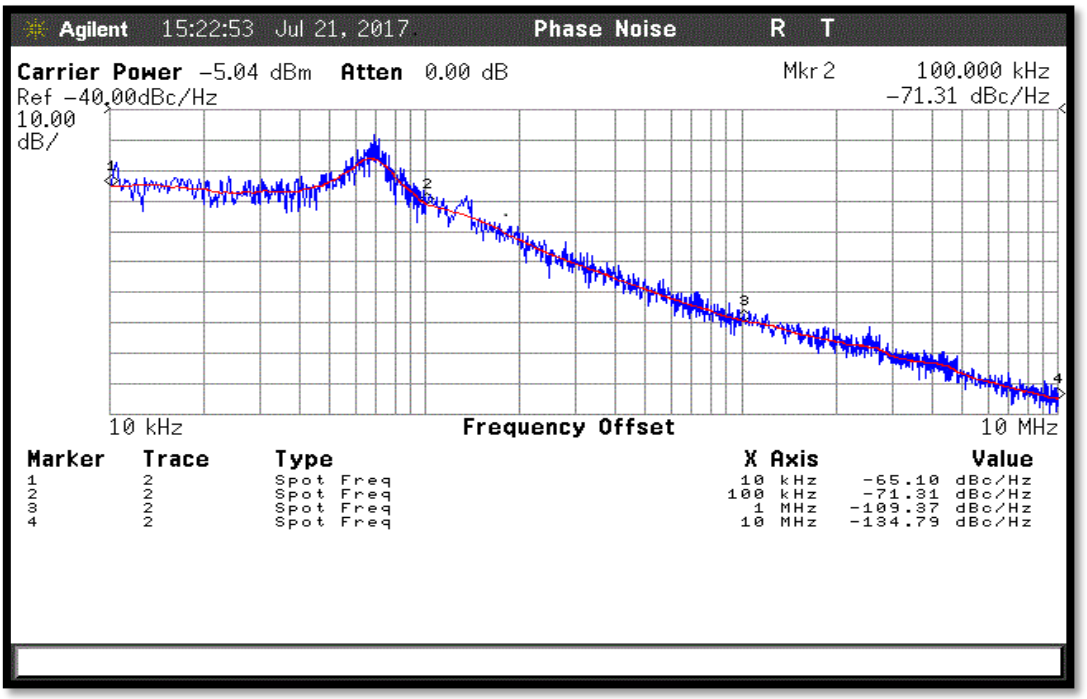
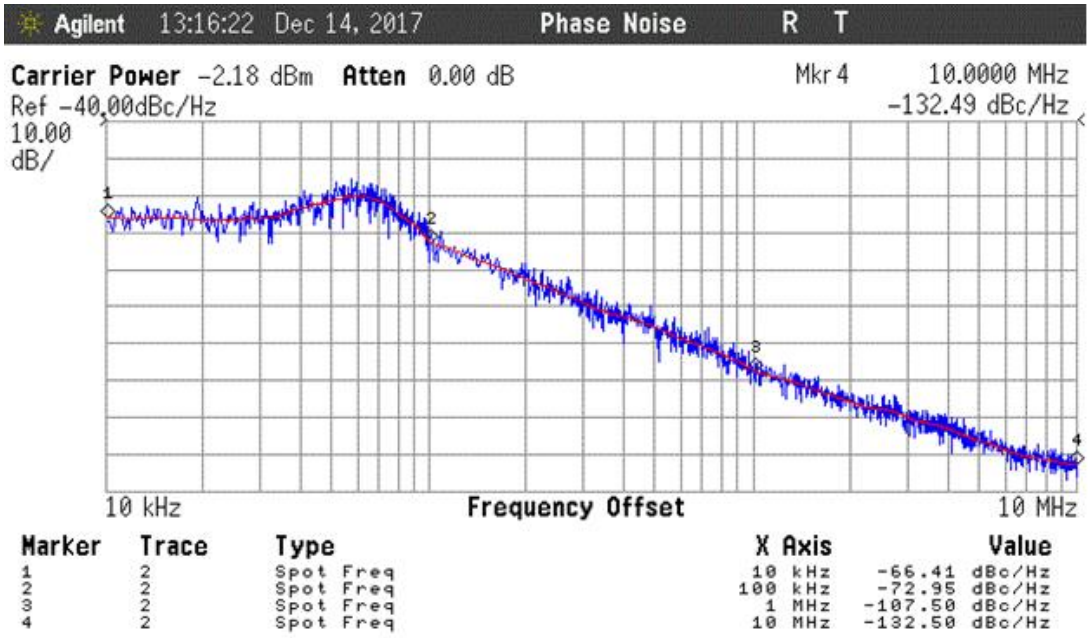


Fig. 11. Measurement environment and die microphotograph.

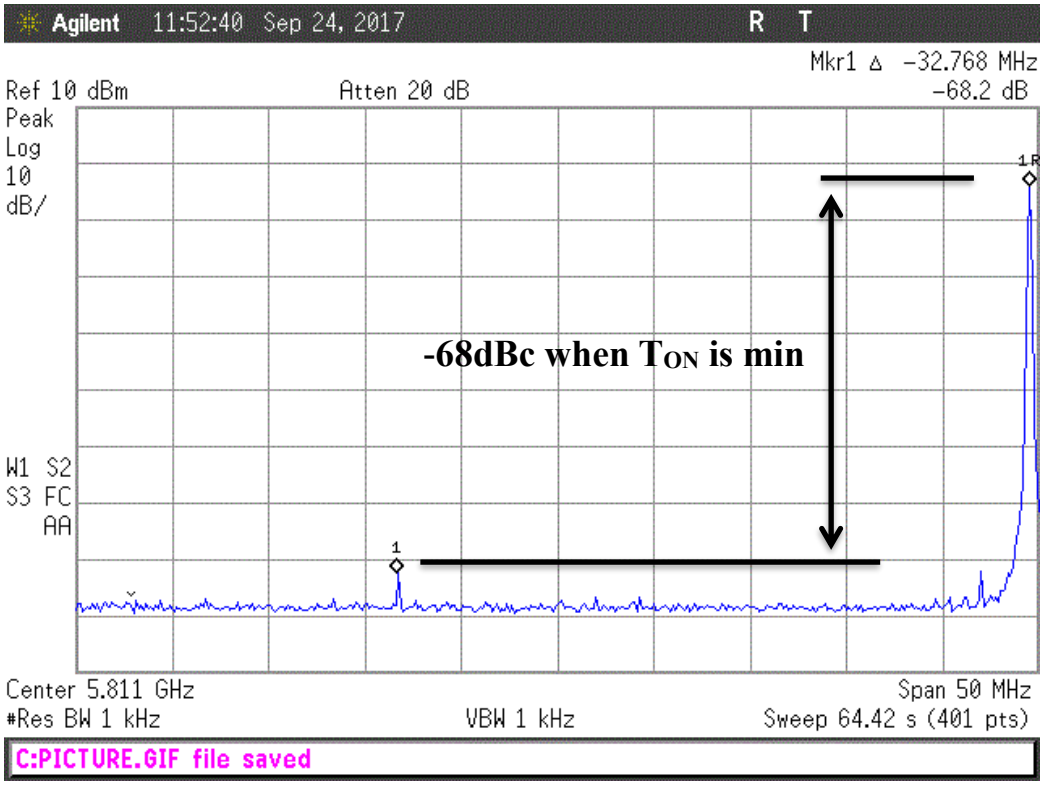


(a)



(b)

Fig. 12. (a) Measured PLL phase noise at 5.835 GHz with an amplifier in CP, (b) measured PLL phase noise at 5.835 GHz without an amplifier, where Focused Ion Beam (FIB) was used to break the amplifier in CP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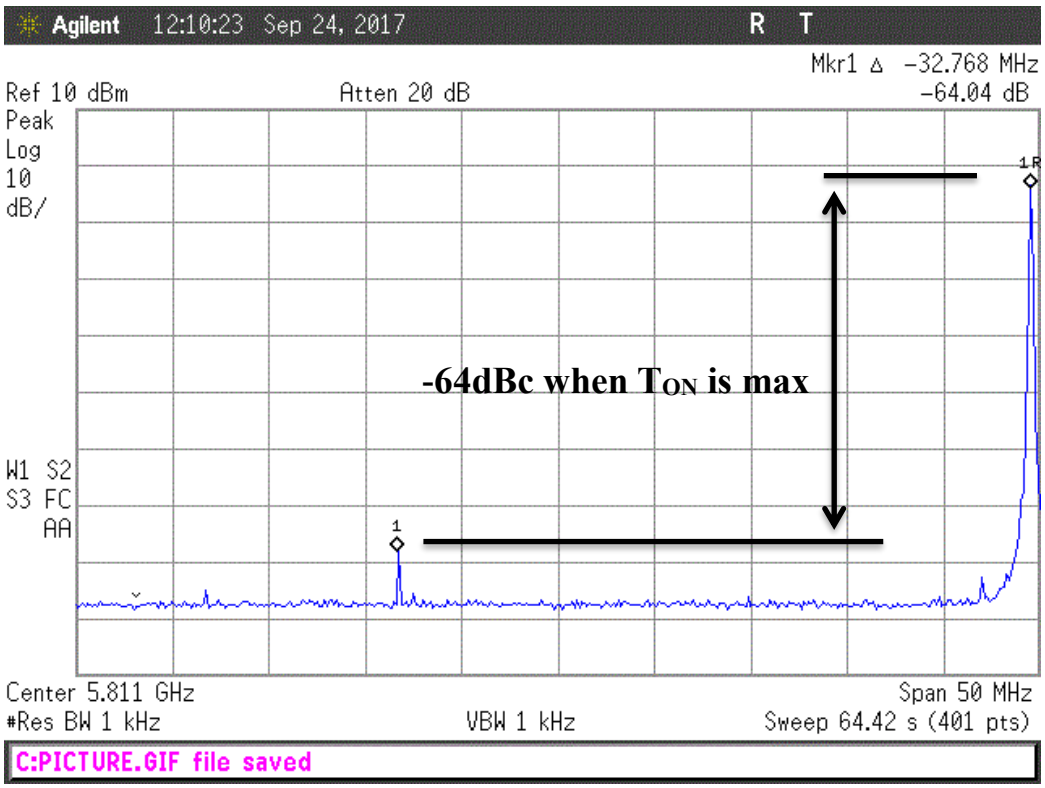
(a)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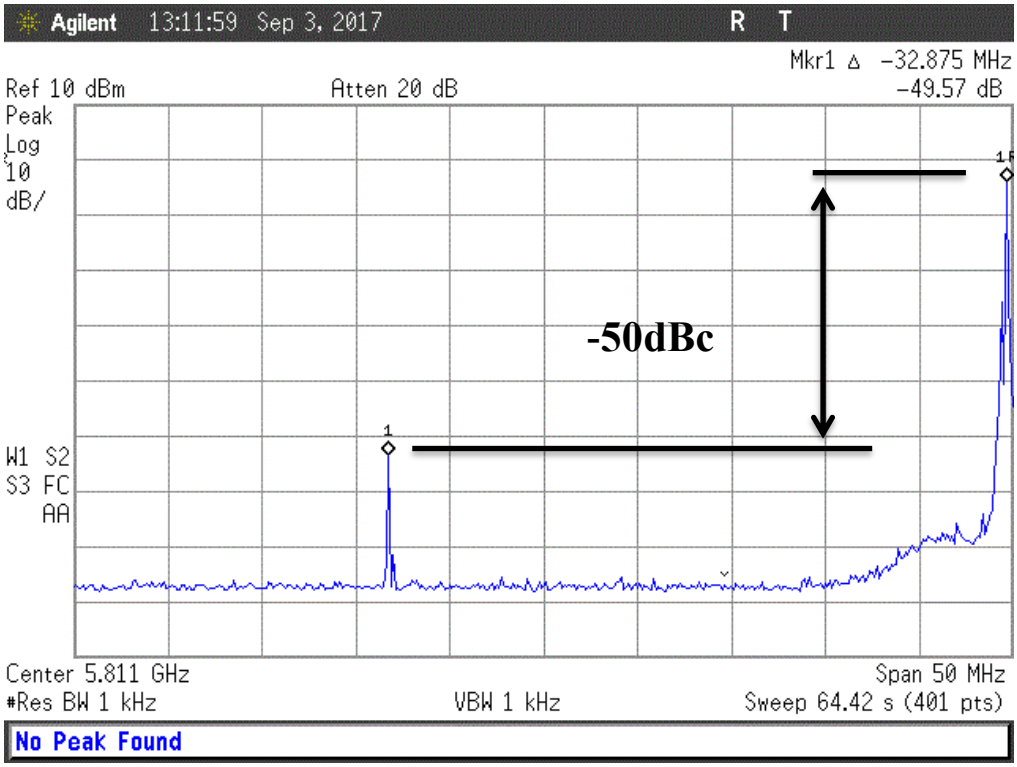
(b)



(c)

Fig. 13. (a) Measured output spectrum of the synthesizer with an amplifier in CP and T_{ON} is minimum, (b) measured output spectrum of the synthesizer with an amplifier in CP and T_{ON} is maximum, and (c) measured output spectrum of the synthesizer without an amplifier, where Focused Ion Beam (FIB) was used to break the amplifier in CP

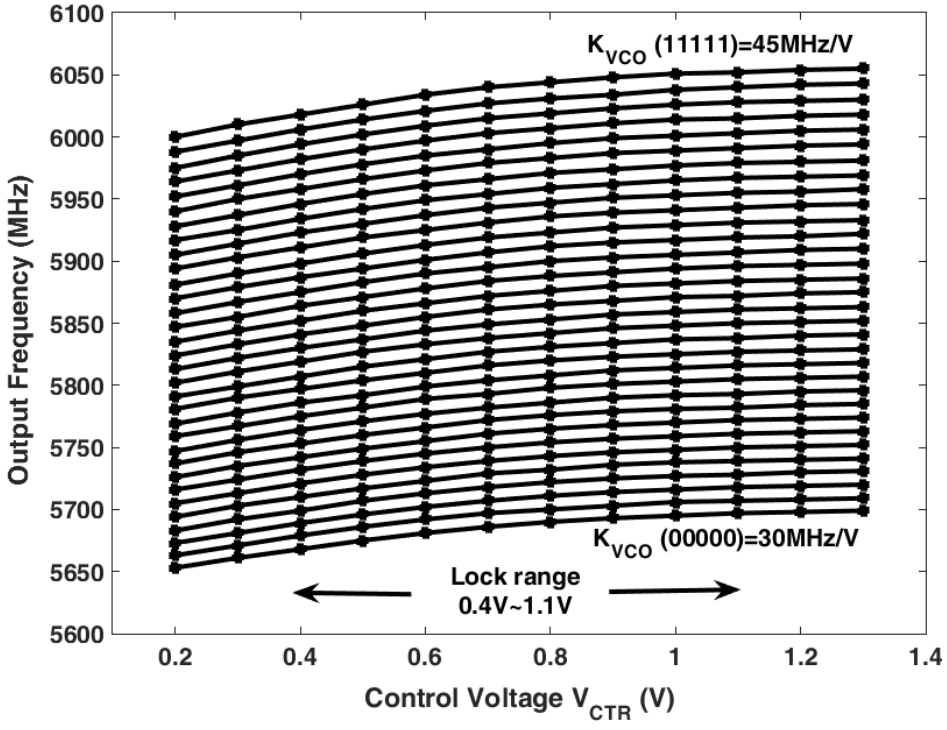


Fig. 14. Measured VCO tuning range with a 5-bit control register

Table II summarizes the measured performance results of this proposed PLL and compares with existing PLL designs [9, 15-22] in the literature. The fabrication technology, supply voltage, frequency range, power consumption, chip area, phase noise, and reference spur are listed in Table II. Regarding the phase noise, our proposed design achieves the lowest phase noise. Meanwhile, the reference spur (*i.e.*, -68dBc) is at least 17% lower than these state-of-the-art designs in [9, 15-20]. In addition, our proposed design has advantages in chip area and phase noise over the design [21], while the reference spur is very close to each other. In contrast with [22], the measurement results of phase noise are very close. Yet, our proposed design outperforms in power consumption, chip area, and reference spur.

TABLE II. Summary of comparison with other state-of-the-art PLL designs

Reference	[9]	[15]	[16]	[17]	[18]	[19]	[20]	[21]	[22]	This work
Fabrication Technology	0.13μm CMOS	0.18μm CMOS	0.18μm CMOS	65nm CMOS	0.18μm CMOS	0.13μm CMOS	0.18μm CMOS	65nm CMOS	65nm CMOS	0.13μm CMOS
Supply Voltage (V)	1.3	N/A	1.8	N/A	0.6	0.5/0.8	1.8	0.5	0.85	1.5
Frequency Range (GHz)	2.4	5.4~5.56	5.7~6.0	5.8	2.4~2.64	8.8~9.2	5.15~5.35	5.95	1.152	5.7~6.0
Power Consumption (mW)	10.7	9.23	36	11	14.4	12	18	0.69	19.8	12
PLL Chip Area (mm^2)	0.31	0.399	N/A	0.133	1.68	1.21	1.045	0.74	0.6	0.56
Phase Noise @1MHz (dBc/Hz)	-96	-85	N/A	-110	-104	-104.5	-104	-98	-109.8	-109
Phase Noise @10MHz (dBc/Hz)	N/A	-117	N/A	-122	-130	N/A	N/A	-129	-134.8	-135
Reference Spur (dBc)	-31.5	-51	N/A	-45	-39.8	-58	-40	-71	>-57	-68

V. CONCLUSION

This paper presents a PLL for a low phase noise and reference spur. Reference spur is suppressed through reducing the current mismatch in charge pump, introducing a delay time controllable PFD, and adopting a low gain VCO. The PLL frequency is 5.7~6.0 GHz. The measured power consumption is 12mW, the reference spur is

-68dBc, and the phase noise is -109dBc/Hz and -135dBc/Hz at 1MHz and 10MHz offset respectively for 5.835 GHz output. In addition, a 5-bit register enables 32 tuning points for a switched capacitor array, which ensures accurate PLL frequency locking. Compared with existing designs in the literature, the measured reference spur is improved by at least 17%, and the PLL achieves the lowest phase noise.

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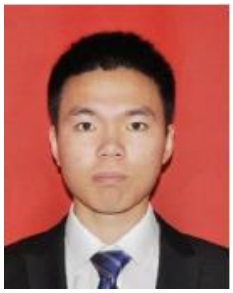

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