A 5.8 GHz 1 V Linear Power Amplifier Using a Novel On-Chip Transformer Power Combiner in Standard 90 nm CMOS

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***Abstract*—A fully integrated 5.8 GHz Class AB linear power amplifier (PA) in a standard 90 nm CMOS process using thin oxide transistors utilizes a novel on-chip transformer power combining network. The transformer combines the power of four push-pull stages with low insertion loss over the bandwidth of interest and is compatible with standard CMOS process without any additional analog or RF enhancements. With a 1 V power supply, the PA achieves 24.3 dBm maximum output power at a peak drain efficiency of 27% and 20.5 dBm output power at the 1 dB compression point.**

***Index Terms*—CMOS power amplifier, power amplifiers, power combiners.**

I. Introduction

THE need for ubiquitous wireless communication systems during the past decade has been a key driver in the development of high frequency low cost integrated circuit building blocks. High levels of integration are desired to achieve a smaller form factor and reduce cost in high volume applications. CMOS technology is the prime contender for achieving this level of integration. Though most of the radio frequency (RF) building blocks have been successfully integrated into CMOS process, the power amplifier (PA) is mostly implemented in a different process technology. Although several advances have been recently made on the design and implementation of CMOS PAs [1]–[3], it still remains the bottleneck in achieving a true single-chip radio solution. The major obstacles in modern deep-submicron CMOS process are the low breakdown voltage and the high knee voltage of transistors. This directly limits the swing available across a given load, thereby limiting the available output power as well. The other major challenge is the loss of on-chip passives in a common digital CMOS process, due to the conductive substrate and the absence of an ultra-thick metal (UTM) option. Power combining is an attractive solution and considerable research efforts have been invested in the last few years in the development of on-chip power combining PAs in CMOS process [3], [4]. In this paper, we describe a novel transformer-based lateral power combiner, which is well-suited for implementation in a low-voltage digital CMOS process, having no RF process enhancements [5]. Various properties of the proposed combiner like efficiency and impedance transformation are analyzed in depth and proper design guidelines provided. Using the power-combiner, a fully integrated Class AB power amplifier has been demonstrated, that can achieve a saturated power level of 24.3 dBm, while operating from a 1 V supply. An important distortion-generating mechanism in a Class AB power amplifier, the power-supply modulation effect, has been analyzed in detail for the designed PA.

The paper is organized as follows. Section II describes the proposed transformer power combiner and its properties, Section III deals with the Class AB power amplifier design using the combiner, Section IV presents an analysis of power supply modulation effects in the designed PA, while Section V presents the measurement results.

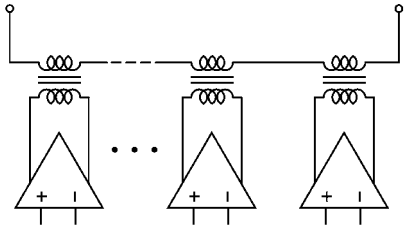

Fig. 1. Power combining network principle.

II. Transformer-Based Power Combiner

The principle of transformer-based power combining is shown in Fig. 1 where the secondary coils of N transformers are connected in series and their primaries are driven by separate differential amplifiers. Thus, the primaries can be driven with low voltages, while the AC voltages add up on the secondary side, generating higher output power.

Transformer based power combiners have been demonstrated before utilizing "slab" inductors to realize a distributed active transformer [4]. However this double-differential structure relies on the creation of virtual grounds, necessitating all the

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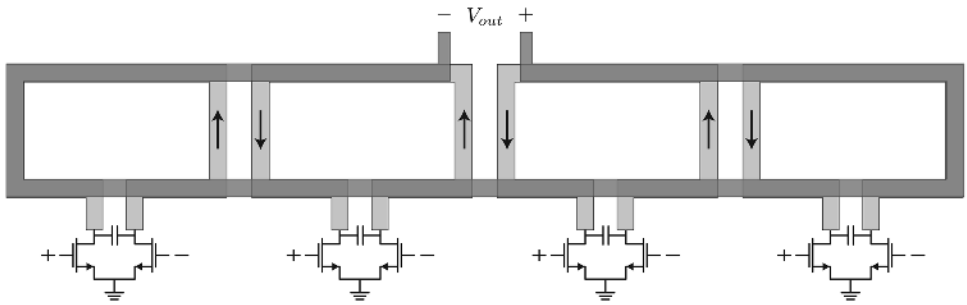

Fig. 2. A simple power combining transformer layout.

eight stages to remain on at all times, preventing efficiency enhancement at power back-off [3]. However, it is possible to design a transformer power-combiner by connecting the secondary windings in series, where each amplifier stage is independent of the others and the structure does not rely on the creation of virtual grounds. A major benefit of this architecture is simple power control. Since each amplifier stage driving the primary operates independently, some of the amplifier stages can be turned off when delivering lower output power. This leads to efficiency enhancement at backed-off power and has been demonstrated already in [3]. The structure proposed in this work also allows power control, however compared to [3], it does not use any additional process option, but relies on a new topology to realize low insertion loss of the combiner.

A. Proposed "Figure 8" Power Combiner Architecture

In Fig. 2 a simple power combining structure with rectangular loop inductors is shown. In this simple transformer layout, the adjacent primary windings carry currents in opposite directions, and thus do not contribute much flux and coupling to the secondary. To minimize this internal flux cancellation, the space between the adjacent windings can be increased. At the expense of area, this is an effective approach and an efficient dual layer approach has been demonstrated in [3]. However [3] uses special RF process options with two thick metal layers. With a single thick metal layer, as is commonly the case in digital CMOS process, a lateral structure is better suited, where the primary and secondary coils lie in the same metal layer next to each other. There are several problems coming up with such a power combining network. The biggest problem is the low magnetic coupling factor between the primary and secondary windings even with minimum metal spacing. Secondly, since the metal spacing is small, capacitive coupling increases and degrades the quality factor of the coil. In addition, a major shortcoming of the lateral transformer structure is current crowding at the inner conductor edges due to proximity effect. This in turn increases the resistance of the structure and lowers the quality factor, resulting in lower transformer efficiency. Thus, the efficiency of a simple lateral transformer configuration is poor.

In this paper, a novel transformer based lateral power combiner is presented, which alleviates most of the problems mentioned above and achieves very low insertion loss over the bandwidth of interest. A new "figure 8" structure [6] as shown in Fig. 7 has been utilized.

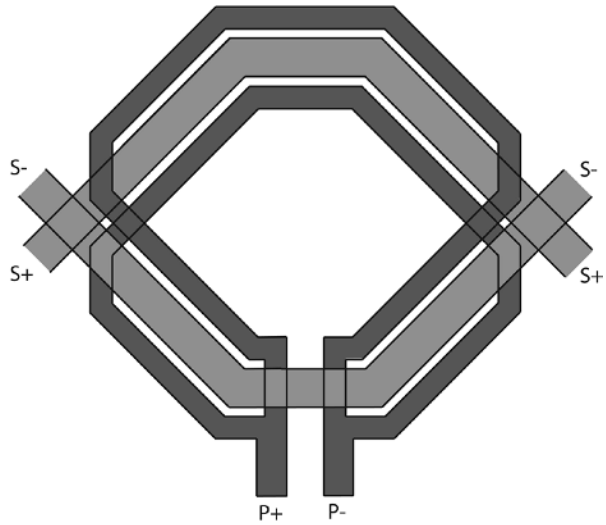

Fig. 3. Layout of each ring consists of two parallel primary coils and one secondary coil.

Each individual differential power amplifier drives the primary but the secondary is implemented in *alternating orientation*, resembling an "8". This layout minimizes the effects of internal flux cancellation because now the currents in the primaries of two adjacent stages are forced to flow in the same direction. This results in better coupling and significant efficiency improvement. An additional benefit stems from the alternating direction of the secondary windings. The secondary loop is now immune to common mode coupling from a distant source since the incoming magnetic flux induces voltages of opposite polarity across each section of the "figure 8". It is thus advantageous to employ an even number of stages. A third important feature of the proposed structure is the use of two parallel coils for each primary, as shown in Fig. 3. Because of the presence of primary windings on either side of each secondary winding, the current crowding effect discussed earlier is mitigated. In the case of a single primary, the edge of the secondary winding, closer to the primary takes the bulk of the current, resulting in higher loss resistance. Now, the current is spread more uniformly in the secondary, reducing the loss substantially.

The final feature of this combiner is the minimization of eddy current losses in the surrounding metal structures. In the layout of the amplifier, it is convenient to place a ground ring around the inductor to provide low inductance paths to supply rails for the amplifier bypass capacitors. This loop lowers the quality

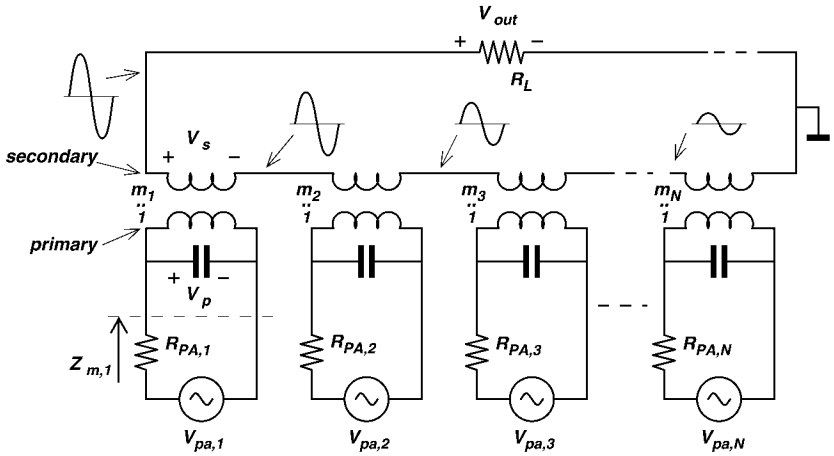

Fig. 4. Equivalent circuit for power combining network.

factor of the transformer due to induced eddy currents. The eddy currents arise from the magnetic leakage due to the imperfect coupling between primary and secondary loops. By alternating the orientation of the secondary loops, the eddy currents are suppressed substantially, allowing a more practical layout to be realized.

B. Impedance Transformation

The power combiner, in addition to efficiently summing the ac voltages of the individual amplifiers, also performs an impedance transformation. Fig. 4 shows N transformers with their secondary windings connected in series. It is important to realize that the secondary winding of each transformer therefore carries the same current $V_{\rm out}/R_L$. As such, all power amplifiers are coupled to each other. In other words, the impedance seen by each PA is also determined by the output voltage and output impedance of all other amplifiers.

To obtain an expression for the impedance Z_m, seen by each PA, one first has to find an expression for the current in the primary winding of the transformers. This current can be obtained by using the superposition theorem. Assume that the turn ratio of transformer j is $1:m_j$, and its primary is driven by an amplifier represented by its Thevenin equivalent voltage source $V_{pa,j}$ and output impedance $R_{PA,j}$. Then, the primary current in transformer j, when only considering voltage source $V_{pa,j}$, can be written as

$$i_{p,j,j} = \frac{m_j^2 V_{pa,j}}{R_L + \sum_{i=1}^{N} m_i^2 R_{PA,i}}. \tag{1}$$

Likewise, the primary current in transformer j when only considering voltage source $V_{pa,k}$ can be written as

$$i_{p,j,k} = \frac{m_j m_k V_{pa,k}}{R_L + \sum_{i=1}^{N} m_i^2 R_{PA,i}}. \tag{2}$$

Summing all these contributions, according to the superposition theorem, leads to the following expression for the current in the primary winding of transformer j

$$i_{p,j} = m_j \frac{\sum_{i=1}^{N} m_i V_{pa,i}}{R_L + \sum_{i=1}^{N} m_i^2 R_{PA,i}}. \tag{3}$$

Since $i_{p,j}$ can also be written as

$$i_{p,j} = \frac{V_{pa,j}}{R_{PA,j} + Z_{m,j}} \tag{4}$$

the transformed load impedance, $Z_{m,j}$, as seen by power amplifier j can now be written as

$$Z_{m,j} = \frac{V_{pa,j}}{i_{p,j}} - R_{PA,j} \tag{5}$$

$$= \frac{\left(R_L + \sum_{i=1}^{N} m_i^2 \cdot R_{PA,i}\right) \cdot V_{pa,j}}{m_j \cdot \sum_{i=1}^{N} m_i \cdot V_{pa,i}} - R_{PA,j}. \tag{6}$$

It can clearly be seen that the transformed load impedance $Z_{m,j}$ depends on both the output impedance and output voltage (both magnitude and phase) of each PA, which can be considered as a form of *load-pull*.

When all power amplifiers have the same output impedance, generate the same output voltage, and all transformers use the same winding ratio m, (5) simplifies to a resistive value of

$$R_m = \frac{R_L}{N \cdot m^2}. \tag{7}$$

The impedance seen by each amplifier is now determined by two factors only: the turn ratio m of each transformer and the number of parallel stages N. Note that it is independent of output impedance of the other power amplifiers. Under the same conditions, the total output power, delivered to the load, equals

$$P_o = N^2 \cdot m^2 \cdot \frac{V_{pa}^2}{2R_L} \tag{8}$$

and the impedance transformation ratio is defined as

$$r = \frac{R_L}{R_m} = N \cdot m^2. \tag{9}$$

From (8), it can be seen that the output power can be increased either by increasing m or N. On the other hand, (9) shows that the impedance transformation ratio increases only linearly with N but quadratically with m. It is well known that in practice a high transformer turn ratio, i.e., a high m, also results in a

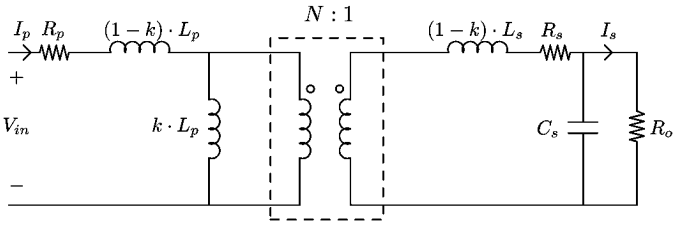

Fig. 5. Simplified model of a transformer.

high insertion loss [4]. Therefore, it is far more efficient to increase the number of stages N, rather than increasing m. Such an approach achieves a high output power with a rather moderate impedance transformation ratio. This is an important aspect in low-voltage PA design.

Since this power combiner uses four $(N = 4)$ independent 1:1 $(m = 1)$ transformers with their secondaries connected in series, the impedance transformation ratio r is equal to 4 and each differential pair sees a transformed impedance of $R_L/4$.

C. Optimum Sizing and Insertion Loss of Power Combiner

The efficiency of the designed power combiner depends upon a number of factors like coupling between the primary and secondary windings, the quality factor of the windings, the values of winding inductances and the tuning mechanism. In order to develop a proper insight into the design of the power combiner, it is necessary to develop a mathematical equation based on a simplified model as shown in Fig. 5, [4]. The efficiency analysis can be simplified by concentrating on one of the four transformer stages, keeping in mind that R_o shown in Fig. 5 is equal to R_L divided by four. To a first order, the efficiency of a four way combiner is same as that of the single stage. In this design, we use a shunt capacitor and not a series capacitor on the secondary side to tune out the inductance.

Fig. 5 shows a simplified model of a transformer, where L_p, L_s are the primary and secondary winding inductances with series loss represented by R_p, R_s, k is the coupling coefficient between primary and secondary windings, R_o is the load resistance for a single stage and C_s is the shunt tuning capacitance. For our 1:1 case, we assume $L_p = L_s$.

We can convert the shunt capacitor-resistor network into an equivalent series network given by

$$R_{\text{eq}} = \frac{R_o}{1+(\omega R_o C_s)^2} \tag{10}$$

$$C_{\text{eq}} = \frac{1+(\omega R_o C_s)^2}{\omega^2 {R_o}^2 C_s}. \tag{11}$$

The efficiency η of the power combiner can be written as

$$\eta = \frac{P_{\text{load}}}{P_{\text{load}} + P_{\text{diss}}} \tag{12}$$

where P_{load} and P_{diss} are the power delivered to the load and power dissipated in the parasitic resistance of the combiner.

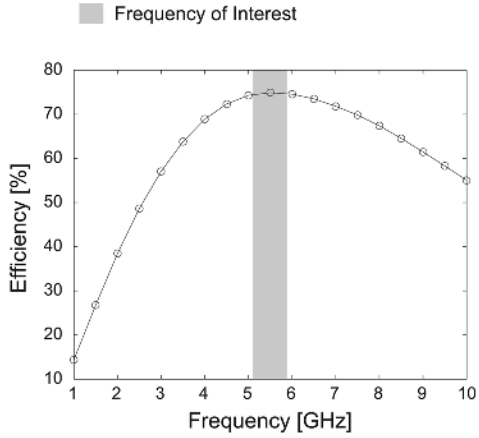

Fig. 6. Efficiency of the power combining network in the band of interest.

Putting values of P_{load} and P_{diss} in the above equation, the value of efficiency can be simplified as

$$\eta = \frac{\frac{1}{1+(\omega R_o C_s)^2} R_o}{\frac{1}{1+(\omega R_o C_s)^2} R_o + R_s + \left|\frac{Z_s + j\omega k L_p}{j\omega k L_p}\right|^2 R_p} \tag{13}$$

where Z_s is the secondary side impedance transformed to the primary side.

The efficiency can be maximixed by setting

$$\omega L_s = \frac{1}{\omega C_{\text{eq}}} \tag{14}$$

assuming $L_p \simeq L_s$. Note that because we use shunt tuning and not series tuning, the value of the tuning capacitor depends on the load resistor, even for a fixed size transformer at a given frequency.

In order to find the optimum winding inductance, we can take a derivative with respect to L_p [4] and set $(\partial\eta)/(\partial L_p)$ to zero. This gives us the optimum inductance value as

$$\omega L_s \simeq \omega L_p = \frac{\alpha}{1+\alpha^2} R_o \tag{15}$$

where

$$\alpha = \frac{1}{\sqrt{\frac{1}{{Q_s}^2} + \frac{Q_p}{Q_s} k^2}} \tag{16}$$

and Q_p and Q_s represent the quality factor of primary and secondary windings.

The above equation also fixes the transformer size, since for an octagonal winding shape at a given frequency, a given inductance value corresponds to a fixed winding diameter, which can be determined using an EM solver.

Using the optimum inductance value and writing the parasitic winding resistances using winding quality factor (Q), the optimum efficiency is derived as

$$\eta_{\max} = \frac{1}{1 + \frac{2}{Q_p Q_s k^2} + 2\sqrt{\frac{1}{Q_p Q_s k^2}\left(1 + \frac{1}{Q_p Q_s k^2}\right)}}. \tag{17}$$

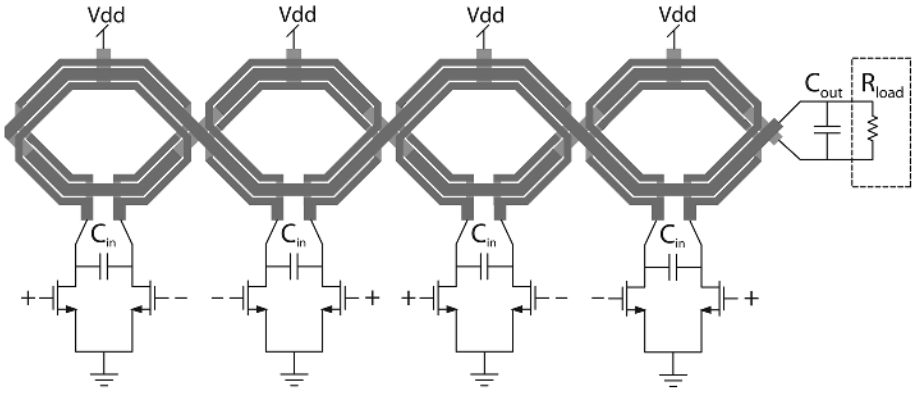

Fig. 7. Simplified schematic of final PA with the implemented "figure 8" power combining network.

This analysis provides the optimum transformer size and tuning capacitor values and shows the efficiency can be increased by either increasing the quality factor of the windings or by increasing the coupling between the primary and secondary windings.

D. Simulation Results

Full wave electromagnetic simulation has been performed using Agilent Momentum. Only the top metal layer was used for the windings while the underpass elements were realized with the lower metal layers. The insertion loss of the power combiner is 1.35 dB (75%) as shown in Fig. 6 and varies by only 0.4% over the band of interest. The proposed combiner is one of the smallest reported (0.65 mm× 0.15 mm), even compared to a 20 GHz combiner [7]. While the efficiency is not the highest reported, it should be noted that no special options like gold metal or thick metal layers were used.

III. Class AB Power Amplifier

The power combiner designed above was used to build a four stage differential Class AB power amplifier. The intended application for the power amplifier is a system which uses variable envelope modulation, requiring linearity. Class AB gives the best compromise between linearity and efficiency and hence was chosen as the preferred topology. The power combining network described in the previous section also acts as a differential-to-single-ended converter and removes the need of any off-chip balun to drive a single-ended antenna. Moreover, transformer based operation helps to eliminate the need of dc blocking capacitors and RF chokes at the output of each differential pair, leading to considerable area saving.

Since the supply voltage of each stage is 1 V, each transistor has to deliver significant amount of current (200 mA) to deliver the required power. Load pull simulations were performed to choose the optimum widths of the devices (1.2 mm) to get maximum output swing and efficiency. Fig. 7 shows the simplified schematic and layout of the implemented PA. Custom finger metal-oxide-metal ("MOM") capacitors ($C_{\rm in} = 2.6$ pF and $C_{\rm out} = 610$ fF) have been used for tuning the primary and secondary windings of the transformer respectively. To minimize the supply and ground bounce, large bypass capacitors (20 pF per stage) are needed. A combined NMOS/finger capacitor has been utilized for this function.

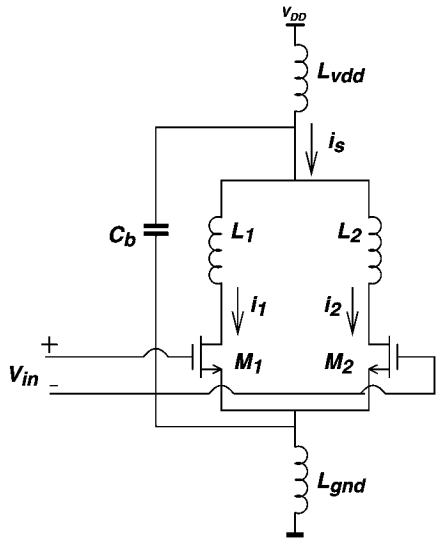

Fig. 8. Simplified circuit of a differential Class B amplifier with on-chip bypass capacitor (C_b) and supply line inductance (L_{vdd}).

IV. Power Supply Modulation Effect

Unwanted power supply modulation, due to a non-zero power supply impedance, is an important effect which causes IM3 degradation and distortion in reduced conduction angle power amplifiers (like B, AB), unless proper care is taken. Particularly in modern wireless era, with an urge to integrate everything on-chip, this effect needs to be analyzed carefully. In a Class-AB differential power amplifier, the DC current drawn from the supply is dependent on the envelope of the RF input voltage. In addition, in a two-tone test, a low-frequency signal current at a frequency equal to the tone spacing is also drawn from the supply. For simplicity, the supply rail modulation effect will be discussed for a Class B amplifier, and the effect in Class AB amplifiers will be very similar.

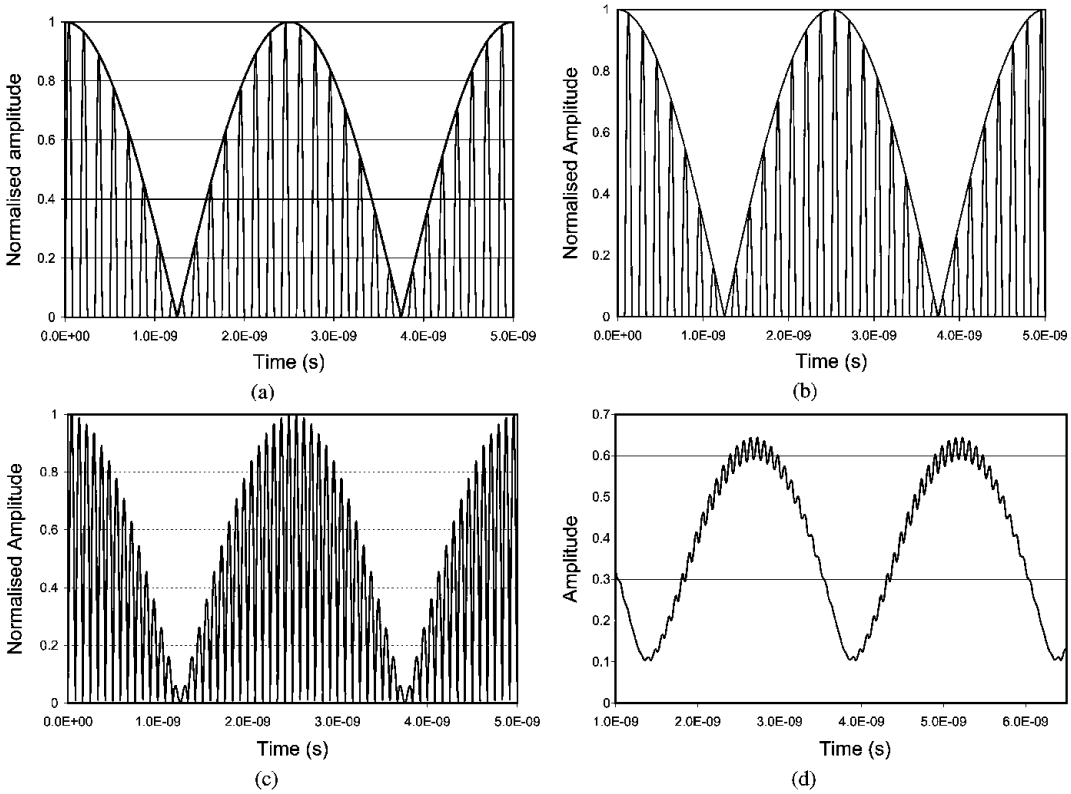

Fig. 9. (a) Drain current waveform of M1, operating in Class B, under two-tone excitation. (b) Drain current waveform of M2. (c) Sum of drain currents of M1 and M2. (d) Supply current after on-chip bypassing.

If two tones at frequencies ω_1 and ω_2 are applied to the input of the amplifier, then the input voltage V_{in} may be represented as

$$\begin{aligned} V_{\text{in}} &= A\sin(\omega_1 t) + A\sin(\omega_2 t) \\ &= 2A\cos\left(\frac{\omega_1-\omega_2}{2}\right)t\sin\left(\frac{\omega_1+\omega_2}{2}\right)t \\ &= 2A\cos(\omega_m t)\sin(\omega_c t) \end{aligned} \tag{18}$$

where ω_m is the modulation frequency and ω_c is the RF carrier frequency. The modulation frequency ω_m is related to the tone spacing $\omega_s(=\omega_1-\omega_2)$ as

$$\omega_m = \frac{1}{2}\omega_s. \tag{19}$$

In a Class B amplifier, the RF current of a single transistor (M_1 in Fig. 8) is a half-wave rectified sinusoid. Under a two-tone excitation, the RF drain current is a rectification of the modulated input waveform. The drain current of transistor M_1 (in Fig. 8) is shown in Fig. 9(a) for a sample case where the two applied tones are at frequencies 5.8 GHz and 6.2 GHz. The differential counterpart (current of M_2) is shown in Fig. 9(b). The sum of these two transistor currents is a full wave rectified sinusoid whose amplitude is modulated by the magnitude of a low-frequency cosine wave, as shown in Fig. 9(c). This current can be mathematically expressed as

$$\begin{aligned} i_s &= i_1 + i_2 \\ &= k|\cos(\omega_m t)||\sin(\omega_c t)| \end{aligned} \tag{20}$$

where k is a scaling constant. Replacing each term in the above equation by its corresponding Fourier series representation, we get

$$\begin{aligned} i_s &= k\left(\frac{2}{\pi} + \frac{4}{\pi}\frac{\cos(2\omega_m t)}{3} - \dots\right) \\ &\quad \times \left(\frac{2}{\pi} - \frac{4}{\pi}\frac{\cos(2\omega_c t)}{3} - \dots\right) \\ &= k\left(\dots - \frac{8}{\pi^2}\frac{\cos(2\omega_c t)}{3} \right. \\ &\quad \left. + \frac{8}{\pi^2}\frac{\cos(2\omega_m t)}{3} - \dots\right) \\ &= k\left(\dots - \frac{8}{\pi^2}\frac{\cos(2\omega_c t)}{3} \right. \\ &\quad \left. + \frac{8}{\pi^2}\frac{\cos(\omega_s t)}{3} - \dots\right) \end{aligned} \tag{21}$$

where $2\omega_m$ is replaced by ω_s (tone spacing).

In the presence of on-chip bypass capacitor (C_b in Fig. 8), the high frequency components of i_s (the terms with $2\omega_c$ etc.

in (21)) will be bypassed, but not the low frequency beat current at frequency ω_s and its harmonics. The supply current (after on-chip bypassing) looks like the waveform in Fig. 9(d). If large off-chip bypass capacitance is not present, this low frequency beat current will have to flow through the supply line and encounter high inductive/resistive impedance.

This generates a supply ripple at the center-tap of the transformer and the voltage there may be represented as

$$V_{dd} = V_{\rm DD} + A_2 \cdot \cos(\omega_s t) + \text{higher harmonics of } \omega_s. \quad (22)$$

This supply ripple at frequency ω_s will mix with each of the two input tones at frequencies ω_1 and ω_2 to generate additional sidebands at frequencies $\omega_1 - \omega_s, \omega_1 + \omega_s, \omega_2 - \omega_s$ and $\omega_2 + \omega_s$. Among these we can easily see that the tones generated at frequencies $\omega_1 + \omega_s = 2\omega_1 - \omega_2$ and $\omega_2 - \omega_s = 2\omega_2 - \omega_1$ add directly to the third order intermodulation already generated by the transistor, thereby further degrading IM3.

In [8], a two-port Volterra analysis is formulated to quantify the distortion generated by power supply ripple in a power amplifier whose supply is provided by a DC-DC converter. Although the origin of supply ripple in our analysis is different, an analysis similar to [8] can be performed to calculate the distortion sidebands generated as a result of the power supply modulation effects.

The frequency domain Volterra series for a system with two input ports and a single output port can be represented as

$$\begin{aligned} S_o = {} & F_1(\omega_a) \circ S_1 + F_2(\omega_a, \omega_b) \circ S_1^2 \\ & + F_3(\omega_a, \omega_b, \omega_c) \circ S_1^3 + \ldots \\ & + G_1(\omega_a) \circ S_2 + G_2(\omega_a, \omega_b) \circ S_2^2 \\ & + G_3(\omega_a, \omega_b, \omega_c) \circ S_2^3 + \ldots \\ & + H_{11}(\omega_a, \omega_b) \circ (S_1 \cdot S_2) \\ & + H_{12}(\omega_a, \omega_b, \omega_c) \circ S_1 S_2^2 \\ & + H_{21}(\omega_a, \omega_b, \omega_c) \circ S_1^2 S_2 + \ldots \end{aligned} \quad (23)$$

where S_1 and S_2 are the two inputs (input signal at transistor gate and supply ripple at transformer primary center tap respectively in our case) and S_o is the output. Here F_i and G_i represent the conventional Volterra operators, while H_{11}, H_{12}, H_{21} etc. represent the cross terms. For example, F_1 would correspond to the forward gain at an input frequency ω_1, G_1 would correspond to the forward supply noise gain at ω_s, H_{11} would correspond to the sideband at $\omega_1 \pm \omega_s$, and H_{12} and H_{21} would correspond to the third order sidebands at $\omega_1 \pm 2\omega_s$ and $2\omega_1 \pm \omega_s$. The operator "$\circ$" represents frequency domain operation of the kernel on the signals at the appropriate frequencies [10].

The sidebands generated by the fundamental tone of supply voltage ripple mixing with the input signals is given by

$$S(\omega_1 \pm \omega_s) = H_{11} \circ S_1 \cdot S_2 \quad (24)$$

where ω_1 is the input frequency, ω_s is the fundamental frequency of the supply ripple and S_1, S_2 are the magnitudes of the two signals. The solution to H_{11} can be derived from a transistor model including all-nonlinearities and is shown in [8]. It should be noted that (24) remains valid even for a power amplifier with no g_m non-linearity. The equation demonstrates that even if the PA has no g_m non-linearity (i.e., F_2, F_3 and all higher terms are zero), if there is a supply ripple generated at frequency ω_s, then due to a non-zero H_{11} for a practical transistor, there will be third-order intermodulation distortion terms present at the output.

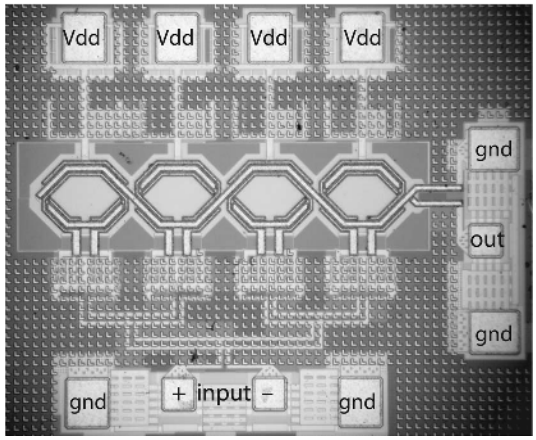

Fig. 10. Die photo of 90 nm CMOS power amplifier.

Thus the following analysis shows the need for off-chip large bypass capacitors to decouple low frequency tones in a two-tone or in general, while applying modulated inputs to the differential PA. On-chip bypass capacitors for decoupling the GHz RF carrier is not sufficient.

V. Experimental Results

The power amplifier using the proposed combiner was fabricated using a 90 nm digital CMOS process utilizing only thin-oxide transistors. The die photo is shown in Fig. 10. The die area is 0.9 mm$\times$ 0.9 mm including the pads. The die was probed using Cascade Microtech differential GSSG probes at the input and single-ended GSG probe at the output. The power output was measured using HP8563E Spectrum Analyzer. Measurement with the spectrum analyzer confirmed that there are no spurious oscillations and the PA is stable at all frequencies.

At a supply voltage of 1 V, the maximum power obtained from the power amplifier is 24.3 dBm with an efficiency of 27%. The cable and probe losses have been carefully de-embedded but the pad losses are included in this number. A plot of the measured and simulated output power versus input drive is shown in Fig. 11. From the plot, the measured 1-dB compression point is calculated at 20.5 dBm. A plot of the measured and simulated drain efficiency versus output power is shown in Fig. 12. The peak drain efficiency (including loss of output power combiner) is 27% and because the amplifier is Class AB in nature, the efficiency drops nearly linearly with decreasing output amplitude. The PAE is not reported since the input impedance of the amplifier is not matched to 50Ω, hence the power gain of the amplifier cannot be properly measured. The input impedance has not been matched since the output stage will be driven by an on-chip driver amplifier.

In order to measure the linearity of the amplifier, a two-tone test was performed. Two tones spaced at 100 MHz and generating a total output power of 20.5 dBm have been applied to the

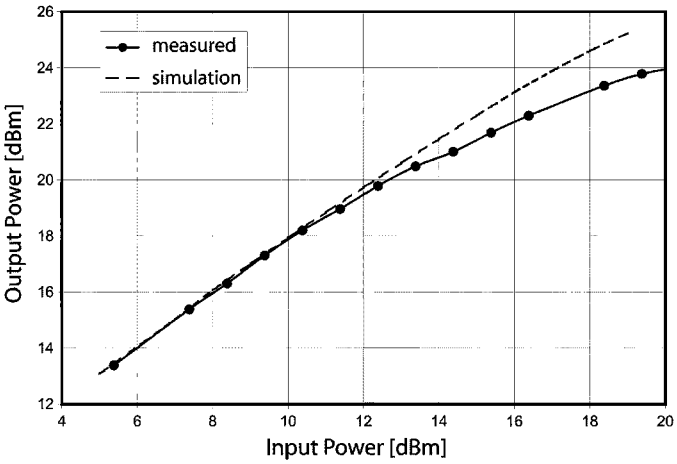

Fig. 11. Measured and simulated output power versus input power.

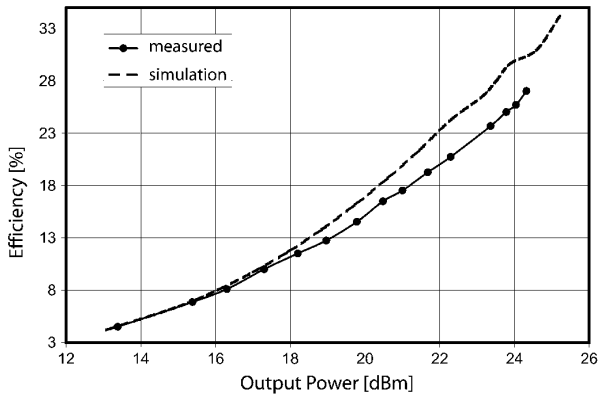

Fig. 12. Measured and simulated efficiency versus output power.

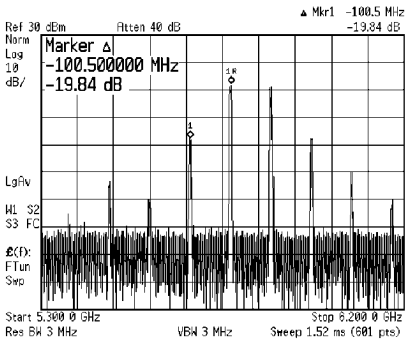

Fig. 13. Measured spectrum for a two-tone test.

input of the PA. As shown in the spectrum of Fig. 13, the measured IM3 at 1-dB compression point is −20 dBc. The simulated value of IM3 at this output power level is −27 dBc. The small-signal and single-tone large-signal measurements with the transformer-coupled power amplifier match the simulations with a good degree of accuracy; however in a two-tone test the measured IM3 at the 1-dB compression point is higher than simulation by about 7 dB. This degradation in IM3 of the amplifier is caused primarily by power-supply modulation effect, as discussed in Section IV. Due to a layout problem, an off-chip decoupling capacitor could not be connected in this version of the chip, and the on-chip capacitor is sufficient to bypass the

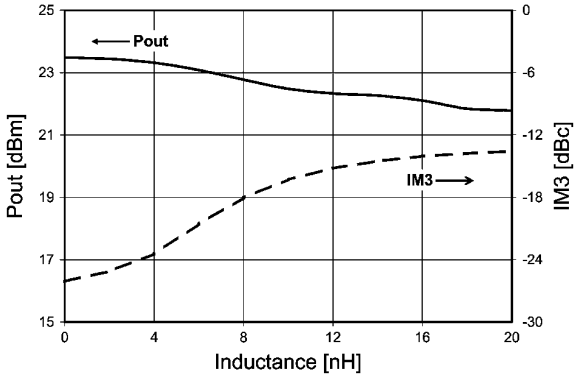

Fig. 14. Degradation in IM3 with increased supply inductance.

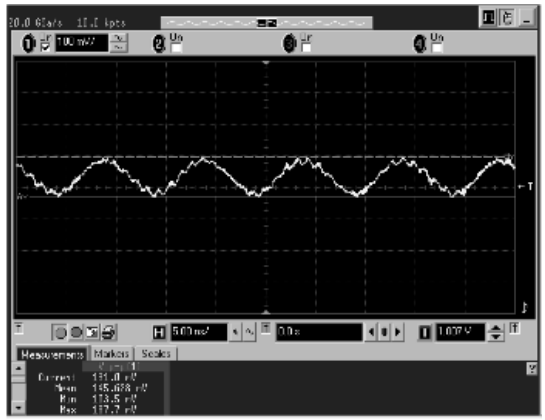

Fig. 15. Measured supply voltage ripple in a two-tone test with 100 MHz tone spacing.

high frequency RF signals, but not the low frequency beat frequency current. As a result, this current has to flow through the supply line, which has high inductance. The resultant voltage ripple causes the IM3 to degrade and the degradation increases with increase in the magnitude of the ripple. This effect has been verified both through simulations and measurements.

Fig. 14 shows the simulated IM3 and fundamental output power (Pout) as the inductance of the supply line is increased from 0 to 20 nH. As clearly seen from the graph, the variation in Pout over the entire range is less than 1.5 dB; however the third-order intermodulation products increase rapidly, degrading IM3 with increase in supply line inductance. Fig. 15 shows the supply ripple measured using an oscilloscope for a two-tone test with 100 MHz tone spacing. Fig. 16 shows the measured IM3 and supply ripple magnitude as a function of the tone spacing. We clearly see as the ripple increases, the IM3 degrades rapidly. The measured IM3 at 200 MHz offset is close to simulation values. We see that the supply ripple is less for 200 MHz tone spacing than 50 MHz, because the on-chip bypass capacitor shunts out more of the beat frequency $(\omega_1 - \omega_2)$ current as the beat frequency itself increases.

The power combiner described in Section II has nearly constant efficiency over the band of interest. Fig. 17 shows the measured output power as a function of frequency. The power amplifier performs well over the whole band, maintaining peak output power greater than 23.5 dBm over the range of 5–5.8 GHz. Compared to state-of-the-art PAs reported in literature, despite using

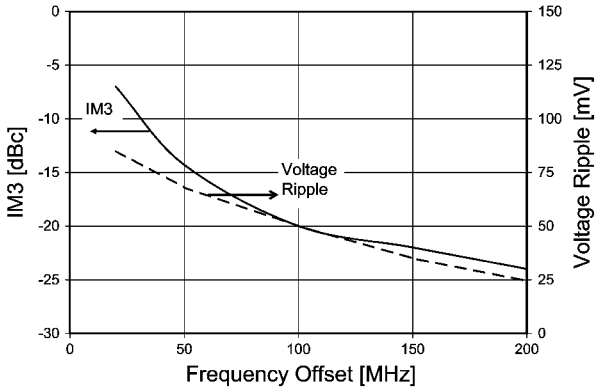

Fig. 16. Measured IM3 degradation and supply voltage ripple in a two-tone test with different tone spacings.

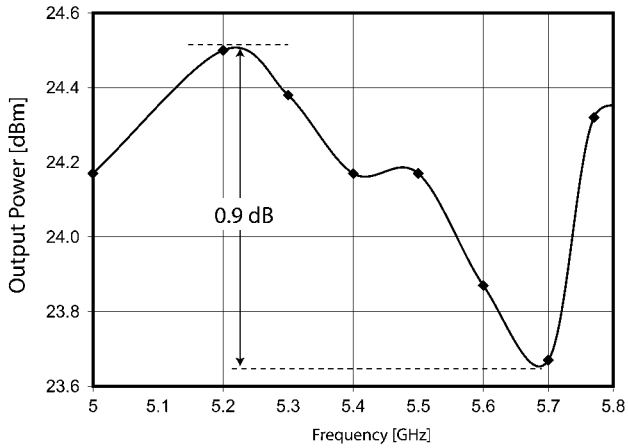

Fig. 17. Measured output power versus frequency.

only 1 V power supply and a digital 90 nm CMOS process, this PA's performance is comparable to many of the designs at higher supply voltage or in processes with RF enhancements.

VI. Conclusion

In this paper, we have presented a CMOS 90 nm power amplifier using thin oxide transistors. A transformer based power combining structure has been designed and used to build a four stage Class AB push pull amplifier. Despite the use of a single 1 V power supply and a digital CMOS process, a high output power of 24.3 dBm at a peak drain efficiency of 27% has been achieved. To the authors' knowledge, this is the highest reported power obtained from a linear power amplifier using 1 V power supply and 90 nm thin oxide transistors.

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