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A 5.8-GHz VCO with CMOS-compatible MEMS inductors

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Abstract

This paper describes a low power, low phase noise 5.8 GHz voltage controlled oscillator (VCO) with on-chip CMOS MEMS inductor. The inductor was fabricated by TSMC 0.18 μm one-poly six-metal (1P6M) CMOS process and also Chip Implementation Center (CIC) micromachining post-process. During the post-process, the dry etching was utilized to remove the oxide between the winding metals and the silicon substrate under the inductor. Due to the alleviation of parasitic capacitance and lossy substrate, the quality factor and resonant frequency will be improved and extended. In this work, quality factor up to 15 was obtained for a 1.88 nH micromachined inductor at 8.5 GHz, and the improvement is up to 88% in maximum quality factor. The CMOS and micromachined inductor were both implemented with a 5.8 GHz VCO. Compared side by side with the CMOS inductor, the CMOS MEMS inductor produced a 5 dB lower phase noise improvement at 1 MHz offset in this 5.8 GHz VCO.

Keywords: CMOS MEMS; Micromachined inductor; Quality factor; VCO; Post-process

1. Introduction

The VCO is one of the important components in any RF/microwave communication system. In a receiver, the oscillator is used together with a mixer to convert the RF signal to an IF signal. The oscillator signal serves as a carrier to modulate low frequency to be transmitted. For a high quality receiver, the LC-oscillator topology is widely chosen because it enables to provide the lowest phase noise for a given amount of power. However, the phase noise and power consumption of LC-type tank oscillator are directly related to the quality factor (Q) of the LC tank. The equivalent quality factor of a LC tank is governed by lower Q factor component; therefore, limited by the CMOS integrated inductor [1].

In standard silicon IC process, the intrinsic problems always deteriorate the performance of passive devices. For example, the stray and parasitic capacitances lower the self-resonance frequency of inductor, and the substrate losses also reduce the Q factor of the device. These inherent problems of the traditional CMOS inductor limit the device performance, and furthermore the specifications of RF circuits, such as the power consumption and phase noise of a VCO circuit. In order to extend the CMOS applications into higher frequency range, the CMOS-compatible micromachining process has been proposed to improve the Q factor and operating frequency of an RF inductor.

In the past 10 years, micromachining techniques have been led into the circuit processes to design a high performance inductor. For example, the surface micromachined solenoid inductors with copper plating, reported on by Kim and Mark [2], can reach to a very high quality value about 60 at 8 GHz. And the selective copper encapsulation on silicon developed by Andrew Yeh et al. [3] also fabricated inductors with quality factor over 30 above 5 GHz. The out-of-plane inductor, reported on by Chua et al. [4], made from a sputtered stress-engineered molybdenum–chromium (MoCr) alloy can make quality factor even reach to 60–85. The above examples employed some respective micromachined processes and materials that can easily make low series resistance and block the lossy path around the device, but they also have the bottleneck to make the total process be compatible with the CMOS.

A similar post-CMOS mask-less micromachining process has been proposed by Carnegie Mellon University. It utilizes

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the top metal as the hard mask to selectively etch the oxide layer; however, the oxide dry etching incorporated with the aluminum may cause the compound aluminum fluoride polymer [5]. This compound polymer then possibly blocks the following etching reaction and fails the releasing process. To avoid the harmful polymer during the etching process, the post-CMOS micromachining process described here will adopt an additional lithography to define the dry etching region. This photoresist layer enables to protect the top metal from the dry etching in reactive ion etching (RIE) and further avoid the polymer problems.

The CMOS MEMS technologies have been widely developed in recent years to alleviate the parasitic problems and increase the functionality in a single chip. This paper proposes the fully compatible CMOS MEMS technologies to improve the characteristics of the inductor, and also verify the improvement with a VCO circuit.

2. CMOS micromachining process

The CMOS MEMS multi-project wafer (MPW) was fabricated by TSMC 0.18 μm one-poly six-metal (1P6M) CMOS process and CIC micromachining post-process. The major materials of metallization and dielectric layer in this CMOS process are aluminum and silicon oxide, respectively. Fig. 1 shows the cross-section views of the MPW with post-CMOS micromachining steps.

For alleviating the dry etching process on dielectric layers, the CMOS passivation layers on etching selective regions are removed during the CMOS process (as Fig. 1(a)). Before the anisotropic dry etching, an additional photoresist layer is spun and lithographed on the wafer for the post-process. This lithography enables to define the protective region of photoresist layer over the metal of the inductor. The thickness of the photoresist requests at least 5 μm to avoid the RIE etching directly on the top meal. The anisotropic RIE etching with CF_4, CHF_3 and O_2 is subsequently used to remove the exposed dielectric oxide in Fig. 1(b). In this step, most photoresist layers would exhaust with the RIE gas. As Fig. 1(c), the following isotropic dry etching with SF_6 and O_2 is then included to remove the underlying silicon substrate and release the microstructures.

The similar post-micromachining process that utilized the top CMOS metal layer as dry etching mask was proposed by [6]. However, direct etching accompanying naked-metal with CHF_3/CF_4 would induce the aluminum fluoride polymer and possibly accumulate surrounding the metal layers. Even higher etching selectivity (lower fluorine-to-carbon ratio) is adopted in RIE recipe, the polymer may still occasionally occur on the etching region and frustrate the following silicon etching. Fig. 2 is an example of CMOS MEMS inductor etching with metal-mask, and the polymer extensively occurs around the etching region. The energy-dispersive spectrometers (EDS) is used to analyze the ingredients of the polymer. Fig. 3 shows the total composing elements of the polymer at 0.5 μm under the surface. The major composing elements are Si and O, and the composite ratio approximates to the chemical formula of silicon-oxide. Other elements are C, F and Al, and the composite ratio of C and F is close to the compound relation between CHF_3 and CF_4. The trace element, Al, is inferred from the strike on metal. The accurate molecular formula of the polymer is difficult to figure out since etching gas chosen in RIE and the total area of naked-metal will both change the composing elements of the polymer. According to above-mentioned reasons, an additional photoresist is necessary to protect the metal layer for better etching performance.

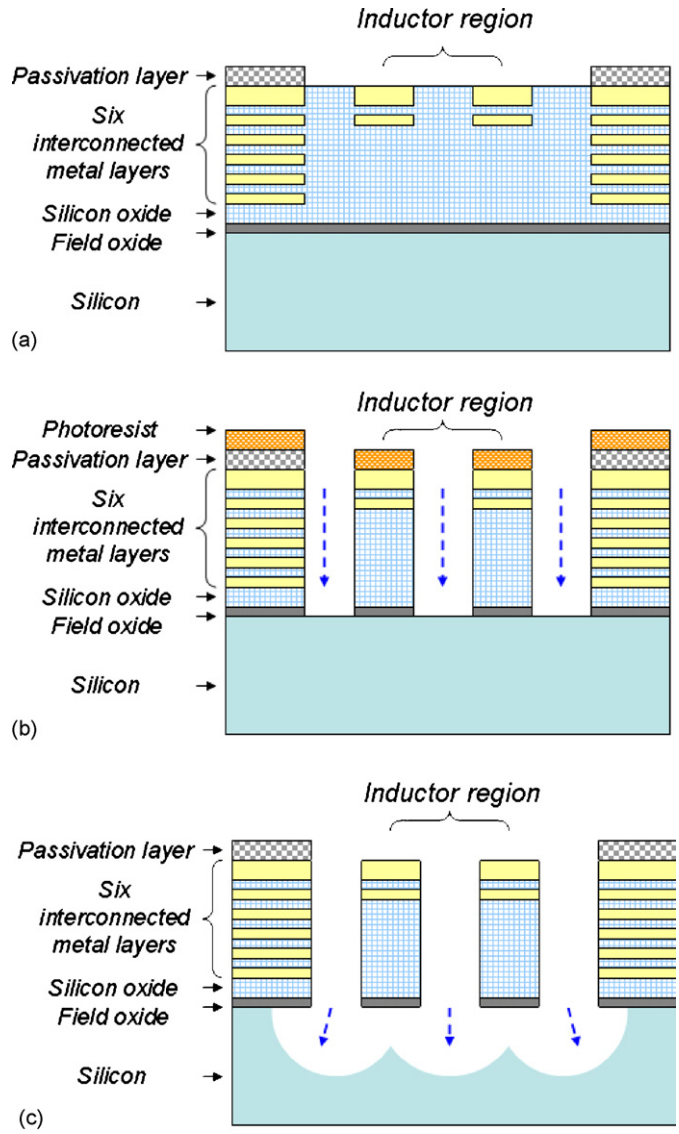


Fig. 1. Post-CMOS micromachining steps: (a) after completion of CMOS, (b) protective photoresist layer and anisotropic dry oxide etching, and (c) the isotropic dry silicon etching and structural release.

After the removal of the parasitic regions and lossy paths around the inductor, the coupling and parasitic capacitances can therefore be suppressed, and the $F_{Q,\max}$ and Q factor are expected to be better after the CMOS MEMS post-process.

3. Model of micromachined inductor

In order to understand the parasitic effect of the silicon substrate, a simplified π model as Fig. 4 is used for the dis-

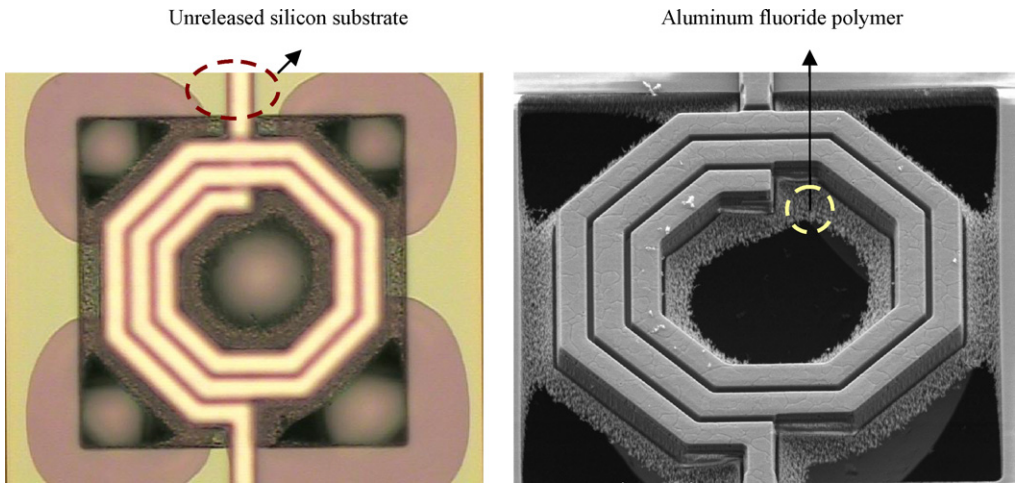
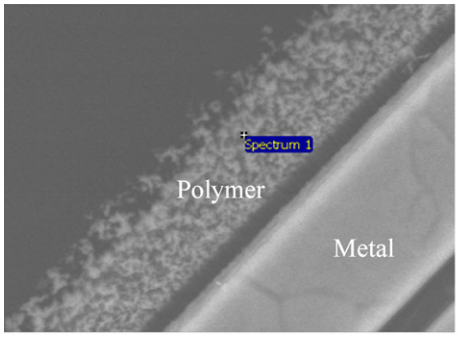


Fig. 2. The aluminum fluoride polymer from the dry etching with metal-mask.



Element	Atomic %
O	62.38
Si	27.59
F	6.84
C	2.56
Al	0.63

Atomic ratio in polymer

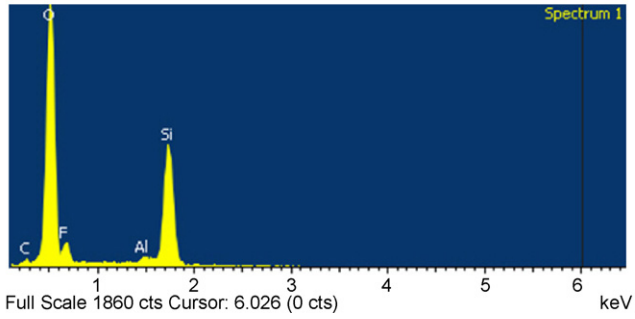


Fig. 3. The composing elements analysis in polymer.

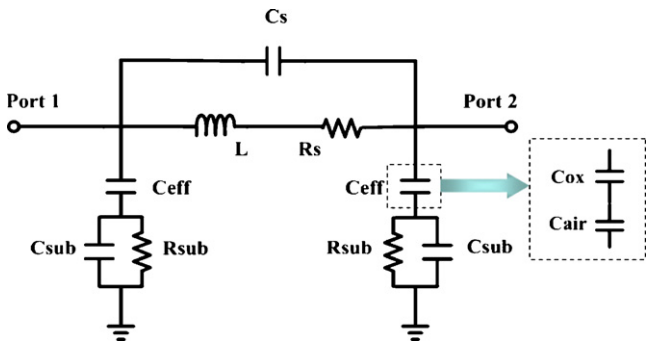


Fig. 4. The lump element model of CMOS MEMS inductor on silicon substrate.

cussion [7]. The self-inductance and series resistance of a spiral inductor is represented by L and R_s, respectively. Series capacitance, C_s, is accounted for the feed-through path due to the capacitive coupling effect between the windings. And the oxide capacitance between the spiral and the field oxide is modeled by C_{ox}. The equivalent capacitor C_{air} is used to model the lossy effect of the released substrate. The C_{ox} and C_{air} are connected series and noted as the C_{eff}. The silicon substrate capacitance and resistance are modeled by C_{sub} and R_{sub}, respectively.

The Q factor of the inductor is defined by the ratio of stored energy to the dissipated energy. If an inductor is modeled by a simple parallel RLC tank, and only the magnetic energy is

considered, the quality factor can be shown that

$$Q = 2\pi \frac{\text{peak magnetic energy} - \text{peak electric energy}}{\text{energy loss in one oscillator cycle}} = \frac{\mathrm{Im}(Z_{11})}{\mathrm{Re}(Z_{11})} \quad (1)$$

where Z_{11} is the input impedance seen at one terminal of the inductor while the other is grounded. According to the model defined in Fig. 4, the calculated result of Q can be expressed as

$$Q = \frac{\omega L_s}{R_s} \frac{R_x}{R_x + [\omega L/R_s)^2 + 1]R_s} \times \left[1 - \frac{R_s^2(C_s + C_x)}{L} - \omega^2 L(C_s + C_x)\right] \quad (2)$$

where

$$R_x = \frac{1}{\omega^2 C_{\text{eff}}^2 R_{\text{sub}}} + \frac{R_{\text{sub}}(C_{\text{eff}} + C_{\text{sub}})^2}{C_{\text{eff}}^2} \quad (3)$$

$$C_x = C_{\text{eff}} \frac{1 + \omega^2 (C_{\text{eff}} + C_{\text{sub}}) C_{\text{si}} R_{\text{sub}}^2}{1 + \omega^2 (C_{\text{eff}} + C_{\text{sub}})^2 R_{\text{sub}}^2} \quad (4)$$

$$C_{\text{eff}} = \frac{C_{\text{ox}} C_{\text{air}}}{C_{\text{ox}} + C_{\text{air}}} \quad (5)$$

The frequency of the maximum Q can be calculated by differentiating the equation Q with frequency. However, the three terms in equation Q all have the factor functioned of frequency, the final differential result will be a complicated formula for partially differential in each term. More reliable and faster estimation of the $F_{Q,\max}$ still requires the help of CAD tools.

4. VCO circuit design

A complementary cross-coupled LC-type VCO with tail current source is chosen in our circuit architecture, and the schematic is shown in Fig. 5. The LC tank is first determined by choosing an inductor with its $F_{Q,\max}$ locates at our desired frequency band. Accumulation mode varactor is chosen to resonate with the inductor to determine the oscillation frequency. In order to compensate the loss in the LC tank, NMOS and PMOS cross-coupled pairs (M2–M3 and M4–M5) are placed parallel with the LC tank to provide negative resistance and sustain the oscillation. The size of M1 is chosen for operating VCO in current limited regime.

The gate width of transistors in cross-coupled pair are chosen for matching the transconductances of NMOS and PMOS to make a more symmetric output swing and reduce flicker noise up-converted into the phase noise. Two self-biased inverters, M6–M7 and M8–M9, are used as the output buffer to isolate the VCO from the 50 Ω termination of the spectrum analyzer.

In practical oscillator, the output signal can be represented as:

$$V_{\text{out}} = A(t)\cos(\omega_0 t + \phi(t)) \quad (6)$$

where $A(t)$ and $\phi(t)$ are both functions of time which represent the fluctuation of amplitude and phase with time variation. In frequency domain, these fluctuations make sidebands close to the frequency of oscillation.

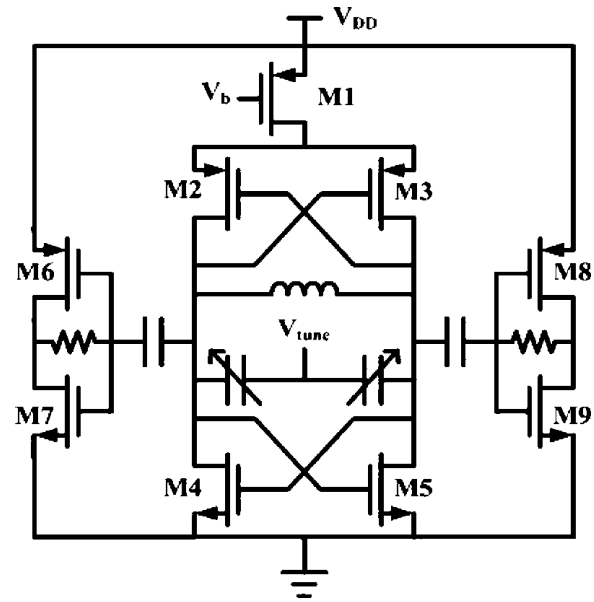


Fig. 5. The schematic of VCO circuit.

Phase noise is defined to quantify the fluctuations in frequency domain, and expressed as the ratio of the single side-band power at a frequency offset $\Delta\omega$ from the carrier with a measurement bandwidth of 1 Hz to the carrier power. The formula of phase noise can be expressed as

$$L\{\Delta\omega\} = 10\log\left[\frac{2FkT}{P_{\text{carrier}}}\left(\frac{\omega_o}{2Q_t\,\Delta\omega}\right)^2\right] \quad (7)$$

where k is the Boltzmann's constant, T the absolute temperature, F an empirical parameter, P_{carrier} the output power of carrier, Q_t the quality factor of the tank, ω_o the oscillation frequency, and $\Delta\omega$ is the offset frequency from the oscillation frequency [8].

According to (7), a high-Q tank can improve the noise shaping effect and the output power of the oscillator when the oscillator is in the current limited regime. In today's CMOS process, the Q factor of inductor is still worse than the capacitor or varactor [9,10]. Therefore, enhancing the Q factor of inductor is quite an effective solution to directly improve the phase noise.

5. Experiment results

5.1. MEMS inductor performance

A 1.88 nH inductor with 2 μm metal thickness, 32.1 μm inner radius, 2.5 turns and 15 μm wide of wires was fabricated in TSMC 0.18 μm CMOS process. After the CMOS, micromachining post-process was applied to fabricate the MEMS inductor. Fig. 6(a and b) show the SEM of CMOS MEMS inductor with hollow silicon substrate, the vertical and lateral etching is around 80 and 50 μm, respectively.

The S-parameters of both inductors were measured by Agilent 8510 network analyzer. The parasitic and stray capacitances around the pad were de-embedded by Y-parameter. The mea-

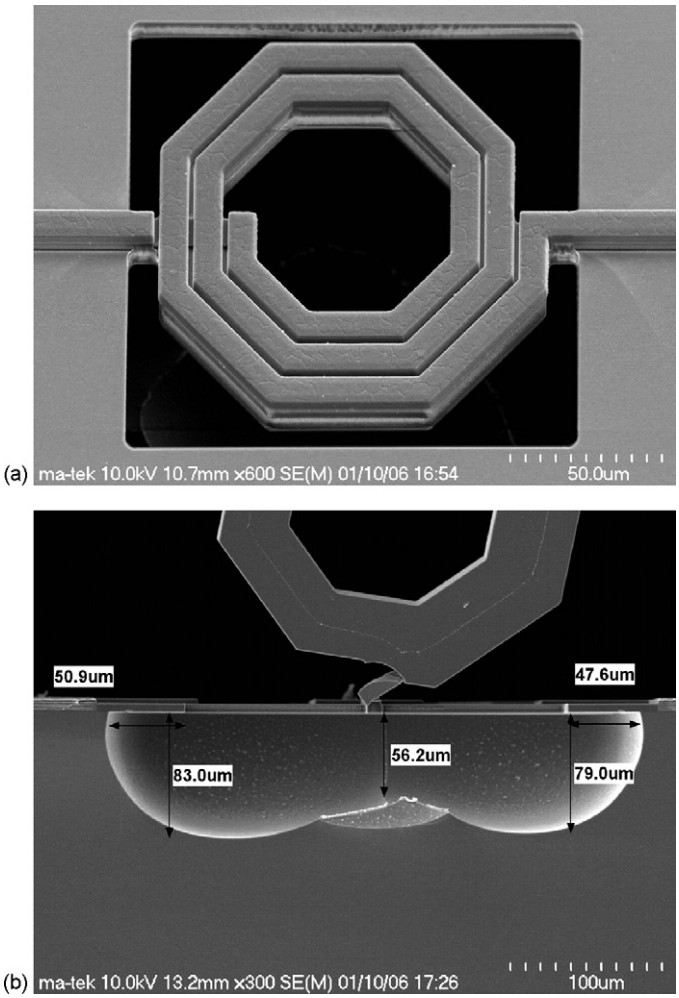


Fig. 6. SEM of CMOS MEMS inductor: (a) a 2.5 turns CMOS MEMS inductor and (b) the substrate etching profile under the CMOS MEMS inductor.

sured inductance and Q factor are both extracted in Fig. 7. The black line means the CMOS MEMS inductor, and the gray line is standard CMOS inductor. Due to the reduction of parasitic capacitance and lossy substrate, the CMOS MEMS inductor has a higher Q factor and $F_{Q,\max}$. In this measurement, the $F_{Q,\max}$ of

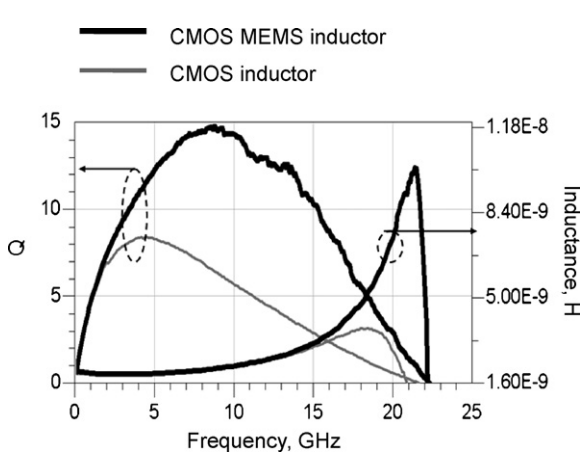


Fig. 7. The measured Q factor and inductance for CMOS and CMOS MEMS inductors.

Table 1
Extracting elements of the inductor model

	CMOS inductor	CMOS MEMS inductor
C_s (fF)	15.2	14.3
R_s (Ω)	3	3
L (nH)	1.88	1.88
C_{eff} (fF)	156	51
C_{sub} (fF)	14.5	16.6
R_{sub} (Ω)	850	2500

CMOS MEMS inductor shifts from 4 to 8.5 GHz and the $Q_{\max}$ raises from 8 to 15, this means an increase of 88% in $Q_{\max}$. The micromachined inductance at low frequency is still around 1.88 nH, hence it becomes more attractive with higher Q factor and available frequency range. The Q factor of the inductor in our design frequency range also rises from 8 to 13.5. The equivalent model elements of CMOS and MEMS inductors in Table 1 are also extracted from the measurement. The C_{eff} drops to 51 fF from 156 fF due to the effect of C_{air}, and the substrate resistance rises to 2500 Ω from 850 Ω due to the removal of the lossy substrate. The C_s also has a slight decrease by the etching removal of the gap insulator.

5.2. VCO performance

Table 2 summarizes the measured oscillator characteristics in CMOS and CMOS MEMS VCO. The CMOS MEMS VCO oscillates at 5.81 GHz and shows a phase noise of −117 dBc/Hz at 1 MHz offset while dissipating only 7.23 mW. The achieved phase noise of the CMOS VCO is −112 dBc/Hz at 1 MHz offset. Comparing to the CMOS VCO, the CMOS MEMS VCO has a 5 dB improvement at 1 MHz offset due to the use of high-Q CMOS MEMS inductor. Fig. 8 is the chip of CMOS MEMS VCO with micromachined inductors, and Fig. 9 shows the phase noise measurement of CMOS MEMS VCO at $V_{tune} = 0$ V. Table 3 summarizes this VCO with other previously published VCO employing micromachined inductors. The wide used definition of figure-of-merit (FOM) is as follows,

$$\mathrm{FOM} = 10\log\left\{\left(\frac{f_0}{\Delta f}\right)^2 \frac{1}{L\{\Delta f\}P}\right\} \tag{8}$$

where f_0 is the carrier frequency, Δf the offset from f_0, $L\{\Delta f\}$ is the phase noise at the offset and P is the power consumption of the core circuit in mW.

Table 2
Summary of VCO characteristics

	CMOS	CMOS MEMS
Supply voltage (V)	1.5	
Tuning voltage (V)	0–1.5	
Current consumption (mA)	5.8	4.82
Frequency (GHz)	5.92–6.6	5.81–6.54
VCO gain (MHz/V)	600	640
Output power (dBm)	−4.02	−4.28
Phase noise (dBc/Hz)	−112 at 1 MHz (5.92 GHz)	−117 at 1 MHz (5.81 GHz)

Table 3
Comparison of VCO with MEMS inductor

	Technologies			
	CMOS inductor with compatible MEMS process (this work)	Electroless plated copper inductor on BJT (Ref. [11])	Electroplated copper inductor on CMOS (Ref. [12])	Surface MEMS inductor on Bi-CMOS (Ref. [4])
f_0 (GHz)	5.8	2	2.6	1.2
f_{offset} (Hz)	1,000,000	100,000	600,000	100,000
Inductor Q	8 → 13 (at 5.8 GHz)	5.5 → 16 (at 2 GHz)	27 (at 2.6 GHz)	8 → 35 (at 1.2 GHz)
PN (dBc/Hz)	−117	−106	−122	−111
P_{sup} (mW)	7.23	18.2	15	11.2
FOM (dB)	184	179	183	182

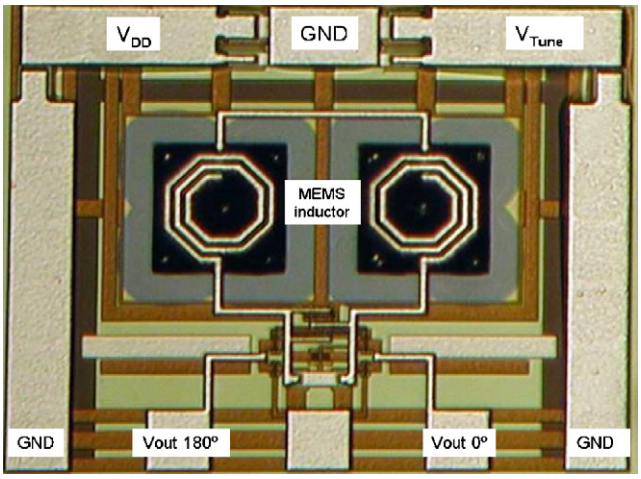


Fig. 8. The photo of the VCO circuit with micromachined inductor.

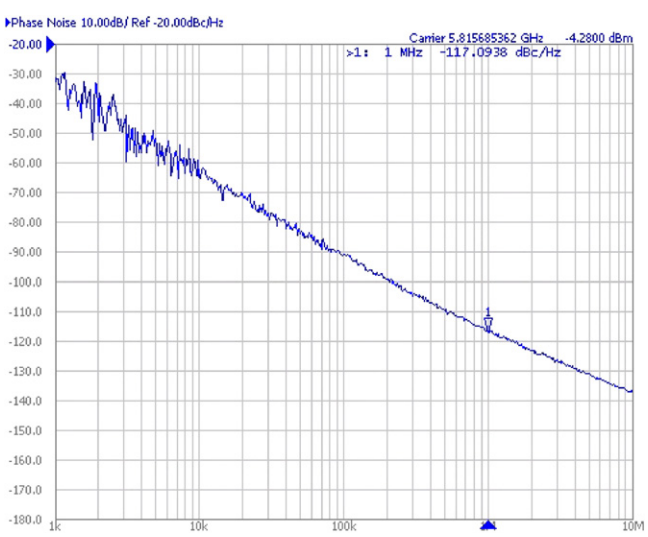


Fig. 9. The phase noise measurement of CMOS MEMS VCO.

6. Conclusion

In this paper, the post-CMOS micromachining process is utilized to obtain an enhanced Q factor inductor. The post-process here is simply and fully compatible with standard CMOS process. Conventional CMOS and micromachined inductor are both verified with the LC-type VCO. We have achieved high-Q factors over 13 at 5.8 GHz and 15 at 8.5 GHz, respectively. A 5.8 GHz LC-type VCO has been designed and fabricated by TSMC 0.18 μm CMOS process. From the CMOS MEMS VCO with micromachined inductors, phase noise as −117 dBc/Hz has been achieved and has a 5 dB improvement comparing to the CMOS VCO. We have successfully demonstrated a fast and fully compatible solution to improve the performance of CMOS inductor and also its circuits.

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Biographies

Sheng-Hsiang Tseng was born in Hsinchu, Taiwan, ROC, in 1977. He received the BS degree in electrical engineering from National Chung Hsing University, Taichung, Taiwan, in 1999 and the MS degree in institute of electronics engineering from National Tsing Hua University, Hsinchu, Taiwan, in 2001, respectively. From 2002, he has worked at Chip Implementation Center (CIC), National Applied Research Laboratories, on CMOS MEMS design. He is currently working toward the PhD degree in institute of electronics engineering at National Tsing Hua University. His research interests include MEMS technologies, micro-sensor and micro-actuator design and simulation, on-chip RF MEMS devices, and integrated CMOS MEMS ICs.

Ying-Jui Hung received the MS degree in electronics engineering from the National Chiao-Tung University, Hsinchu, Taiwan, in 2005. He is currently an assistant researcher at the National Chip Implementation Center, Hsinchu, Taiwan. His current research interests include the RF VCO circuit design and applications of MEMS devices for RF circuit design.

Ying-Zong Juang received the MS and PhD degrees in electrical engineering from National Cheng Kung University, Taiwan, in 1992 and 1998, respectively. He joined the institute of Chip Implementation Center, Science-Based Industrial Park, Hsinchu, in October 1998. At CIC, he has majored in the RF circuit design and device modeling, furthermore, from 1999 to 2000, he joined a project to create a new process flow to implement the BCD devices on the same chip. Now, he is the researcher and deputy director of CIS/CIC. He organized several projects including 5 GHz transceiver for IEEE 802.11a, frequency synthesizer integrated for IEEE 802.11b, and 0.35 μm CMOS/MEMS design environment. His interested topics include RF/MEMS module design, RF MEMS devices design and simulation, and mixed-signal design for RF front-end.

Michael S.-C. Lu was born in Taipei, Taiwan, ROC, in 1968. He received the BS and MS degrees in power mechanical engineering from National Tsing Hua University, Hsinchu, Taiwan, in 1991 and 1993, respectively. In 2002, he received the PhD degree in electrical engineering from Carnegie Mellon University, Pittsburgh, PA. Since August 2002, he has been an assistant professor with the Department of the Electrical Engineering and the Electronics Institute at National Tsing Hua University, Taiwan. His research interests include integrated CMOS-micromachined sensors and actuators, probe-based data storage and manipulation, and control systems.